MP1530

Triple Output Step-Up Plus Charge Pump for TFT Bias

Monolithic Power Systems

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General Description

The MP1530 is a triple output step-up converter with charge-pumps to make a complete DC/DC converter to power a TFT LCD panel from a regulated 3.3V or 5V supply.

The MP1530 includes a 1.4MHz fixed-frequency step-up converter and a positive and negative linear regulator. The linear regulators are powered from a charge-pump driven by the step-up converter switch node.

A single on/off control enables all 3 outputs. The outputs are internally sequenced at power-on for ease of use. An internal soft-start prevents overloading the input source at startup. Cycle-by-cycle current limit reduces component stress.

The MP1530 is available in both a tiny 3mm by 3mm, 16 pin QFN package and a 16 pin TSSOP package.

Ordering Information

Part Number *	Package	Temperature
MP1530DQ	QFN16 (3x3)	-40°C to + 85°C
MP1530DM	TSSOP16	-40°C to + 85°C

* For Tape & Reel use suffix - Z (e.g. MP1530DQ-Z)

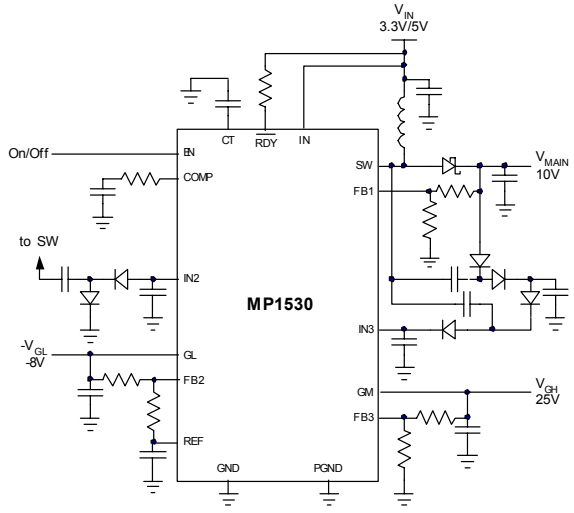
Features

- 2.7 to 5.5V Operating Input Range
- 2.8A Switch Current Limit
- 3 Outputs In Single Package
  - Step-Up Converter up to 22V
  - Positive 20mA Linear Regulator
  - Negative 20mA Linear Regulator
- 250mΩ Internal Power MOSFET Switch
- Up to 95% Efficiency
- 1μA Shutdown Mode
- Fixed 1.4MHz frequency
- Positive Regulator up to 38V
- Negative Regulator down to -20V
- Internal Power-On Sequencing
- Adjustable Soft-Start/ Fault Timer
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Under Voltage Lockout
- Ready Flag
- Available in 16 Pin TSSOP & 3mm x 3mm QFN Packages

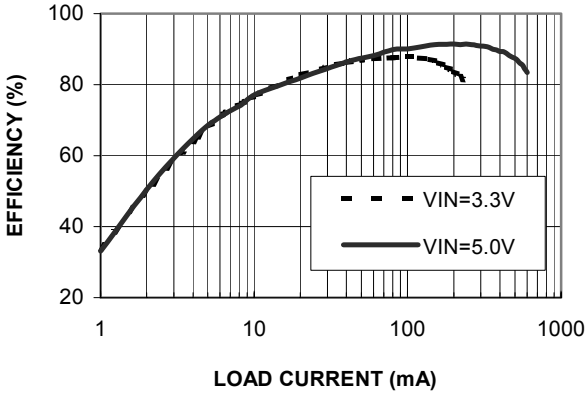
Applications

- TFT LCD Displays
- Portable DVD Players
- Tablet PCs
- Car Navigation Displays

Typical Application Circuit



Step Up Converter Efficiency vs. Load Current (V_{MAIN}=13V)



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Absolute Maximum Ratings	**(Note 1)**
IN Supply Voltage	-0.3V to 6V
SW Voltage	-0.3V to 25V
IN2, GL Voltage	0.3V to -25V
IN3, GH Voltage	-0.3V to 40V
IN2 to IN3 Voltage	-0.3V to 60V
All Other Pins	-0.3V to 6V
Junction Temperature	125°C
Lead Temperature	260°C
Storage Temperature	-65°C to 150°C

Recommended Operating Conditions	**(Note 2)**
Input Voltage	2.7V to 5.5V
Main Output Voltage	V_{IN} to 22V
IN2, GL Voltage	0V to -20V
IN3, GH Voltage	0V to 38V
Operating Temperature	-40°C to 85°C

Package Thermal Characteristics	**(Note 3)**
Thermal Resistance, θ_{JA} (3x3QFN-16)	60°C/W
Thermal Resistance, θ_{JA} (TSSOP-16)	100°C/W

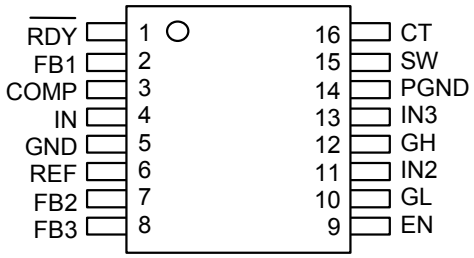
Electrical Characteristics (V_{IN} = 5.0V, T_A = 25°C, unless specified otherwise. Note 4)

Parameters	**Symbol**	**Condition**	**Min**	**Typ**	**Max**	**Units**
Input Voltage Range	V_{IN}		2.7		5.5	V
IN Undervoltage Lockout Threshold	V_{UVLO}	IN Rising	2.25		2.65	V
IN Undervoltage Lockout Hysteresis				100		mV
IN Shutdown Current		V_{EN}≤0.3V		0.5	1	µA
IN Quiescent Current		V_{EN}>2V, V_{FB1}=1.4V		1.3	1.6	mA
EN Input High Voltage	V_{EN}	EN Rising	1.6			V
EN Input Low Voltage					0.3	V
EN Hysteresis				100		mV
EN Input Bias Current					1	µA
Oscillator						
Switching Frequency	f_{sw}		1	1.4		MHz
Maximum Duty Cycle	D_M		85	90		%
Soft Start Period		C_{CT}=10nF		6		ms
Regulator #2 Turn-On/Turn-Off Delay				3		µs
		C_{CT}=10nF		6		ms
Error Amplifier						
Error Amplifier Voltage Gain	Av_{EA}			400		V/V
Error Amplifier Transconductance	Gm_{EA}			1000		µA/V
COMP Maximum Output Current				±100		µA
FB1, FB3 Regulation Voltage			1.22	1.25	1.28	V
FB2 Regulation Voltage			-25	0	25	mV
FB1, FB3 Input Bias Current		V_{FB1}=V_{FB3}=1.25V		±100		nA
FB2 Input Bias Current		V_{FB2}=0V		±100		nA
Reference (REF)						
REF Regulation Voltage		I_{REF}=50µA	1.22	1.25	1.28	V
REF Load Regulation		0µA < I_{REF} < 200µA		1	1.2	%
Output Switch (SW)						
SW On resistance		V_{IN}=5V		250		mΩ
		V_{IN}=3V		400		mΩ
SW Current Limit	I_{LIM}		2.8	3.6		A

Parameters	Symbol	Condition	Min	Typ	Max	Units
SW Leakage current		V_{SW}=22V		0.5	1	µA
GL Dropout Voltage **(Note 5)**		V_{GL}=-10V, I_{GL}=-20mA			0.3	V
GH Dropout Voltage **(Note 5)**		V_{GH}=20V, I_{GH}=20mA			1	V
GL Leakage Current		V_{IN2}=-15V, V_{GL}=GND			1	µA
GH Leakage Current		V_{IN3}=25V, V_{GH}=GND			1	µA
Thermal Shutdown				160		°C

Note 1. Exceeding these ratings may damage the device.
Note 2. The device is not guaranteed to function outside its operating rating.
Note 3. Measured on approximately 1" square of 1 oz. copper.
Note 4. Typical values are guaranteed by design, not production tested.
Note 5. Dropout Voltage is the input to output differential at which the circuit ceases to regulate against further reduction in input voltage.

Pin Description



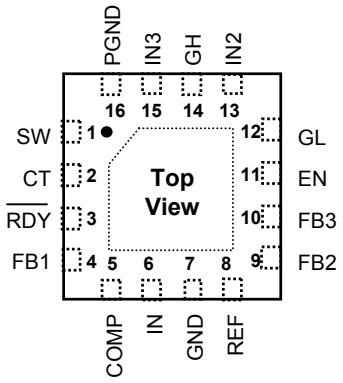


Table 1: Pin Designators

QFN	TSSOP	Name	Function
1	15	SW	Step-Up Converter Power Switch Node. Connect an inductor between the input source and **SW**, and connect a rectifier from **SW** to the main output to complete the step-up converter. **SW** is the drain of the internal 250mΩ N-channel MOSFET switch.
2	16	CT	Timing Capacitor for power supply soft-start and power-on sequencing. A capacitor from **CT** to **GND** controls the soft-start and sequencing turn-on delay periods. See *Power-On Sequencing and Start Up Timing Diagram*.
3	1	$\overline{\text{RDY}}$	Regulators Not Ready. During startup **$\overline{\text{RDY}}$** will be left high. Once the turn-on sequence is complete, this pin will be pulled low if all **FB** voltages exceed 80% of their specified thresholds. After all regulators are turned-on, a fault in any regulator that causes the respective FB voltage to fall below 80% of its threshold will cause **$\overline{\text{RDY}}$** to go high after approximately 15µs. If the fault persists for more than approximately 6ms (for C_{CT}=10nF), the entire chip will shut down. See *Fault Sensing and Timer*.
4	2	FB1	Step-Up Converter Feedback Input. **FB1** is the inverting input of the internal error amplifier. Connect a resistive voltage divider from the output of the step-up converter to **FB1** to set the step-up converter output voltage.
5	3	COMP	Step-Up Converter Compensation Node. **COMP** is the output of the error amplifier. Connect a series RC network to compensate the regulation control loop of the step-up converter.
6	4	IN	Internal Power Input. **IN** supplies the power to the MP1530. Bypass **IN** to **PGND** with a 10µF or greater capacitor.
7	5	GND	Signal Ground.
8	6	REF	Reference Output. **REF** is the 1.25V reference voltage output. Bypass **REF** to **GND** with a 0.1µF or greater capacitor. Connect **REF** to the low-side resistor of the negative linear regulator feedback string.
9	7	FB2	Negative Linear Regulator Feedback Input. Connect the **FB2** feedback resistor string between **GL** and **REF** to set the negative linear regulator output voltage. **FB2** regulation threshold is **GND**.
10	8	FB3	Positive Linear Regulator Feedback Input. Connect the **FB3** feedback resistor string between **GH** and **GND** to set the positive linear regulator output voltage. **FB3** regulation threshold is 1.25V.
11	9	EN	On/Off Control Input. Drive **EN** high to turn on the MP1530, drive **EN** low to turn it off. For automatic startup, connect **EN** to **IN**. Once the MP1530 is turned on, it sequences the outputs on (See *Power-On Sequencing*). When turned off, all outputs are immediately disabled.
12	10	GL	Negative Linear Regulator Output. **GL** is the output of the negative linear regulator. **GL** can supply up to 20mA to the load. Bypass **GL** to **GND** with a 1µF or greater, low-ESR, ceramic capacitor.
13	11	IN2	Negative Linear Regulator Input. **IN2** is the input of the negative linear regulator. Drive **IN2** with an inverting charge pump powered from **SW**. **IN2** can go as low as -20V. For QFN package **IN2** connects to exposed pad.
14	12	GH	Positive Linear Regulator Output. **GH** is the output of the positive linear regulator. **GH** can supply as much as 20mA to the load. Bypass **GH** to **GND** with a 1µF or greater, low-ESR, ceramic capacitor.
15	13	IN3	Positive Linear Regulator Input. **IN3** is the input to the positive linear regulator. Drive **IN3** with a doubling, tripling, or quadrupling charge pump from **SW**. **IN3** voltage can go as high as 38V.
16	14	PGND	Power Ground. **PGND** is the source of the internal 250mΩ N-channel MOSFET switch. Connect **PGND** to **GND** as close to the MP1530 as possible.

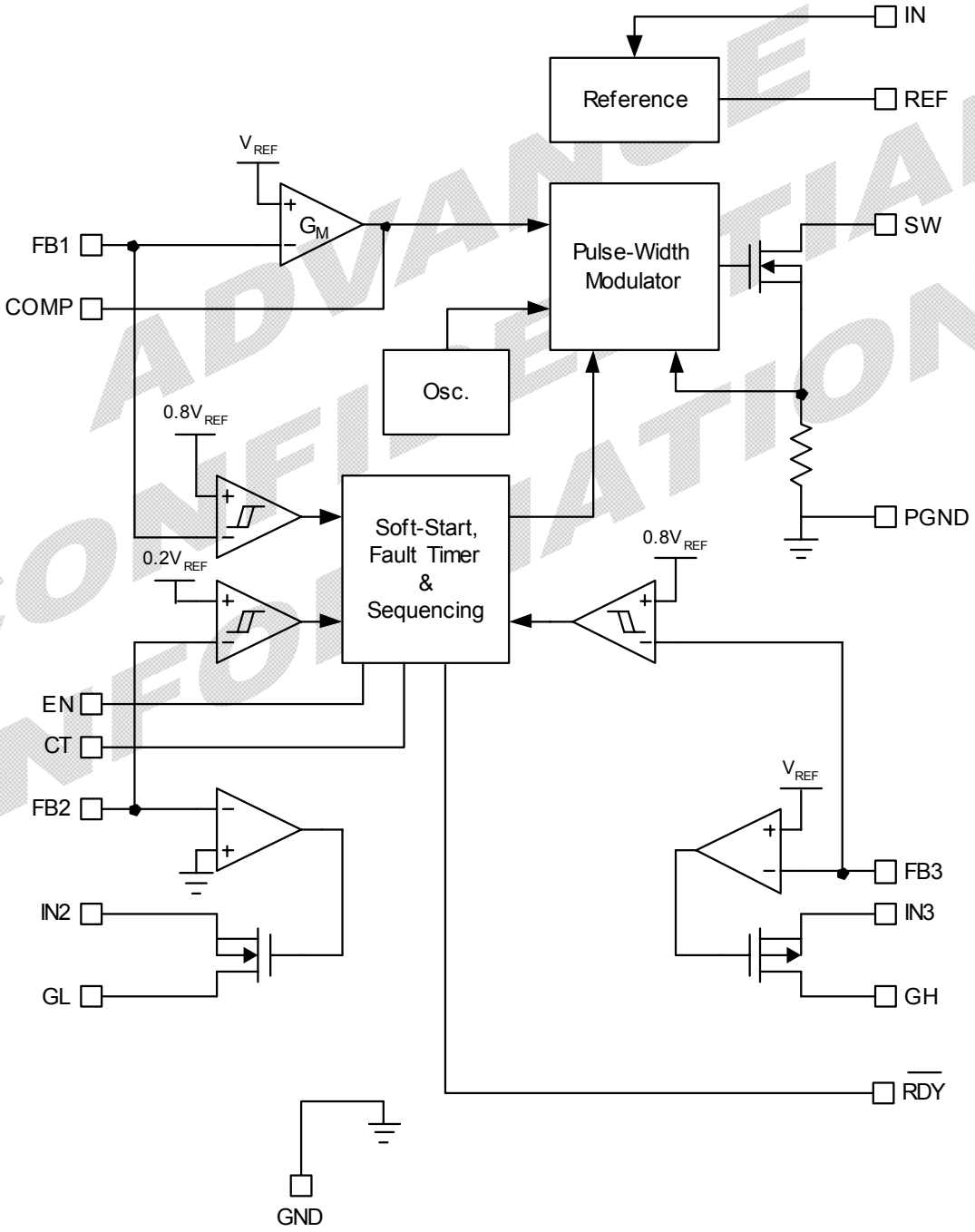


Figure 1: Internal Block Diagram

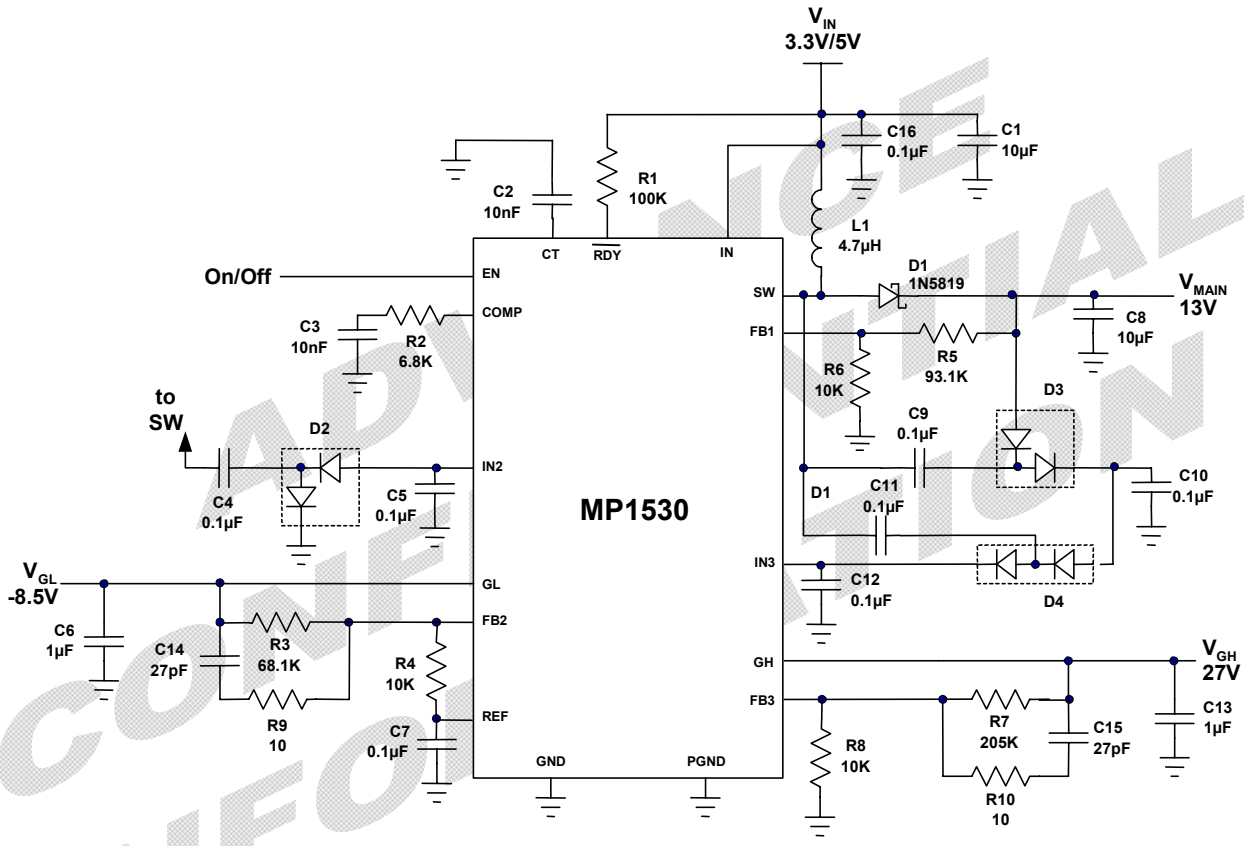


Figure 2: Triple Output Boost Application Circuit

Table 2. Component / Supplier List for Figure 2

Designator	Description	Manufacturer	Phone	Fax	Website
C1	10V, X5R, 1210, Ceramic Capacitor, 1210ZD106MAT	AVX	408-436-5400	408-437-1500	www.avx.com
C8	25V, X5R, 1210 Ceramic Capacitor, 12103D106MAT	AVX	408-436-5400	408-437-1500	www.avx.com
C6	25V, X7R, 1206 Ceramic Capacitor, 12063C105KAT	AVX	408-436-5400	408-437-1500	www.avx.com
C13	50V, X7R, 1210 Ceramic Capacitor, 12105C105KAT	AVX	408-436-5400	408-437-1500	www.avx.com
D1	1A 40V Schottky Diode, SOD-123, 1N5819HW-7	Diodes Inc	805-446-4800	805-446-4850	www.diodes.com
D2, D3, D4	200mA 40V Dual Schottky Diodes, SOT23, BAS40-04-7	Diodes Inc	805-446-4800	805-446-4850	www.diodes.com
L1	2.26A Inductor, SMD, Unshielded 817FY-4R7M=P3	Toko	847-297-0070	847-699-7864	www.toko.com

Functional Description

The MP1530 is a step-up converter with two integrated linear regulators to power TFT LCD panels. Typically the linear regulators are powered from diode charge-pumps driven from the switch node (**SW**). The user can set the positive charge-pump to be a doubler, tripler, or quadrupler to achieve the required linear regulator input voltage for the selected output voltage. Typically the negative charge-pump is configured as a 1x inverter.

Step-Up Converter

The step-up, fixed-frequency, 1.4MHz converter employs a current-mode control architecture that maximizes loop bandwidth to provide fast-transient responses needed for TFT LCD drivers. High switching frequency allows for smaller inductors and capacitors minimizing board space and thickness.

Linear Regulators

The positive linear regulator (**GH**) uses a P-channel pass element to drop the input voltage down to the regulated output voltage. The feedback of the positive linear regulator is a conventional error amplifier with the regulation threshold at 1.25V.

The negative linear regulator (**GL**) uses a N-channel pass element to raise the negative input voltage up to the regulated output voltage. The feedback threshold for the negative linear regulator is ground. The resistor string goes from **REF** (1.25V) to **FB2** and from **FB2** to **GL** to set the negative output voltage, **GL**.

The difference between the voltage at **IN3** and the voltage at **IN2** is limited to 60V abs. max.

Fault Sensing and Timer

Each of the 3 outputs has an internal comparator that monitors its respective output voltage by measuring the voltage at its respective **FB** input. When any **FB** input indicates that the output voltage is below approximately 80% of the correct regulation voltage, the fault timer enables and the $\overline{\textbf{RDY}}$ pin goes high. The fault timer uses the same **CT** capacitor as the soft-start sequencer. If any fault persists to the end of the fault timer (One **CT** cycle is 6ms for a 10nF capacitor), all outputs are disabled. Once the outputs are shut down due to the fault timer, the MP1530 must be re-enabled by either cycling **EN** or by cycling the input power. When re-enabled, the MP1530 cycles through the normal power-on sequence. If the fault persists for less than the fault timer period, $\overline{\textbf{RDY}}$ will be pulled low and the part will function as though no fault has occurred.

Power-On Sequencing and Soft-Start

The MP1530 automatically sequences its outputs at startup. When **EN** goes from low to high, or if **EN** is held high and the input voltage **IN** rises above the under-voltage lockout threshold, the outputs turn on in the following sequence:

1. step up converter
2. negative linear regulator (**GL**)
3. positive linear regulator (**GH**)

Each output turns on with a soft-start voltage ramp. The soft-start ramp period is set by the timing capacitor connected between **CT** and **GND**. A 10nF capacitor at **CT** sets the soft-start ramp period to 6ms. The timing diagram is shown in Figure 3.

After the MP1530 is enabled, the power-on reset spans three periods of the **CT** ramp. First the step-up converter is powered up with reference to the **CT** ramp and allowed one period of the **CT** ramp to settle. Next the negative linear regulator (**GL**) is soft-started by ramping **REF,** which coincides with the **CT** ramp, and also allowed one **CT** ramp period to settle.

The positive linear regulator (**GH**) is then soft-started and allowed to settle in one period of **CT** ramp. Nine periods of the **CT** ramp have occurred since the chip enabled. If all outputs are in regulation (>80%), the **CT** will stop ramping and be held at ground. The $\overline{\textbf{RDY}}$ pin will be pulled down to an active low. If any output remains below regulation (<80%) before and through the nine **CT** periods, $\overline{\textbf{RDY}}$ will remain high and **CT** will begin its fault timer pulse.

Start-Up Timing Diagram

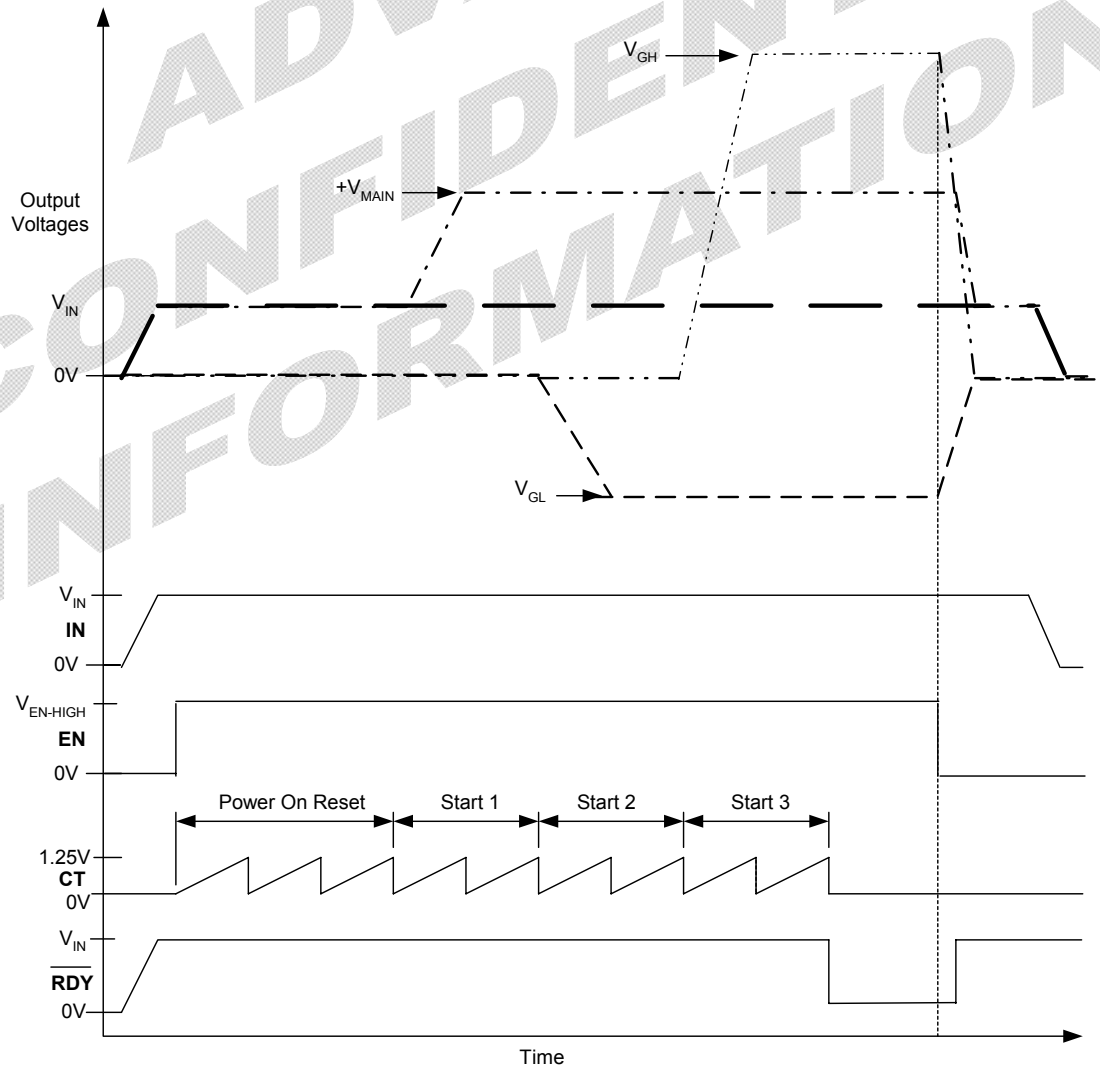


Figure 3: Start-Up Timing Diagram

Design Procedure

Setting the Output Voltages

Set the output voltage on each output by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the feedback threshold voltage. Use 10KΩ to 50KΩ for the low-side resistor R_L of the voltage divider.

For the step-up converter, determine the high-side resistor R_H by the equation:

$$R_H = (V_{MAIN} - V_{FB1}) / (V_{FB1} / R_L)$$

Where V_{MAIN} is the output voltage of the step-up converter.

For the positive charge-pump, determine the high-side resistor R_H by the equation:

$$R_H = (V_{GH} - V_{FB3}) / (V_{FB3} / R_L)$$

For the negative charge-pump, determine the high-side resistor R_H by the equation:

$$R_H = -V_{GL} / (V_{REF} / R_L)$$

Selecting the Inductor

The inductor is required to force the higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current that results in lower peak inductor current, reducing stress on the internal N-channel switch. However, the larger value inductor has a larger physical size, higher series resistance, lower saturation current for a given package size.

Choose an inductor that does not saturate at the device current limit. A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum load current. Make sure that the peak inductor current is below the device current limit to prevent loss of regulation. Calculate the required inductance value by the equation:

$$L = (V_{IN} * (V_{MAIN} - V_{IN})) / (V_{MAIN} * f_{SW} * \Delta I)$$

Where V_{IN} is the input voltage, f_{SW} is the switching frequency, and ΔI is the peak-to-peak inductor ripple current.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. A low ESR capacitor is required to keep the noise at the IC to a minimum. Since it absorbs the input switching current it requires an adequate ripple current rating. Use a capacitor with RMS current rating greater than the inductor ripple current (see *Selecting The Inductor* to determine the inductor ripple current). One 10µF ceramic capacitor is used in the application circuit of Figure 2 because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up converter typically runs directly from the output of another regulated supply. Typically, the input capacitance can be reduced below the value used in the typical application circuit.

To insure stable operation place the input capacitor as close to the IC as possible. Alternately a smaller high quality 0.1µF ceramic capacitor may be placed closer to the IC if the larger capacitor is placed further away.

Selecting the Rectifier Diodes

The MP1530's high switching frequency demands high-speed rectifiers. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. Typically, a 1A Schottky diode

is recommended for the step-up converter. 100mA Schottky diodes such as Central Semiconductor CMPSH-3 are recommended for low current charge-pump circuits.

Selecting the Output Capacitor of the Step-Up Converter

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple to a minimum. The characteristics of the output capacitor also affect the stability of the regulation control system. A 10µF ceramic capacitor works well in most applications. In the case of ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE} \sim= (1- (V_{IN}/ V_{MAIN})) * I_{LOAD} / (2*C_{MAIN}*f_{SW})$$

Where V_{RIPPLE} is the output ripple voltage, I_{LOAD} is the load current, and C_{MAIN} is the capacitance of the output capacitor of the step-up converter.

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meets the output requirement.

The number of positive charge-pump stages N_{POS} is given by:

$$N_{POS} = (V_{GH}+V_{DROPOUT} - V_{MAIN}) / (V_{MAIN} - 2* V_D)$$

Where V_D is the forward voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator.

The number of negative charge-pump stages N_{NEG} is given by:

$$N_{NEG} = (-V_{GL}+V_{DROPOUT}) / (V_{MAIN} - 2* V_D)$$

Use $V_{DROPOUT}$ = 1V for positive charge-pump and $V_{DROPOUT}$ = 0.3V for negative charge-pump.

Selecting the Flying Capacitor in Charge-Pump Stages

Increasing the flying capacitor C_X values increases the output current capability. A 0.1µF ceramic capacitor works well in most low current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > N * V_{MAIN}$$

Where N is the stage number in which the flying capacitor appears.

Step-Up Converter Compensation

The MP1530 uses current mode control which unlike voltage mode has only a single pole roll off due to the output filter. The DC gain (A_{VDC}) is equated from the product of current control to output gain ($A_{VCSCONTROL}$), error amplifier gain (A_{VEA}), and the feedback divider.

$$A_{VDC} = A_{VCSCONTROL}*A_{VEA}*V_{FB1} / V_{MAIN}$$

$$A_{VDC} = 4*V_{IN}/(I_{LOAD})*400*V_{FB1}*V_{MAIN}$$

The output filter pole is given in hertz by:

$$f_{FILTERPOLE} = I_{LOAD} / (\pi*V_{MAIN}*C_{MAIN})$$

The output filter zero is given in hertz by:

$$f_{FILTERZERO} = 1 / (2*\pi*R_{ESR}*C_{MAIN})$$

Where R_{ESR} is the output capacitor's equivalent series resistance.

With all boost regulators the right half plane zero (RHPZ) is given in hertz by:

$$f_{RHPZ} = (V_{IN}/V_{MAIN})^2 * V_{MAIN} / (2*\pi*I_{LOAD}*L)$$

Error Amplifier Compensation

To stabilize the feedback loop dynamics the error amplifier compensation is as follows:

$$f_{POLE1} \approx 1 / (2*\pi*10^6*C3)$$

$$f_{ZERO1} = 1 / (2*\pi*R2*C3)$$

Where R2 and C3 are part of the compensation network in Figure 2. A 6.8KΩ and 10nF combination gives about 70° of phase margin and bandwidth of about 35KHz for most load conditions.

Linear Regulator Compensation

The positive or negative regulated voltages of two linear regulators are controlled by a transconductance amplifier and a P-channel or N-channel pass transistor respectively. The DC gain of either LDO is approximately 100dB with a slight dependency on load current. The output capacitor (C_{LDO}) and resistance load (R_{LOAD}) make-up the dominant pole.

$$f_{LDOPOLE1} = 1 / (2*\pi*R_{LOAD}*C_{LDO})$$

The pass transistor's internal pole is about 10Hz to 30Hz. To compensate for the two pole system and add more phase and gain margin, a lead-lag resistor capacitor network is necessary.

For the positive linear regulator:

$$f_{POSPOLE1} = 1 / (2*\pi*(R10+R7||R8)*C15)$$

$$f_{POSZERO1} = 1 / (2*\pi*(R10+R7)*C15)$$

For the negative linear regulator:

$$f_{NEGPOLE1} = 1 / 2*\pi*(R9+R3||R4)*C14)$$

$$f_{NEGZERO1} = 1 / (2*\pi*(R9+R3)*C14)$$

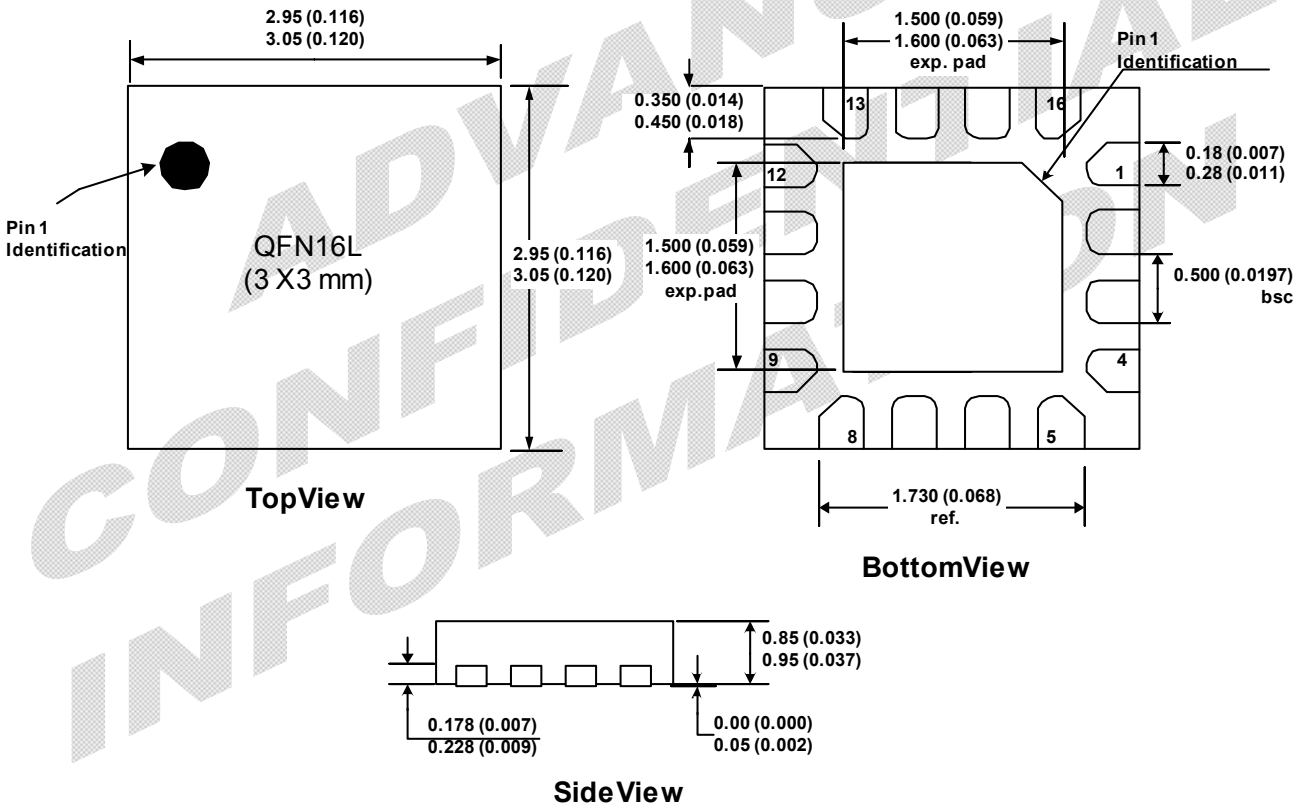
$f_{POSPOLE1}$ and $f_{NEGPOLE1}$ are necessary to cancel out the zero created by the equivalent series resistance (R_{LDOESR}) of the output capacitor.

$$f_{LDOZERO} = 1 / (2*\pi*R_{LDOESR}*C_{LDO})$$

For component values shown in Figure 2 a 10Ω and 27pF RC network gives about 45° of phase margin and a bandwidth of about 70KHz on both regulators.

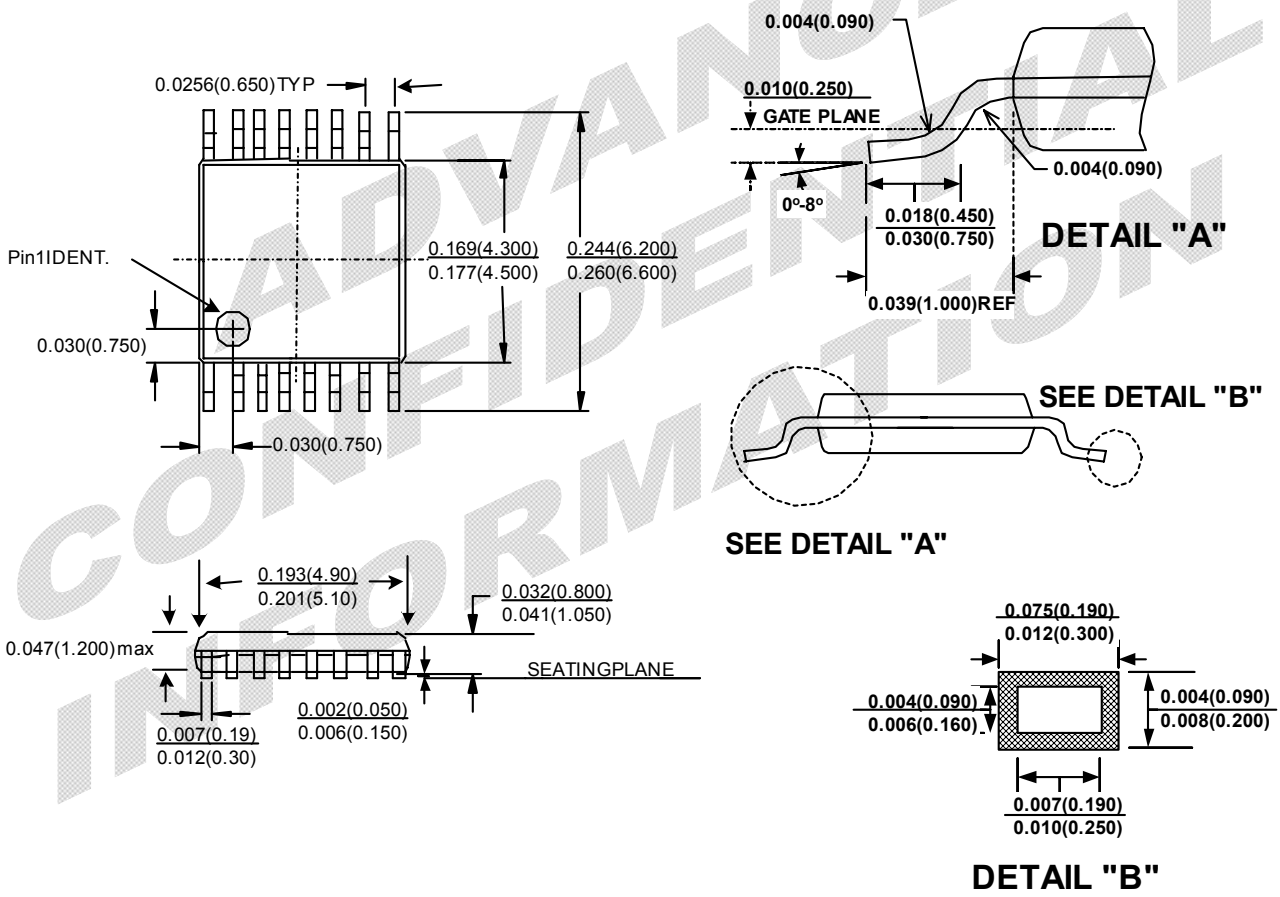
Packaging

QFN16
(3mm x 3mm)



NOTE:
1) Control dimension is in millimeters. Dimension in bracket is inch.

TSSOP16



NOTE:
1) Control dimension is in inches. Dimension in bracket is millimeters.