IA4421 Universal ISM Band FSK Transceiver

DESCRIPTION

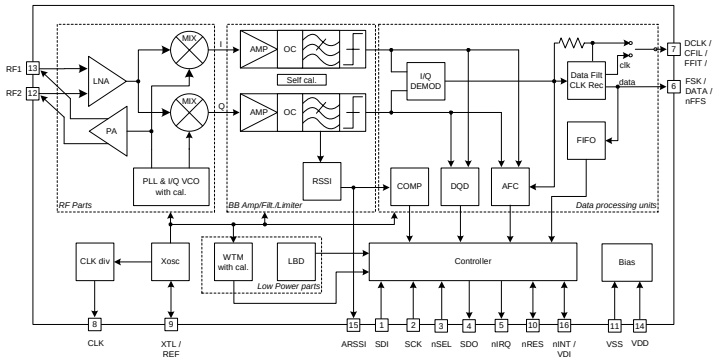
Integration's IA4421 is a single chip, low power, multi-channel FSK transceiver designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 433, 868 and 915 MHz bands. The IA4421 transceiver is a part of Integration's EZRadio™ product line, which produces a flexible, low cost, and highly integrated solution that does not require production alignments. The chip is a complete analog RF and baseband transceiver including a multi-band PLL synthesizer with PA, LNA, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation.

The IA4421 features a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency-hopping, bypassing multipath fading and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. The receiver baseband bandwidth (BW) is programmable to accommodate various deviation, data rate and crystal tolerance requirements. The transceiver employs the Zero-IF approach with I/Q demodulation. Consequently, no external components (except crystal and decoupling) are needed in most applications.

The IA4421 dramatically reduces the load on the microcontroller with the integrated digital data processing features: data filtering, clock recovery, data pattern recognition, integrated FIFO and TX data register. The automatic frequency control (AFC) feature allows the use of a low accuracy (low cost) crystal. To minimize the system cost, the IA4421 can provide a clock signal for the microcontroller, avoiding the need for two crystals.

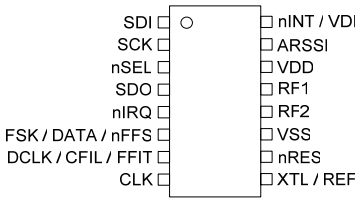
For low power applications, the IA4421 supports low duty cycle operation based on the internal wake-up timer.

FUNCTIONAL BLOCK DIAGRAM



IA4421

PIN ASSIGNMENT



See back page for ordering information.

FEATURES

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast-settling, programmable, high-resolution PLL synthesizer
- Fast frequency-hopping capability
- High bit rate (up to 115.2 kbps in digital mode and 256 kbps in analog mode)
- Direct differential antenna input/output
- Integrated power amplifier
- Programmable TX frequency deviation (15 to 240 kHz)
- Programmable RX baseband bandwidth (67 to 400 kHz)
- Analog and digital RSSI outputs
- Automatic frequency control (AFC)
- Data quality detection (DQD)
- Internal data filtering and clock recovery
- RX synchron pattern recognition
- SPI compatible serial control interface
- Clock and reset signals for microcontroller
- 16 bit RX Data FIFO
- Two 8 bit TX data registers
- Low power duty cycle mode
- Standard 10 MHz crystal reference with in circuit calibration
- Wake-up timer
- 2.2 to 3.8 V supply voltage
- Low power consumption
- Low standby current (0.3 μA)
- Compact 16 pin TSSOP package
- Supports very short packets (down to 3 bytes)
- High quality temperature stability of the RF parameters
- High quality adjacent channel rejection/blocking

TYPICAL APPLICATIONS

- Home security and alarm
- Remote control, keyless entry
- Wireless keyboard/mouse and other PC peripherals
- Toy controls
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED FEATURE-LEVEL DESCRIPTION

The IA4421 FSK transceiver is designed to cover the unlicensed frequency bands at 433, 868 and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

The receiver block employs the Zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The IA4421 incorporates a fully integrated multi-band PLL synthesizer, PA with antenna tuning, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows the usage of multiple channels in any of the bands.

RF Power Amplifier (PA)

The power amplifier has an open-collector differential output and can directly drive a loop antenna with a programmable output power level. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and the so-called "hand effect".

LNA

The LNA has approximately 250 Ohm input impedance, which functions well with the proposed antennas (see: Application Notes available from **www.integration.com**)

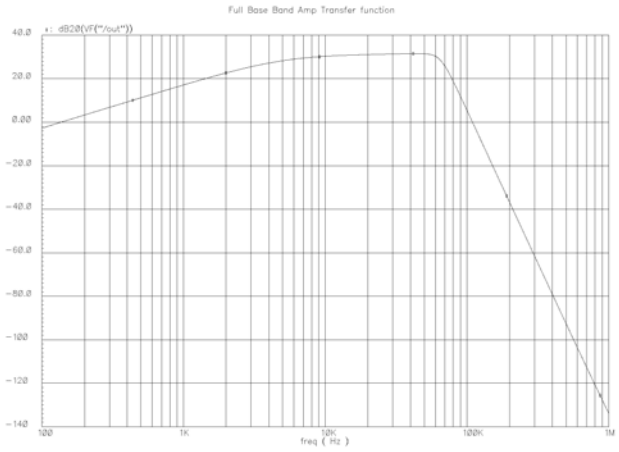
If the RF input of the chip is connected to 50 Ohm devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain can be selected in four steps (between 0 and -20dB relative to the highest gain) according to RF signal strength. It can be useful in an environment with strong interferers.

Baseband Filters

The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. This allows setting up the receiver according to the characteristics of the signal to be received.

An appropriate bandwidth can be chosen to accommodate various FSK deviation, data rate and crystal tolerance requirements. The filter structure is 7th order Butterworth low-pass with 40 dB suppression at 2*BW frequency. Offset cancellation is done by using a high-pass filter with a cut-off frequency below 7 kHz.



Data Filtering and Clock Recovery

Output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Analog operation: The filter is an RC type low-pass filter followed by a Schmitt-trigger (St). The resistor (10 kOhm) and the St are integrated on the chip. An (external) capacitor can be chosen according to the actual bit rate. In this mode, the receiver can handle up to 256 kbps data rate. The FIFO can not be used in this mode and clock is not provided for the demodulated data.

Digital operation: A digital filter is used with a clock frequency at 29 times the bit rate. In this mode there is a clock recovery circuit (CR), which can provide synchronized clock to the data. Using this clock the received data can fill a FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow mode. The CR starts in fast mode, then after locking it automatically switches to slow mode

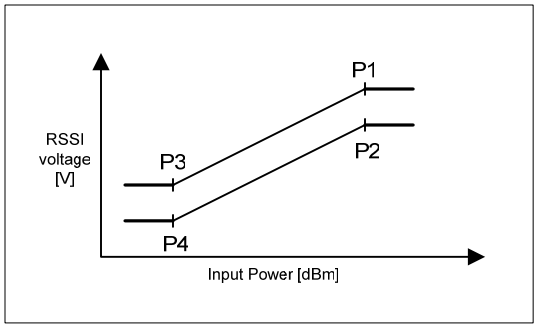
(Only the digital data filter and the clock recovery use the bit rate clock. For analog operation, there is no need for setting the correct bit rate.)

Data Validity Blocks

RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the external filter capacitor. Pin 15 is used as analog RSSI output. The digital RSSI can be monitored by reading the status register.

Analog RSSI Voltage vs. RF Input Power



P1	-65 dBm	1300 mV
P2	-65 dBm	1000 mV
P3	-100 dBm	600 mV
P4	-100 dBm	300 mV

DQD

The operation of the Data Quality Detector is based on counting the spikes on the unfiltered received data. High output signal indicates an operating FSK transmitter within baseband filter bandwidth from the local oscillator. DQD threshold parameter can be set by using the *Data Filter Command.*

AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can minimize the TX/RX offset in discrete steps, allowing the use of:

- Narrower receiver bandwidth (i.e. increased sensitivity)
- Higher data rate
- Inexpensive crystals

Crystal Oscillator

The IA4421 has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet.

The transceiver can supply a clock signal for the microcontroller; so accurate timing is possible without the need for a second crystal.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the *Configuration Setting Command,* the chip provides a fixed number (196) of further clock pulses ("clock tail") for the microcontroller to let it go to idle or sleep mode. If this clock output is not used, turn the output buffer off by the *Power Management Command.*

Low Battery Voltage Detector

The low battery detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level. The detector circuit has 50 mV hysteresis.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 uA typical) and can be programmed from 1 ms to several days with an accuracy of ±10%.

The wake-up timer calibrates itself to the crystal oscillator at every startup. For proper calibration of the wake-up timer the crystal oscillator must be running before the wake-up timer is enabled. The calibration process takes approximately 0.5ms. For the crystal start up time (tsx), see page 10.

Event Handling

In order to minimize current consumption, the transceiver supports different power saving modes. Active mode can be initiated by several wake-up events (negative logical pulse on nINT input, wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up or receiving a request through the serial interface).

If any wake-up event occurs, the wake-up logic generates an interrupt signal, which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The source of the interrupt can be read out from the transceiver by the microcontroller through the SDO pin.

Interface and Controller

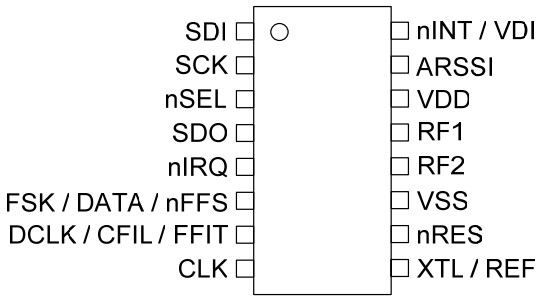
An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the transceiver and the received data.

The transmitter block is equipped with two 8 bit wide TX data registers. It is possible to write 8 bits into the register in burst mode and the internal bit rate generator transmits the bits out with the predefined rate. For further details, see the TX Register Buffered Data Transmission section.

It is also possible to store the received data bits into a FIFO register and read them out in a buffered mode.

PACKAGE PIN DEFINITIONS

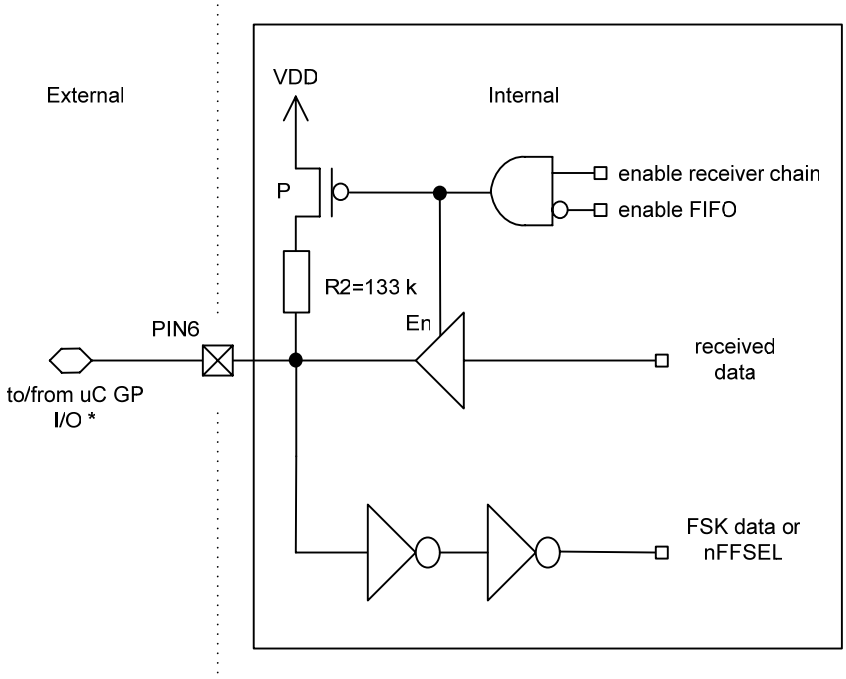
Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output



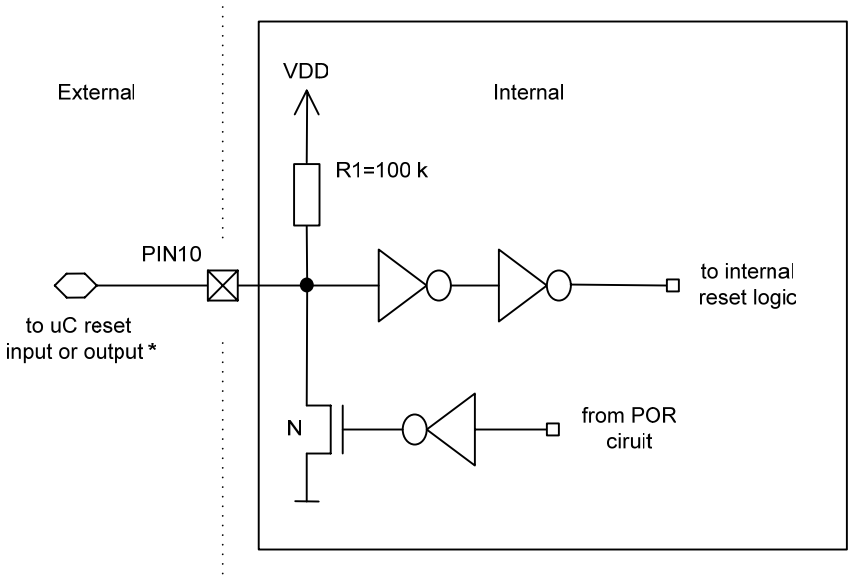
Pin	Name	Type	Function
1	SDI	DI	Data input of the serial control interface (SPI compatible)
2	SCK	DI	Clock input of the serial control interface
3	nSEL	DI	Chip select input of the serial control interface (active low)
4	SDO	DO	Serial data output with bus hold
5	nIRQ	DO	Interrupt request output (active low)
6	FSK	DI	Transmit FSK data input (internal pull up resistor 133 k)
	DATA	DO	Received data output (FIFO not used)
	nFFS	DI	FIFO select input (active low) In FIFO mode, when bit *ef* is set in *Configuration Setting Command* (internal pull up resistor 133 k)
7	DLCK	DO	Received data clock output (Digital filter used, FIFO not used)
	CFIL	AIO	External data filter capacitor connection (Analog filter used)
	FFIT	DO	FIFO interrupt (active high) Number of the bits in the RX FIFO has reached the preprogrammed limit In FIFO mode, when bit *ef* is set in *Configuration Setting Command*
8	CLK	DO	Microcontroller clock output
9	XTL	AIO	Crystal connection (the other terminal of crystal to VSS) or external reference input
	REF	AIO	External reference input. Use 33 pF series coupling capacitor
10	nRES	DIO	Open drain reset output with internal pull-up and input buffer (active low)
11	VSS	S	Ground reference voltage
12	RF2	AIO	RF differential signal input/output
13	RF1	AIO	RF differential signal input/output
14	VDD	S	Positive supply voltage
15	ARSSI	AO	Analog RSSI output
16	nINT	DI	Interrupt input (active low)
	VDI	DO	Valid data indicator output

Note: The actual mode of the multipurpose pins (pin 6 and 7) is determined by the TX/RX data I/O settings of the transceiver.

PIN6 Internal Structure (FSK / DATA / nFFS)



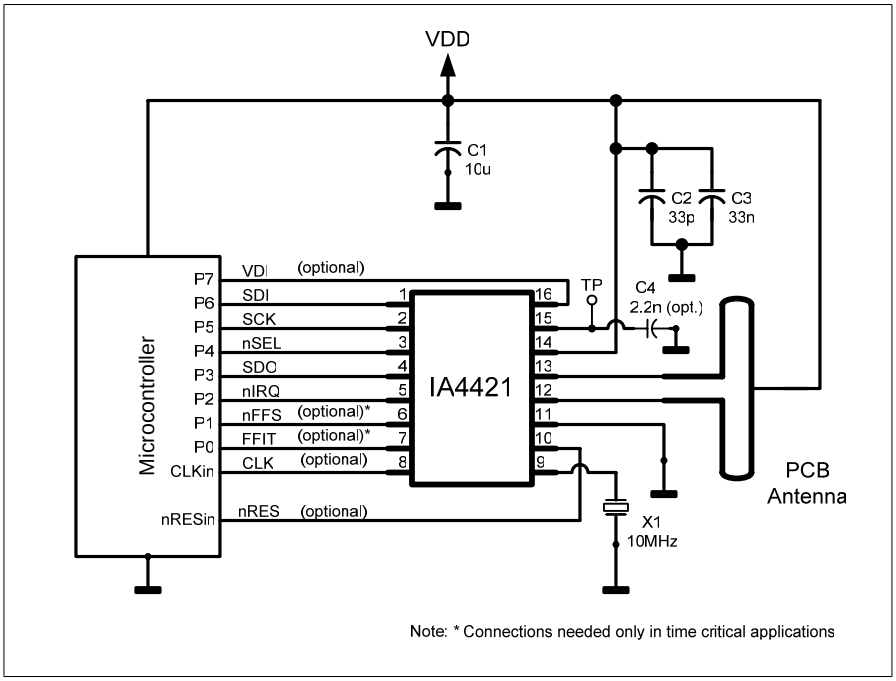
PIN10 Internal Structure (nRES I/O)



*** Note:** These pins can be left floating.

Typical Application

Typical application with FIFO usage



Mode		Pin 6	Pin 7
Transmit	el=0 in *Configuration Setting Command*	TX Data input	Not used
	el=1 in *Configuration Setting Command*	nFFS input (TX Data register can be accessed)	
Receive	ef=0 in *Configuration Setting Command*	RX Data output	RX Data clock output
	ef=1 in *Configuration Setting Command*	nFFS input (RX Data FIFO can be accessed)	FFIT output

GENERAL DEVICE SPECIFICATIONS

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6	V
V_{in}	Voltage on any pin (except RF1 and RF2)	-0.5	V_{dd}+0.5	V
V_{oc}	Voltage on open collector outputs (RF1, RF2)	-0.5	V_{dd}+1.5 (Note 1)	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	^{o}C
T_{ld}	Lead temperature (soldering, max 10 s)		260	^{o}C

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	3.8	V
V_{oc}	Voltage range on open collector outputs (RF1, RF2)	V_{dd}-1.5 (Note 2)	V_{dd}+1.5	V
T_{op}	Ambient operating temperature	-40	85	^{o}C

Note 1: Cannot be higher than 7 V.

Note 2: Cannot be lower than 1.2 V.

ELECTRICAL SPECIFICATION

Test Conditions: T_{op} = 27 °C; V_{dd} = V_{oc} = 3.3 V)

DC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
$I_{dd\_TX\_0}$	Supply current (TX mode, P_{out} = 0 dBm)	433 MHz band		15		mA
		868 MHz band		16		
		915 MHz band		17		
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, P_{out} = P_{max})	433 MHz band		22	26	mA
		868 MHz band		23	27	
		915 MHz band		24	28	
I_{dd_RX}	Supply current (RX mode)	433 MHz band		11	13	mA
		868 MHz band		12	14	
		915 MHz band		13	15	
I_{pd}	Standby current (Sleep mode)	All blocks disabled		0.3	1	µA
I_{lb}	Low battery voltage detector current consumption			0.5	1.7	µA
I_{wt}	Wake-up timer current consumption			1.5	3.5	µA
I_x	Idle current	Crystal oscillator on (Note 1)		0.6	1.2	mA
V_{lb}	Low battery detect threshold	Programmable in 0.1 V steps	2.25		3.75	V
V_{lba}	Low battery detection accuracy			+/- 3		%
V_{il}	Digital input low level voltage				0.3*V_{dd}	V
V_{ih}	Digital input high level voltage		0.7*V_{dd}			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	µA
I_{ih}	Digital input current	V_{ih} = V_{dd}, V_{dd} = 3.8 V	-1		1	µA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

Notes are on page 11.

AC Characteristics (PLL parameters)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	(Note 2)	9	10	11	MHz
f_o	Receiver LO/Transmitter carrier frequency	433 MHz band, 2.5 kHz resolution	430.24		439.75	MHz
		868 MHz band, 5.0 kHz resolution	860.48		879.51	
		915 MHz band, 7.5 kHz resolution	900.72		929.27	
t_{lock}	PLL lock time	Frequency error < 1kHz after 10 MHz step		30		us
$t_{st, P}$	PLL startup time (Note 10)	With a running crystal oscillator		200	300	us

AC Characteristics (Receiver)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
BW	Receiver bandwidth	mode 0		67		kHz
		mode 1		134		
		mode 2		200		
		mode 3		270		
		mode 4		340		
		mode 5		400		
BR_{RX}	FSK bit rate (Note 10)	With internal digital filters	0.6		115.2	kbps
BRA_{RX}	FSK bit rate (Note 10)	With analog filter			256	kbps
P_{min}	Receiver Sensitivity	BER 10^{-3}, BW=67 kHz, BR=1.2 kbps, 868 MHz Band (Note 3)		-110		dBm
AFC_{range}	AFC locking range	df_{FSK}: FSK deviation in the received signal		$0.8*df_{FSK}$		
$IIP3_{inh}$	Input IP3	In band interferers in high bands (868 MHz, 915 MHz)		-21		dBm
$IIP3_{outh}$	Input IP3	Out of band interferers $\lvert f-f_o \rvert > 4$ MHz		-18		dBm
$IIP3_{inl}$	IIP3 (LNA –6 dB gain)	In band interferers in low band (433 MHz)		-15		dBm
$IIP3_{outl}$	IIP3 (LNA –6 dB gain)	Out of band interferers $\lvert f-f_o \rvert > 4$ MHz		-12		dBm
P_{max}	Maximum input power	LNA: high gain	0			dBm
Cin	RF input capacitance			1		pF
RS_a	RSSI accuracy			+/- 6		dB
RS_r	RSSI range			46		dB
RS_{ps}	RSSI power supply dependency	When input signal level lower than -54 dBm and greater than -100 dBm		+35		mV/V
C_{ARSSI}	Filter capacitor for ARSSI		1			nF
RS_{step}	RSSI programmable level steps			6		dB
RS_{resp}	DRSSI response time	Until the RSSI signal goes high after the input signal exceeds the preprogrammed limit C_{ARRSI} = 4.7 nF		500		us
P_{sp_rx}	Receiver spurious emission				-60	dBm

Notes are on page 11.

AC Characteristics (Transmitter)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
I_{OUT}	Open collector output DC current	Programmable	0.5		6	mA
P_{max_50}	Max. output power delivered to 50 Ohm load over a suitable matching network (Note 4)	In 433 MHz band		7		dBm
		In 868 MHz / 915 MHz bands		5		
P_{max_ant}	Max. EIRP with suitable selected PCB antenna. (Note 6)	In 433 MHz band with monopole antenna with matching network (Note 4)		7		dBm
		In 868 MHz / 915 MHz bands (Note 5)		7		
P_{out}	Typical output power	Selectable in 3 dB steps (Note 7)	P_{max}-21		P_{max}	dBm
P_{sp}	Spurious emission $\lvert f-f_{sp} \rvert > 1$ MHz	At max power 50 Ohm load (Note 4)			-55	dBc
		With PCB antenna (Note 5)			-60	dBc
P_{harm}	Harmonic suppression	At max power 50 Ohm load (Note 4)			-35	dBc
		With PCB antenna (Note 5)			-42	dBc
C_o	Output capacitance (set by the automatic antenna tuning circuit)	In 433 MHz band	2	2.6	3.2	pF
		In 868 MHz / 915 MHz bands	2.1	2.7	3.3	
Q_o	Quality factor of the output capacitance	In 433 MHz band	13	15	17	
		In 868 MHz / 915 MHz bands	8	10	12	
L_{out}	Output phase noise	100 kHz from carrier, in 868 MHz band		-80		dBc/Hz
		1 MHz from carrier, in 868 MHz band		-103		
BR_{TX}	FSK bit rate	Via internal TX data register			172	kbps
BRA_{TX}	FSK bit rate	TX data connected to the FSK input			256	kbps
df_{fsk}	FSK frequency deviation	Programmable in 15 kHz steps	15		240	kHz

AC Characteristics (Turn-on/Turnaround timings)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
t_{sx}	Crystal oscillator startup time	Default capacitance bank setting, crystal ESR < 50 Ohm (Note 9). Crystal load capacitance = 16 PF.		2	7	ms
$T_{tx\_XTAL\_ON}$	Transmitter turn-on time	Synthesizer off, crystal oscillator on with 10 MHz step		250		us
$T_{rx\_XTAL\_ON}$	Receiver turn-on time	Synthesizer off, crystal oscillator on with 10 MHz step		250		us
$T_{tx\_rx\_SYNT\_ON}$	Transmitter – Receiver turnover time	Synthesizer and crystal oscillator on during TX/RX change with 10 MHz step		150		us
$T_{rx\_tx\_SYNT\_ON}$	Receiver – Transmitter turnover time	Synthesizer and crystal oscillator on during RX/TX change with 10 MHz step		150		us

AC Characteristics (Others)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
C_{xl}	Crystal load capacitance, see crystal selection guide	Programmable in 0.5 pF steps, tolerance +/- 10%	8.5		16	pF
t_{POR}	Internal POR timeout	After V_{dd} has reached 90% of final value (Note 8)			50	ms
t_{PBt}	Wake-up timer clock accuracy	Crystal oscillator must be enabled to ensure proper calibration at the start up. (Note 9)		+/- 10		%
$C_{in,\ D}$	Digital input capacitance				2	pF
$t_{r,\ f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Notes are on page 11.

AC Characteristics (continued)

Note 1: Measured with disabled clock output buffer.

Note 2: Not using a 10 MHz crystal is allowed but not recommended because all crystal referred timing and frequency parameters will change accordingly.

Note 3: See the BER diagrams in the measurement results section for detailed information.

Note 4: See reference design with *50 Ohm Matching Network* for details.

Note 5: See reference design with *Resonant PCB Antenna (BIFA)* for details.

Note 6: Optimal antenna admittance/impedance:

IA4421	Yantenna [mS]	Zantenna [Ohm]	Lantenna [nH]
433 MHz	2 – j5.9	52 + j152	62
868 MHz	1.2 - j11.9	7.8 + j83	15.4
915 MHz	1.49 - j12.8	9 + j77	13.6

Note 7: Adjustable in 8 steps.

Note 8: During this period, commands are not accepted by the chip.

Note 9: The crystal oscillator start up time strongly depends on the capacitance seen by the oscillator. Low capacitance and low ESR crystal is recommended with low parasitic PCB layout design.

Note 10: By design.

CONTROL INTERFACE

Commands to the transmitter are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control and command registers.

The receiver will generate an interrupt request (IT) for the microcontroller - by pulling the nIRQ pin low - on the following events:

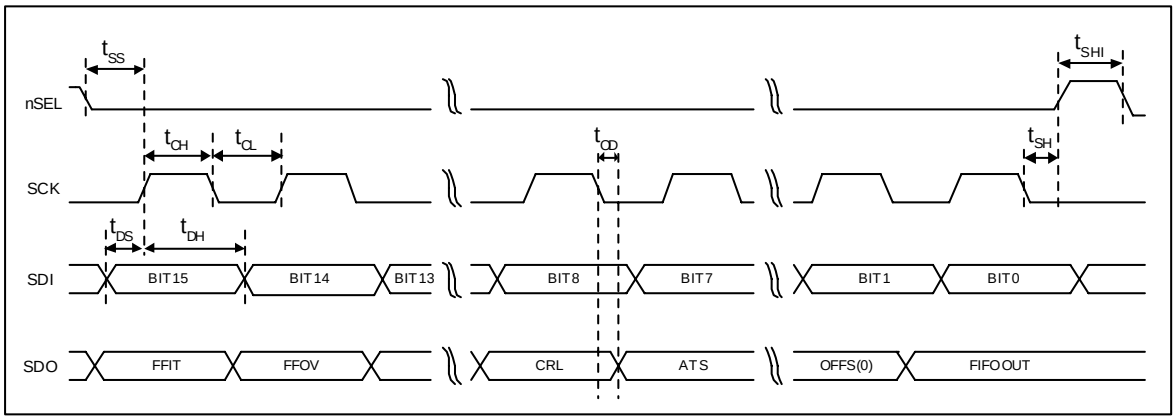
- The TX register is ready to receive the next byte (RGIT)
- The FIFO has received the preprogrammed amount of bits (FFIT)
- Power-on reset (POR)
- FIFO overflow (FFOV) / TX register underrun (RGUR)
- Wake-up timer timeout (WKUP)
- Negative pulse on the interrupt input pin nINT (EXT)
- Supply voltage below the preprogrammed value is detected (LBD)

FFIT and FFOV are applicable when the FIFO is enabled. RGIT and RGUR are applicable only when the TX register is enabled. To identify the source of the IT, the status bits should be read out.

Timing Specification

Symbol	Parameter	Minimum value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram



Control Commands

	Control Command	Related Parameters/Functions	Related control bits
1	Configuration Setting Command	Frequency band, crystal oscillator load capacitance, RX FIFO and TX register enable	el, ef, b1 to b0, x3 to x0
2	Power Management Command	Receiver/Transmitter mode change, synthesizer, crystal oscillator, PA, wake-up timer, clock output enable	er, ebb, et, es, ex, eb, ew, dc
3	Frequency Setting Command	Frequency of the local oscillator/carrier signal	f11 to f0
4	Data Rate Command	Bit rate	cs, r6 to r0
5	Receiver Control Command	Function of pin 16, Valid Data Indicator, baseband bandwidth, LNA gain, digital RSSI threshold	p16, d1 to d0, i2 to i0, g1 to g0, r2 to r0
6	Data Filter Command	Data filter type, clock recovery parameters	al, ml, s, f2 to f0
7	FIFO and Reset Mode Command	Data FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable, POR sensitivity	f3 to f0, sp, ff, al, dr
8	Synchron Pattern Command	Synchron pattern	b7 to b0
9	Receiver FIFO Read Command	RX FIFO read	
10	AFC Command	AFC parameters	a1 to a0, rl1 to rl0, st, fi, oe, en
11	TX Configuration Control Command	Modulation parameters, output power	mp, m3 to m0, p2 to p0
12	PLL Setting Command	CLK out buffer speed, low power mode of the crystal oscillator, dithering, PLL bandwidth	ob1 to ob0, ddit, ddy, bw0
13	Transmitter Register Write Command	TX data register write	t7 to t0
14	Wake-Up Timer Command	Wake-up time period	r4 to r0, m7 to m0
15	Low Duty-Cycle Command	Enable and set low duty-cycle mode	d6 to d0, en
16	Low Battery Detector and Microcontroller Clock Divider Command	LBD voltage and microcontroller clock division ratio	d2 to d0, v3 to v0
17	Status Read Command	Status bit readout	

In general, setting the given bit to one will activate the related function. In the following tables, the POR column shows the default values of the command registers after power-on.

Description of the Control Commands

1. Configuration Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	0	0	el	ef	b1	b0	x3	x2	x1	x0	8008h

Bit *el* enables the internal data register.
Bit *ef* enables the FIFO mode. If *ef*=0 then DATA (pin 6) and DCLK (pin 7) are used for data and data clock output.

b1	b0	Frequency Band [MHz]
0	0	Reserved
0	1	433
1	0	868
1	1	915

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
…				
1	1	1	0	15.5
1	1	1	1	16.0

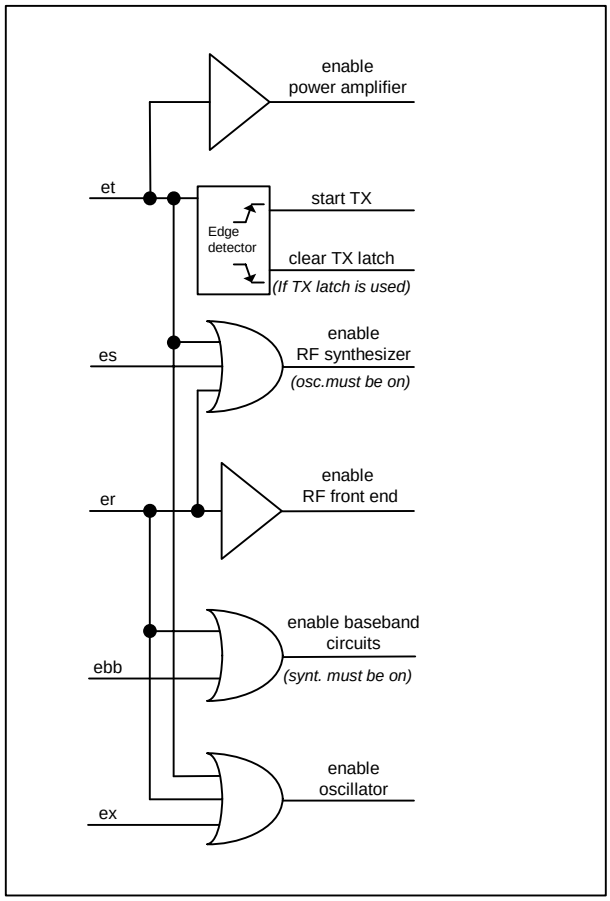
2. Power Management Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	1	0	er	ebb	et	es	ex	eb	ew	dc	8208h

Bit	Function of the control bit	Related blocks
er	Enables the whole receiver chain	RF front end, baseband, synthesizer, oscillator
ebb	The receiver baseband circuit can be separately switched on	Baseband
et	Switches on the PLL, the power amplifier, and starts the transmission (If TX register is enabled)	Power amplifier, synthesizer, oscillator
es	Turns on the synthesizer	Synthesizer
ex	Turns on the crystal oscillator	Crystal oscillator
eb	Enables the low battery detector	Low battery detector
ew	Enables the wake-up timer	Wake-up timer
dc	Disables the clock output (pin 8)	Clock output buffer

The ebb, es, and ex bits are provided to optimize the TX to RX or RX to TX turnaround time.

Logic connections between power control bits:



Note:

- If both *et* and *er* bits are set the chip goes to receive mode.
- FSK / nFFSEL input are equipped with internal pull-up resistor. To achieve minimum current consumption do not pull this input to logic low in sleep mode.

3. Frequency Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

The 12-bit parameter F (bits *f11* to *f0*) should be in the range of 96 and 3903. When F value sent is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as:

$f_0 = 10 * C1 * (C2 + F/4000)$ [MHz]

The constants C1 and C2 are determined by the selected band as:

Band [MHz]	C1	C2
433	1	43
868	2	43
915	3	30

4. Data Rate Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	cs	r6	r5	r4	r3	r2	r1	r0	C623h

The actual bit rate in transmit mode and the expected bit rate of the received data stream in receive mode is determined by the 7-bit parameter R (bits *r6* to *r0*) and bit *cs*.

BR = 10000 / 29 / (R+1) / (1+*cs**7) [kbps]

In the receiver set R according to the next function:

R= (10000 / 29 / (1+*cs**7) / BR) – 1, where BR is the expected bit rate in kbps.

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error.

Data rate accuracy requirements:

Clock recovery in slow mode: $\Delta BR/BR < 1/(29*N_{bit})$ Clock recovery in fast mode: $\Delta BR/BR < 3/(29*N_{bit})$

BR is the bit rate set in the receiver and ΔBR is the bit rate difference between the transmitter and the receiver. N_{bit} is the maximum number of consecutive ones or zeros in the data stream. It is recommended for long data packets to include enough 1/0 and 0/1 transitions, and to be careful to use the same division ratio in the receiver and in the transmitter.

5. Receiver Control Command

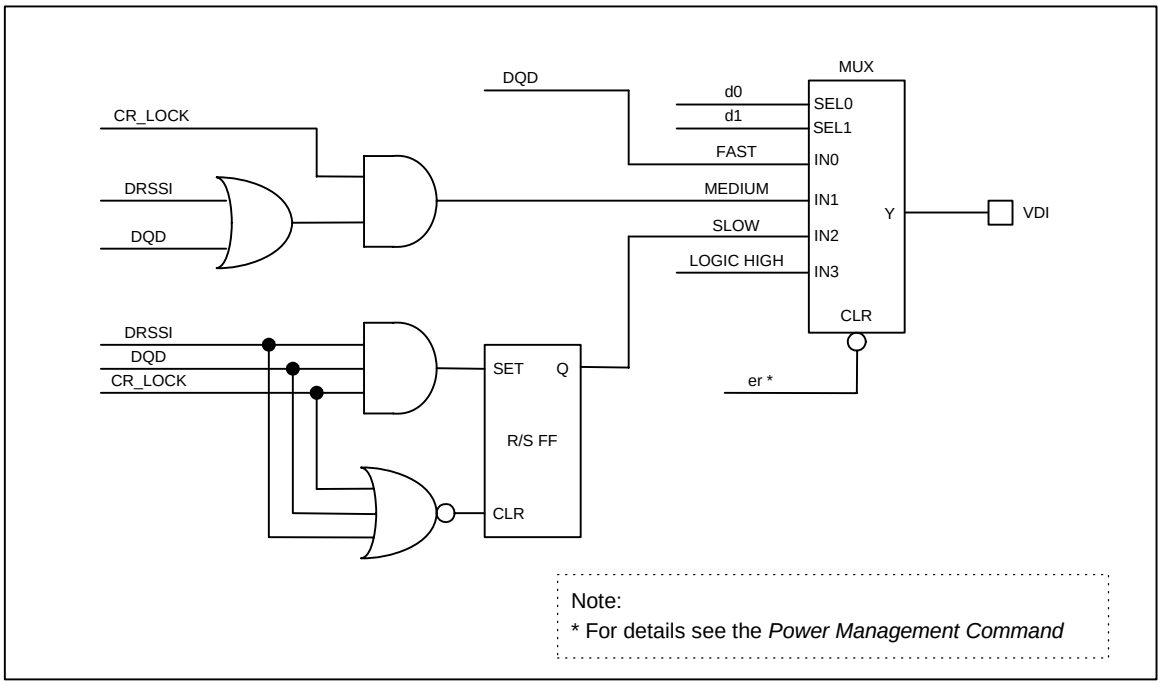
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	0	p16	d1	d0	i2	i1	i0	g1	g0	r2	r1	r0	9080h

Bit 10 *(p16)*: pin16 function select

p16	Function of pin 16
0	Interrupt input
1	VDI output

Bits 9-8 *(d1 to d0)*: VDI (valid data indicator) signal response time setting:

d1	d0	Response
0	0	Fast
0	1	Medium
1	0	Slow
1	1	Always on



Bits 7-5 *(i2 to i0)*: Receiver baseband bandwidth (BW) select:

i2	i1	i0	BW [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved

Bits 4-3 *(g1 to g0)*: LNA gain select:

g1	g0	relative to maximum [dB]
0	0	0
0	1	-6
1	0	-14
1	1	-20

Bits 2-0 *(r2 to r0)*: RSSI detector threshold:

r2	r1	r0	$RSSI_{setth}$ [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	Reserved
1	1	1	Reserved

The RSSI threshold depends on the LNA gain, the real RSSI threshold can be calculated:

$$RSSI_{th}=RSSI_{setth}+G_{LNA}$$

6. Data Filter Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	al	ml	1	s	1	f2	f1	f0	C22Ch

Bit 7 (*al*): Clock recovery (CR) auto lock control, if set.

CR will start in fast mode, then after locking it will automatically switch to slow mode.

Bit 6 (*ml*): Clock recovery lock control

1: fast mode, fast attack and fast release (4 to 8 bit preamble (1010...) is recommended)

0: slow mode, slow attack and slow release (12 to 16 bit preamble is recommended)

Using the slow mode requires more accurate bit timing (see *Data Rate Command*).

Bits 4 (s): Select the type of the data filter:

s	Filter Type
0	Digital filter
1	Analog RC filter

Digital: This is a digital realization of an analog RC filter followed by a comparator with hysteresis. The time constant is automatically adjusted to the bit rate defined by the *Data Rate Command*.

Note: Bit rate can not exceed 115 kpbs in this mode.

Analog RC filter: The demodulator output is fed to pin 7 over a 10 kOhm resistor. The filter cut-off frequency is set by the external capacitor connected to this pin and VSS.

The table shows the optimal filter capacitor values for different data rates

1.2 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115.2 kbps	256 kbps
12 nF	8.2 nF	6.8 nF	3.3 nF	1.5 nF	680 pF	270 pF	150 pF	100 pF

Note: If analog RC filter is selected the internal clock recovery circuit and the FIFO can not be used.

Bits 2-0 (*f2* to *f0*): DQD threshold parameter.

Note: To let the DQD report "good signal quality" the threshold parameter should be 4 in cases where the bitrate is close to the deviation. At higher deviation/bitrate settings, a higher threshold parameter can report "good signal quality" as well.

7. FIFO and Reset Mode Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	1	0	f3	f2	f1	f0	sp	al	ff	dr	CA80h

Bits 7-4 (*f3* to *f0*): FIFO IT level. The FIFO generates IT when the number of received data bits reaches this level.

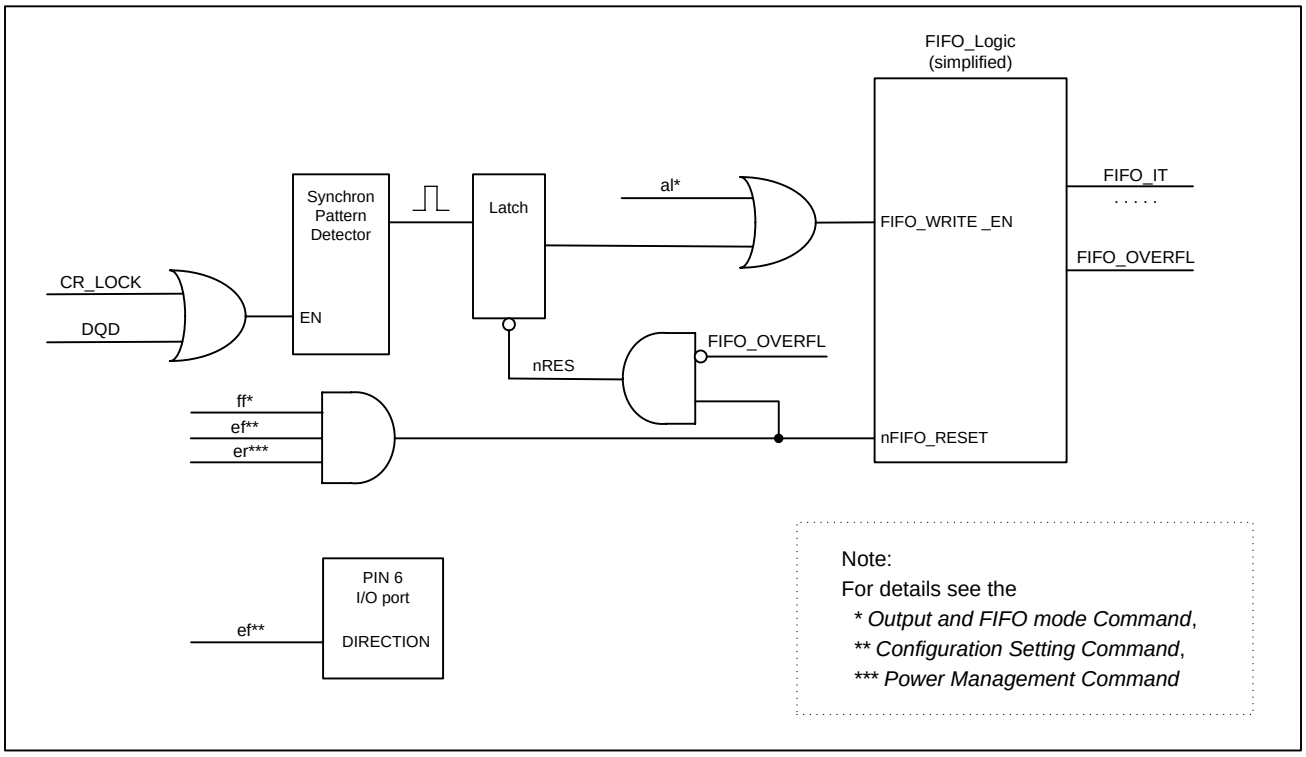
Bit 3 (*sp*): Select the length of the synchron pattern:

sp	Byte1	Byte0 (POR)	Synchron Pattern (Byte1+Byte0)
0	2Dh	D4h	2DD4h
1	Not used	D4h	D4h

Note: Byte0 can be programmed by the *Synchron Pattern Command*.

Bit 2 (*al*): Set the input of the FIFO fill start condition:

al	
0	Synchron pattern
1	Always fill



Bit 1 (*ff*): FIFO fill will be enabled after synchron pattern reception. The FIFO fill stops when this bit is cleared.

Bit 0 (*dr*): Disables the highly sensitive RESET mode.

Reset mode	Reset triggered when
Sensitive reset dr=0	Vdd below 1.5V Vdd glitch greater than 500mV
Non-sensitive reset dr=1	Vdd below 0.25V

Note: To restart the synchron pattern recognition, bit 1 should be cleared and set.

8. Synchron Pattern Command

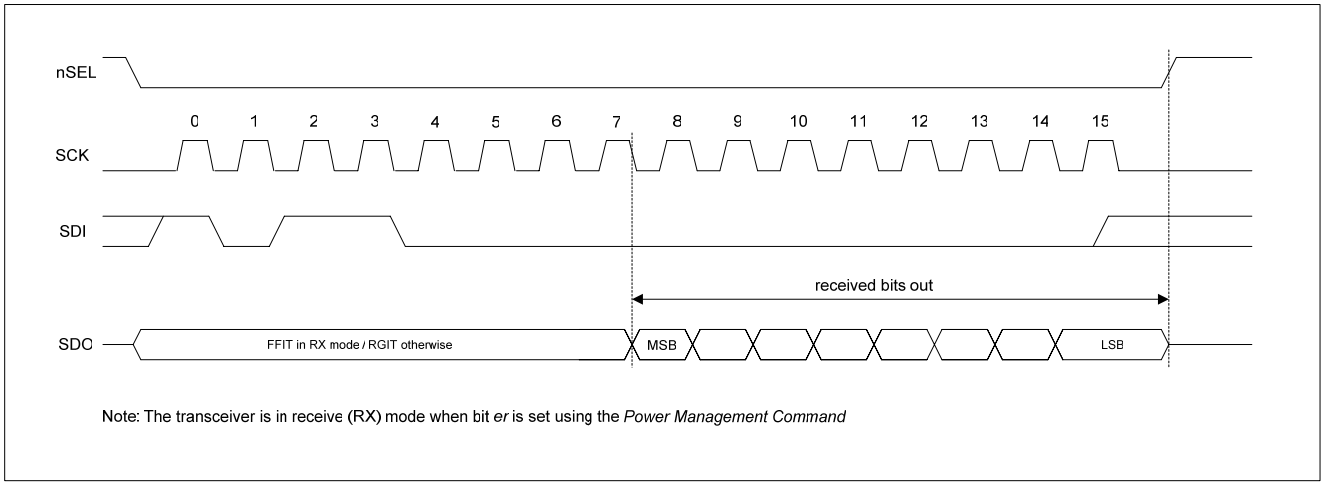
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	b7	b6	b5	b4	b3	b2	b1	b0	CED4h

The Byte0 used for synchron pattern detection can be reprogrammed by B <b7:b0>.

9. Receiver FIFO Read Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	B000h

With this command, the controller can read 8 bits from the receiver FIFO. Bit 6 *(ef)* must be set in *Configuration Setting Command.*



Note:: During FIFO access f_{SCK} cannot be higher than $f_{ref}/4$, where f_{ref} is the crystal oscillator frequency. When the duty-cycle of the clock signal is not 50 % the shorter period of the clock pulse width should be at least $2/f_{ref}$.

10. AFC Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	a1	a0	rl1	rl0	st	fi	oe	en	C4F7h

Bit 7-6 (*a1 to a0*): Automatic operation mode selector:

a1	a0	
0	0	Auto mode off (Strobe is controlled by microcontroller)
0	1	Runs only once after each power-up
1	0	Keep the f_{offset} only during receiving (VDI=high)
1	1	Keep the f_{offset} value independently from the state of the VDI signal

Bit 5-4 *(rl1 to rl0)*: Range limit. Limits the value of the frequency offset register to the next values:

rl1	rl0	Max deviation
0	0	No restriction
0	1	+15 f_{res} to -16 f_{res}
1	0	+7 f_{res} to -8 f_{res}
1	1	+3 f_{res} to -4 f_{res}

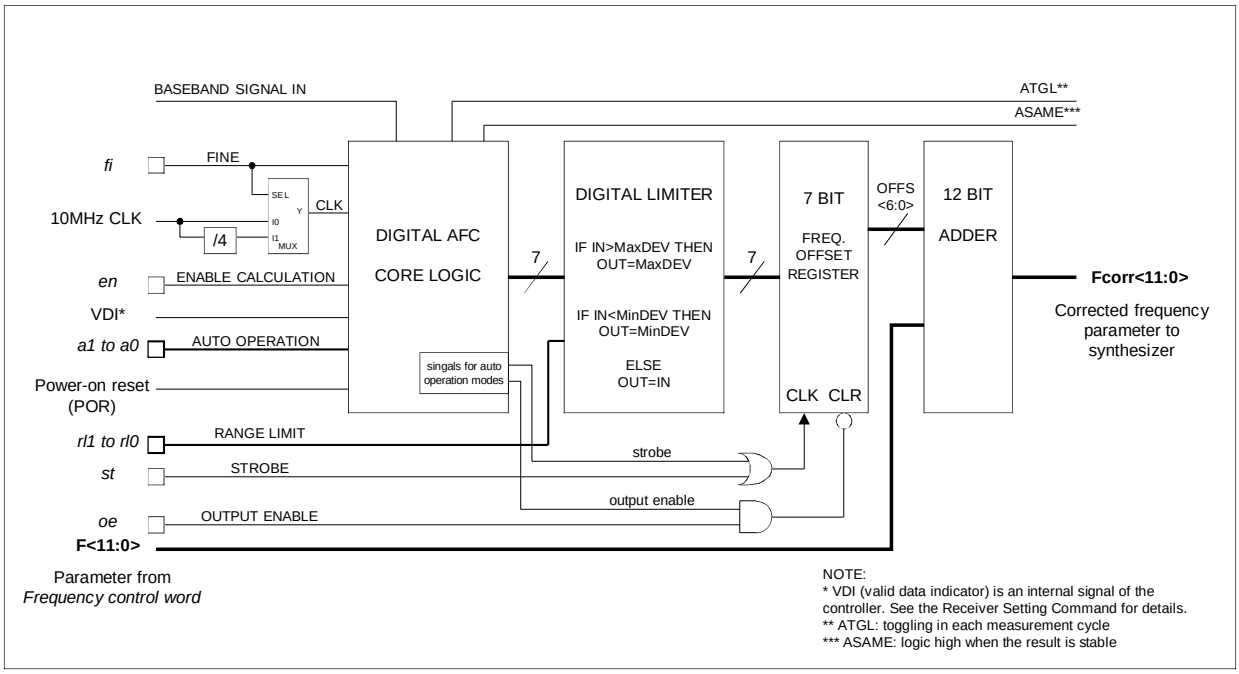
f_{res}:
433 MHz bands: 2.5 kHz
868 MHz band: 5 kHz
915 MHz band: 7.5 kHz

Bit 3 *(st)*: Strobe edge, when *st* goes to high, the actual latest calculated frequency error is stored into the offset register of the AFC block.

Bit 2 (*fi*): Switches the circuit to high accuracy (fine) mode. In this case, the processing time is about twice as long, but the measurement uncertainty is about half.

Bit 1 (*oe*): Enables the frequency offset register. It allows the addition of the offset register to the frequency control word of the PLL.

Bit 0 (*en*): Enables the calculation of the offset frequency by the AFC circuit.



Note: *Lock* bit is high when the AFC loop is locked, *f_same* bit indicates when two subsequent measuring results are the same, *toggle* bit changes state in every measurement cycle.

In manual mode, the strobe signal is provided by the microcontroller. One measurement cycle (and strobe) signal can compensate about 50-60% of the actual frequency offset. Two measurement cycles can compensate 80%, and three measurement cycles can compensate 92%. The ATGL bit in the status register can be used to determine when the actual measurement cycle is finished.

In automatic operation mode (no strobe signal is needed from the microcontroller to update the output offset register) the AFC circuit is automatically enabled when the VDI indicates potential incoming signal during the whole measurement cycle and the circuit measures the same result in two subsequent cycles.

There are three operation modes, examples from the possible application:

1, (*a1*=0, *a0*=1) The circuit measures the frequency offset only once after power up. This way, extended TX-RX maximum distance can be achieved.

Possible application:

In the final application, when the user inserts the battery, the circuit measures and compensates for the frequency offset caused by the crystal tolerances. This method allows for the use of a cheaper quartz in the application and provides protection against tracking an interferer.

2a, (*a1*=1, *a0*=0) The circuit automatically measures the frequency offset during an initial effective low data rate pattern –easier to receive- (i.e.: 00110011) of the package and changes the receiving frequency accordingly. The further part of the package can be received by the corrected frequency settings.

2b, (*a1*=1, *a0*=0) The transmitter must transmit the first part of the packet with a step higher deviation and later there is a possibility of reducing it.

In both cases (2a and 2b), when the VDI indicates poor receiving conditions (VDI goes low), the output register is automatically cleared. Use these settings when receiving signals from different transmitters transmitting in the same nominal frequencies.

3, (*a1*=1, *a0*=1) It's the same as 2a and 2b modes, but suggested to use when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is kept independently of the state of the VDI signal.

11. TX Configuration Control Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	1	0	0	mp	m3	m2	m1	m0	0	p2	p1	p0	9800h

Bits 8-4 *(mp, m3 to m0)*: FSK modulation parameters:

The resulting output frequency can be calculated as:

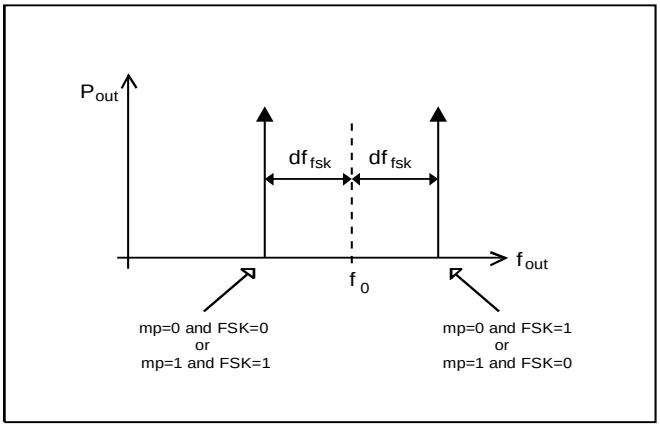
$$f_{out} = f_0 + (-1)^{SIGN} * (M + 1) * (15\ kHz)$$

where:

f_0 is the channel center frequency (see the *Frequency Setting Command*)
M is the four bit binary number <*m3 : m0*>
SIGN = (*mp*) XOR FSK

Bits 2-0 *(p2 to p0)*: Output power:

p2	p1	p0	Relative Output Power [dB]
0	0	0	0
0	0	1	-2.5
0	1	0	-5
0	1	1	-7.5
1	0	0	-10
1	0	1	-12.5
1	1	0	-15
1	1	1	-17.5



Note:

- FSK represents the value of the actual data bit.
- The output power given in the table is relative to the maximum available power, which depends on the actual antenna impedance. (See: Antenna Application Note: IA ISM-AN1)

12. PLL Setting Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	0	ob1	ob0	1	ddy	ddit	1	bw0	CC67h

Note: POR default setting of the register carefully selected to cover almost all typical applications.

Bit 6-5 (ob1-ob0): Microcontroller output clock buffer rise and fall time control.

ob1	ob0	Selected uC CLK frequency
0	0	5 or 10 MHz (recommended)
0	1	3.3 MHz
1	X	2.5 MHz or less

Note: Needed for optimization of the RF performance. Optimal settings can vary according to the external load capacitance.

(Typ conditions: T_{op} = 27 °C; V_{dd} = V_{oc} = 2.7 V, Crystal ESR = 30 Ohm)

Bit 3 (ddy): Switches on the delay in the phase detector when this bit is set.

Bit 2 (*ddit*): When set, disables the dithering in the PLL loop.

Bit 0 (*bw0*): PLL bandwidth can be set for optimal TX RF performance.

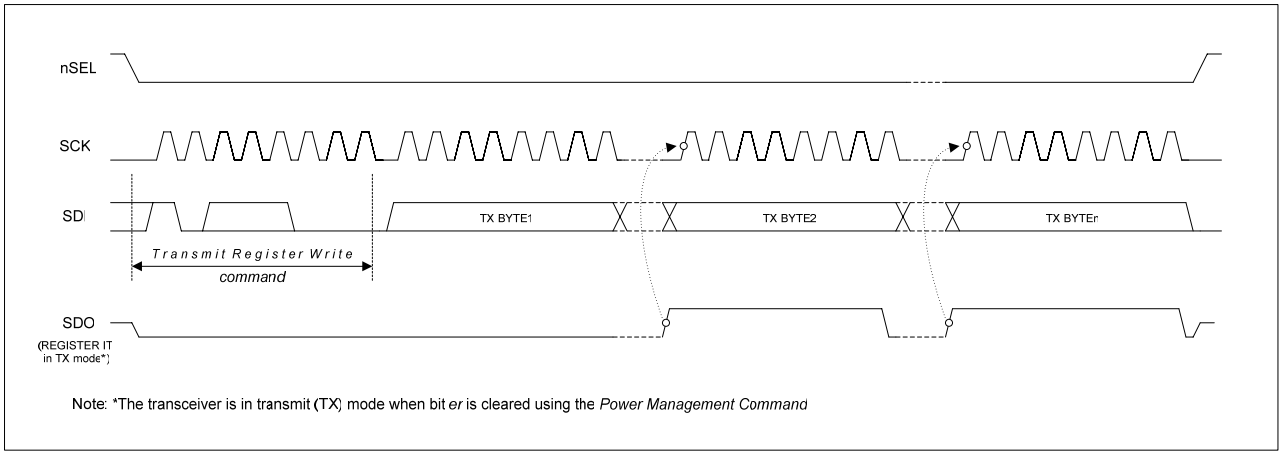
bw0	Max bit rate [kbps]	Phase noise at 1MHz offset [dBc/Hz]
0	86.2	-107
1	256	-102

13. Transmitter Register Write Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	1	0	0	0	t7	t6	t5	t4	t3	t2	t1	t0	B8AAh

With this command, the controller can write 8 bits *(t7 to t0)* to the transmitter data register. Bit 7 *(el)* must be set in *Configuration Setting Command.*

Multiple Byte Write with Transmit Register Write Command:



Note: Alternately the transmit register can be directly accessed by nFFSEL (pin6).

14. Wake-Up Timer Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up time period can be calculated by (*m7 to m0*) and (*r4 to r0*):

$T_{wake\text{-}up} = 1.03 * M * 2^R + 0.5$ [ms]

Note:

- For continual operation the *ew* bit should be cleared and set at the end of every cycle.
- For future compatibility, use R in a range of 0 and 29.

15. Low Duty-Cycle Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	d6	d5	d4	d3	d2	d1	d0	en	C80Eh

With this command, Low Duty-Cycle operation can be set in order to decrease the average power consumption in receiver mode.

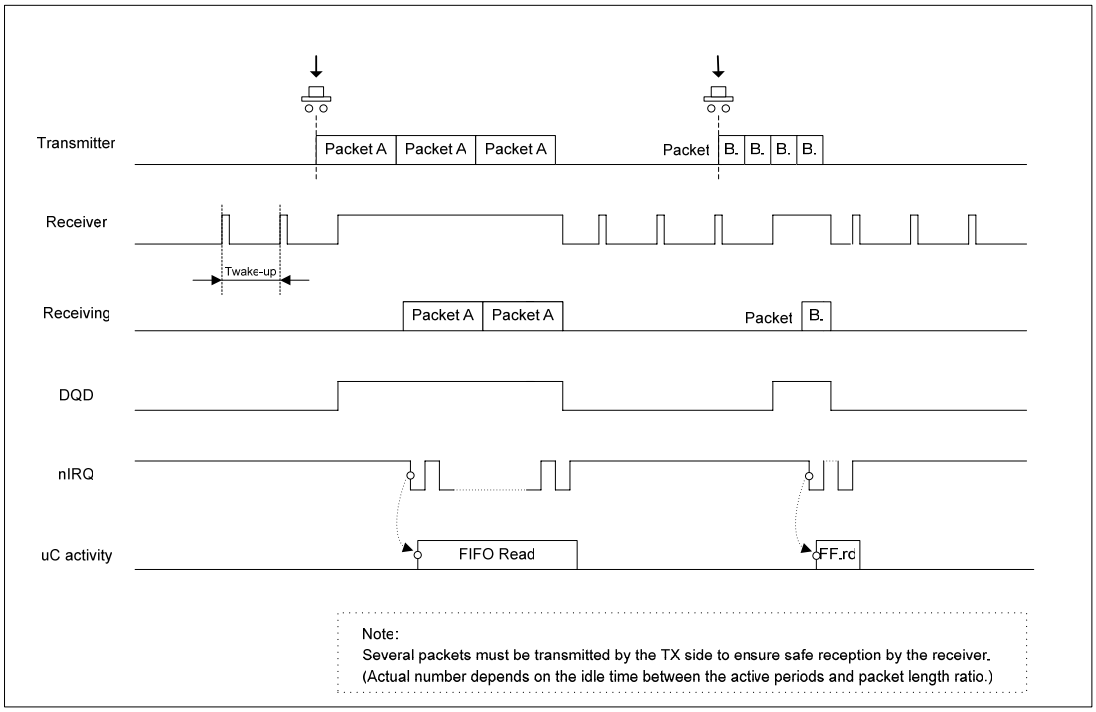
The time cycle is determined by the *Wake-Up Timer Command*.

The Duty-Cycle can be calculated by using (*d6* to *d0*) and M. (M is parameter in a *Wake-Up Timer Command*.)

Duty-Cycle= (D * 2 +1) / M *100%

The on-cycle is automatically extended while DQD indicates good received signal condition (FSK transmission is detected in the frequency range determined by *Frequency Setting Command* plus and minus the baseband filter bandwidth determined by the *Receiver Control Command*).

Application Proposal For LPDM (Low Power Duty-Cycle Mode) Receivers:



Bit 0 *(en)*: Enables the Low Duty-Cycle Mode. Wake-up timer interrupt is not generated in this mode.

Note: In this operation mode, bit *er* must be cleared and bit *ew* must be set in the *Power Management Command.*

16. Low Battery Detector and Microcontroller Clock Divider Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d2	d1	d0	0	v3	v2	v1	v0	C000h

The 4 bit parameter *(v3 to v0)* represents the value V, which defines the threshold voltage V_{lb} of the detector:

V_{lb} = 2.25 + V * 0.1 [V]

Clock divider configuration:

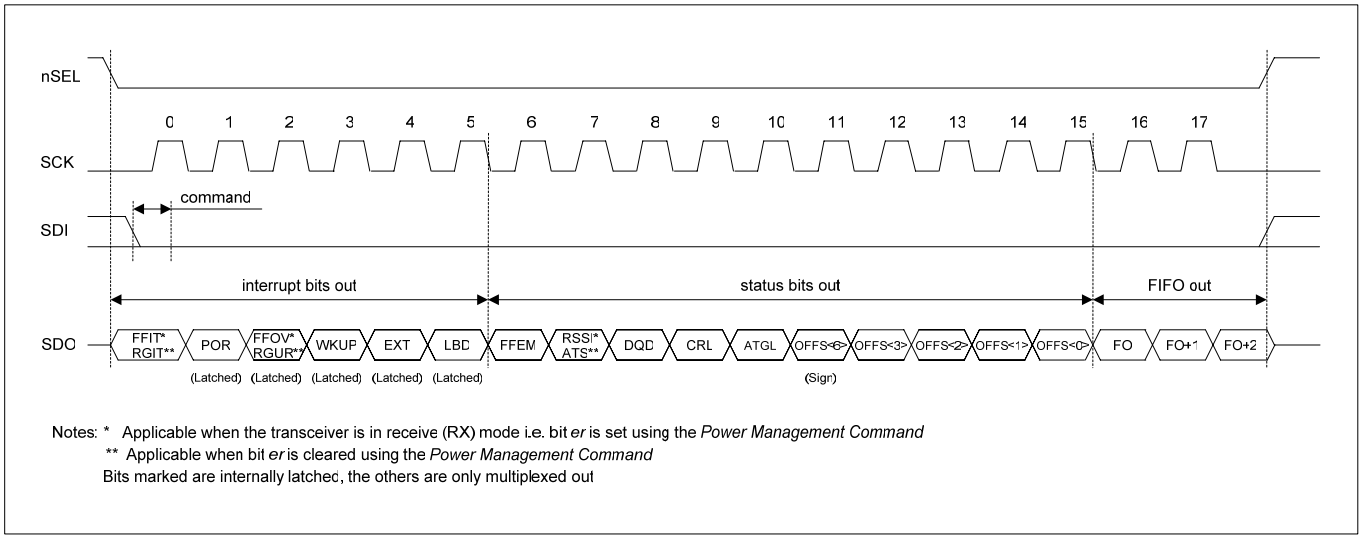
d2	d1	d0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

The low battery detector and the clock output can be enabled or disabled by bits *eb* and *dc,* respectively, using the *Power Management Command.*

17. Status Read Command

The read command starts with a zero, whereas all other control commands start with a one. If a read command is identified, the status bits will be clocked out on the SDO pin as follows:

Status Register Read Sequence with FIFO Read Example:



Notes: * Applicable when the transceiver is in receive (RX) mode i.e. bit *er* is set using the *Power Management Command*
** Applicable when bit *er* is cleared using the *Power Management Command*
Bits marked are internally latched, the others are only multiplexed out

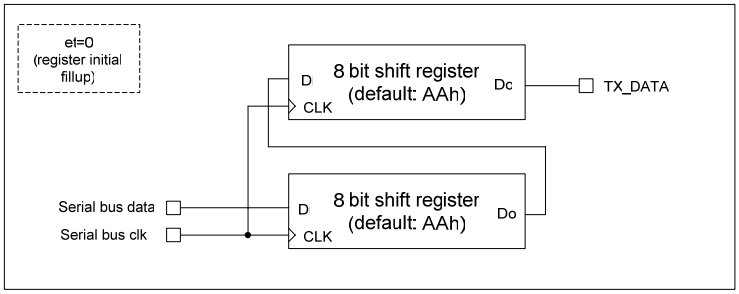
RGIT	TX register is ready to receive the next byte (Can be cleared by *Transmitter Register Write Command*)
FFIT	The number of data bits in the RX FIFO has reached the pre-programmed limit (Can be cleared by any of the FIFO read methods)
POR	Power-on reset (Cleared after *Status Read Command*)
RGUR	TX register under run, register over write (Cleared after *Status Read Command*)
FFOV	RX FIFO overflow (Cleared after *Status Read Command*)
WKUP	Wake-up timer overflow (Cleared after *Status Read Command*)
EXT	Logic level on interrupt pin (pin 16) changed to low (Cleared after *Status Read Command*)
LBD	Low battery detect, the power supply voltage is below the pre-programmed limit
FFEM	FIFO is empty
ATS	Antenna tuning circuit detected strong enough RF signal
RSSI	The strength of the incoming signal is above the pre-programmed limit
DQD	Data quality detector output
CRL	Clock recovery locked
ATGL	Toggling in each AFC cycle
OFFS(6)	MSB of the measured frequency offset (sign of the offset value)
OFFS(3) -OFFS(0)	Offset value to be added to the value of the frequency control parameter (Four LSB bits)

Note: In order to get accurate values the AFC has to be disabled during the read by clearing the "*en*" bit in the AFC Control Command (bit 0).

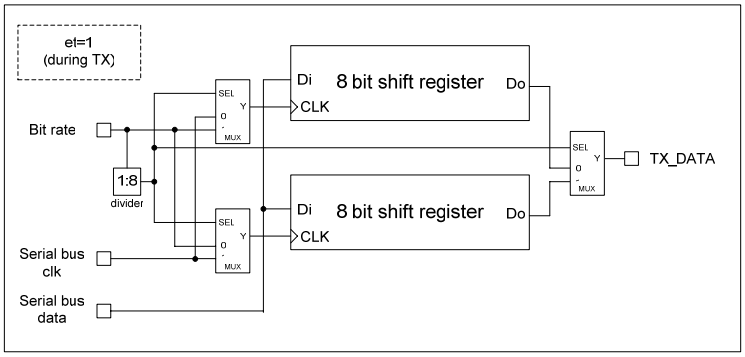
TX REGISTER BUFFERED DATA TRANSMISSION

In this operating mode (enabled by bit *el,* in the *Configuration Control Command*) the TX data is clocked into one of the two 8-bit data registers. The transmitter starts to send out the data from the first register (with the given bit rate) when bit *et* is set with the *Power Management Command*. The initial value of the data registers (AAh) can be used to generate preamble. During this mode, the SDO pin can be monitored to check whether the register is ready (SDO is high) to receive the next byte from the microcontroller.

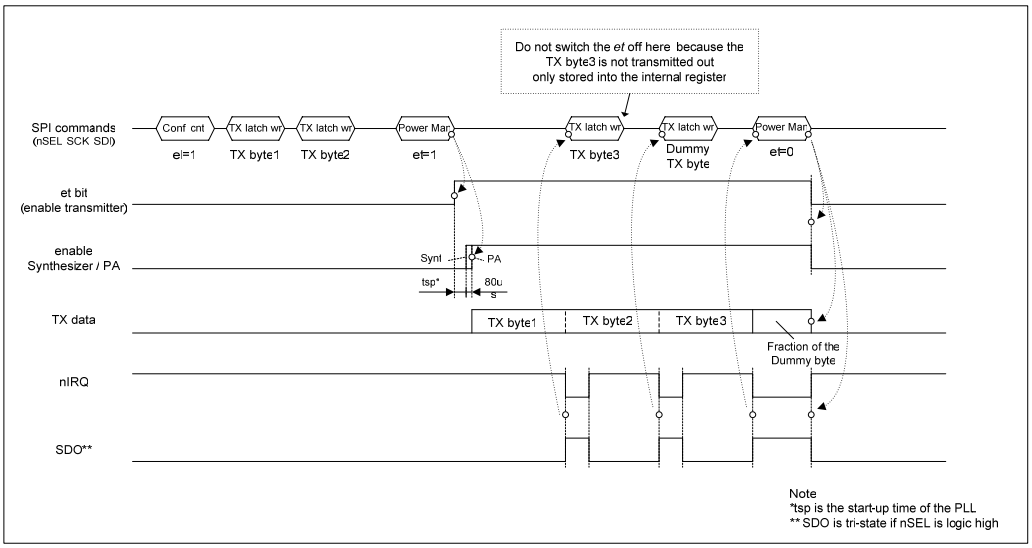
TX register simplified block diagram (before transmit)



TX register simplified block diagram (during transmit)



Typical TX register usage



Note: The content of the data registers are initialized by clearing bit *et*.

RX FIFO BUFFERED DATA READ

In this operating mode, incoming data are clocked into a 16 bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and the synchron pattern recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

Interrupt Controlled Mode:

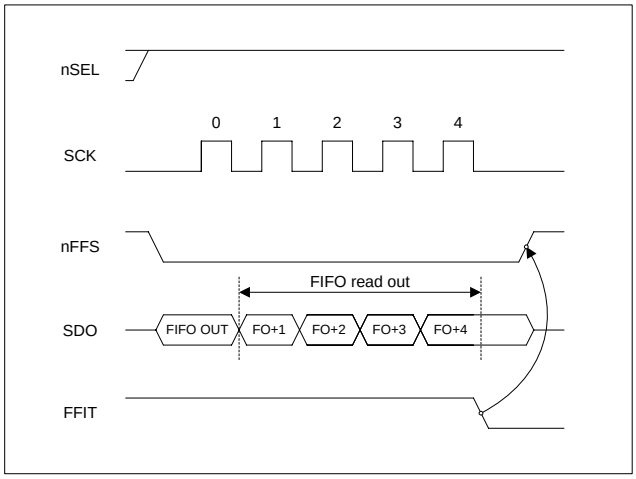
The user can define the FIFO IT level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.

Polling Mode:

When nFFS signal is low the FIFO output is connected directly to the SDO pin and its content can be clocked out by the SCK. Set the FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken.

An SPI read command is also available to read out the content of the FIFO.

FIFO Read Example with FFIT Polling



Note:: During FIFO access f_{SCK} cannot be higher than $f_{ref}/4$, where f_{ref} is the crystal oscillator frequency. When the duty-cycle of the clock signal is not 50 % the shorter period of the clock pulse should be at least $2/f_{ref}$.

RECOMMENDED PACKET STRUCTURES

	Preamble	Synchron word (Can be network ID)	Payload	CRC
Minimum length	4 - 8 bit (1010b or 0101b)	D4h (programmable)	?	4 bit - 1 byte
Recommended length	8 -12 bit (e.g. AAh or 55h)	2DD4h (D4 is programmable)	?	2 byte

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the IA4421 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C_0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 300 ohms ESR (equivalent series loss resistance). However, lower C_0 and ESR values guarantee faster oscillator startup.

The crystal frequency is used as the reference of the PLL, which generates the local oscillator frequency (f_{LO}). Therefore f_{LO} is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable local oscillator frequency error.

Whenever a low frequency error is essential for the application, it is possible to "pull" the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the "midrange", for example 16 pF. The "pull-ability" of the crystal is defined by its motional capacitance and C_0.

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate: 2.4 kbps	Deviation [+/- kHz]						
	30	**45**	**60**	**75**	**90**	**105**	**120**
433 MHz	20	30	50	70	90	100	100
868 MHz	10	20	25	30	40	50	60
915 MHz	10	15	25	30	40	50	50

Bit Rate: 9.6 kbps	Deviation [+/- kHz]						
	30	**45**	**60**	**75**	**90**	**105**	**120**
433 MHz	15	30	50	70	80	100	100
868 MHz	8	15	25	30	40	50	60
915 MHz	8	15	25	30	40	50	50

Bit Rate: 38.4 kbps	Deviation [+/- kHz]						
	30	**45**	**60**	**75**	**90**	**105**	**120**
433 MHz	don't use	5	20	30	50	75	75
868 MHz	don't use	3	10	20	25	30	40
915 MHz	don't use	3	10	15	25	30	40

Bit Rate: 115.2 kbps	Deviation [+/- kHz]						
	105	**120**	**135**	**150**	**165**	**180**	**195**
433 MHz	don't use	3	20	30	50	70	80
868 MHz	don't use	don't use	10	20	25	35	45
915 MHz	don't use	don't use	10	15	25	30	40

RX-TX ALIGNMENT PROCEDURES

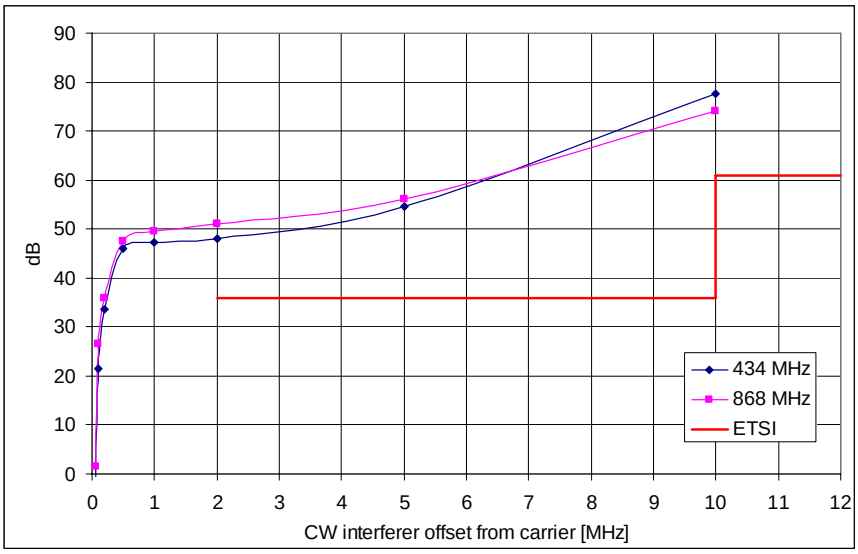
RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "*en*" bit in the AFC Control Command (bit 0).

TYPICAL PERFORMANCE CHARACTERISTICS

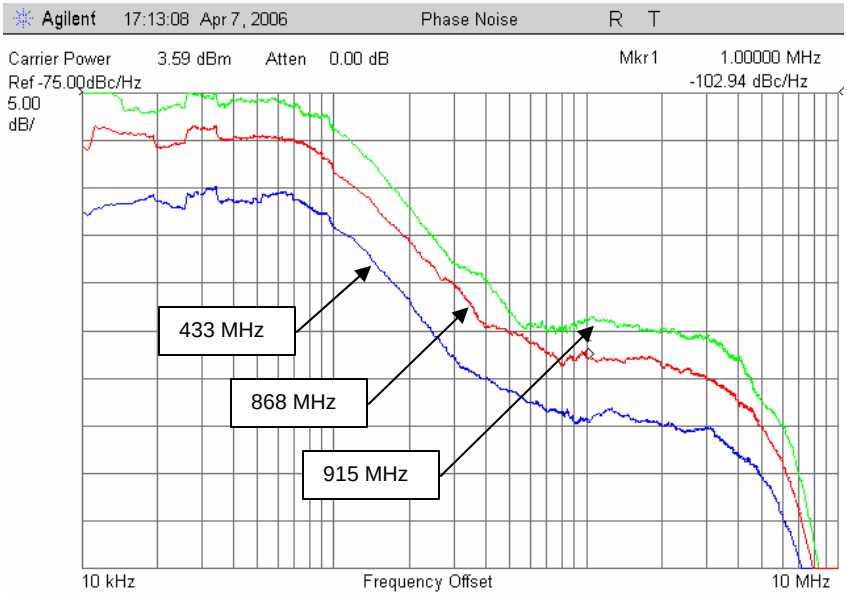
Channel Selectivity and Blocking:



Note:

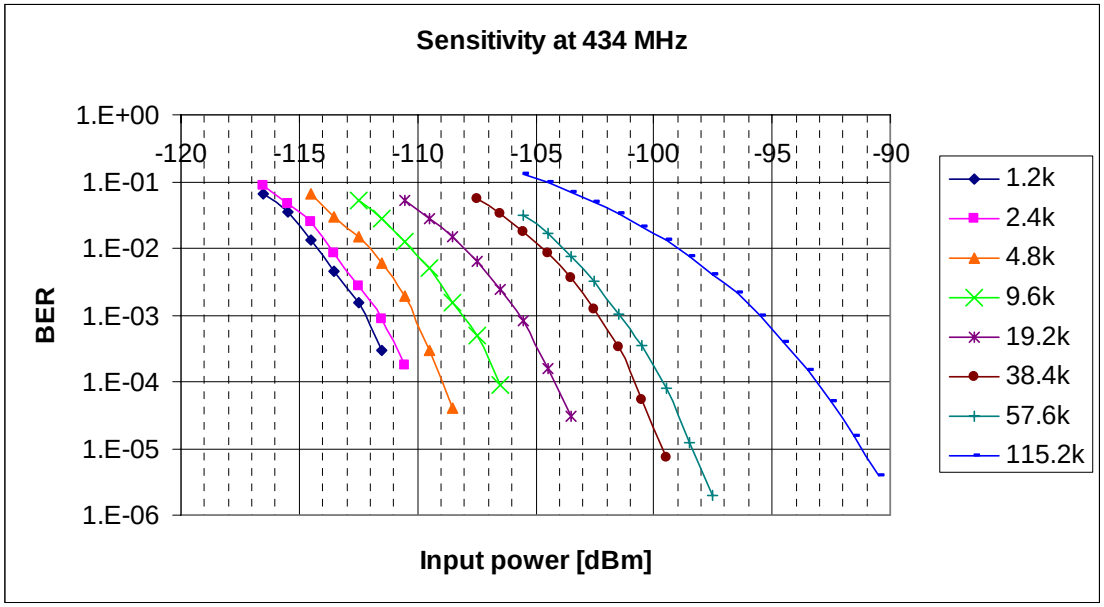
- LNA gain maximum, filter bandwidth 67 kHz, data rate 9.6 kbps, AFC switched off, FSK deviation +/- 45 kHz, V_{dd} = 2.7 V
- Measured according to the descriptions in the ETSI Standard EN 300 220-1 v2.1.1 (2006-01 Final Draft), section 9
- The ETSI limit given in the figure is drawn by taking 109dBm typical sensitivity into account, and corresponds to receiver class 2 requirements (section 4.1.1)

Phase Noise Performance in the 433, 868 and 915 MHz Bands:

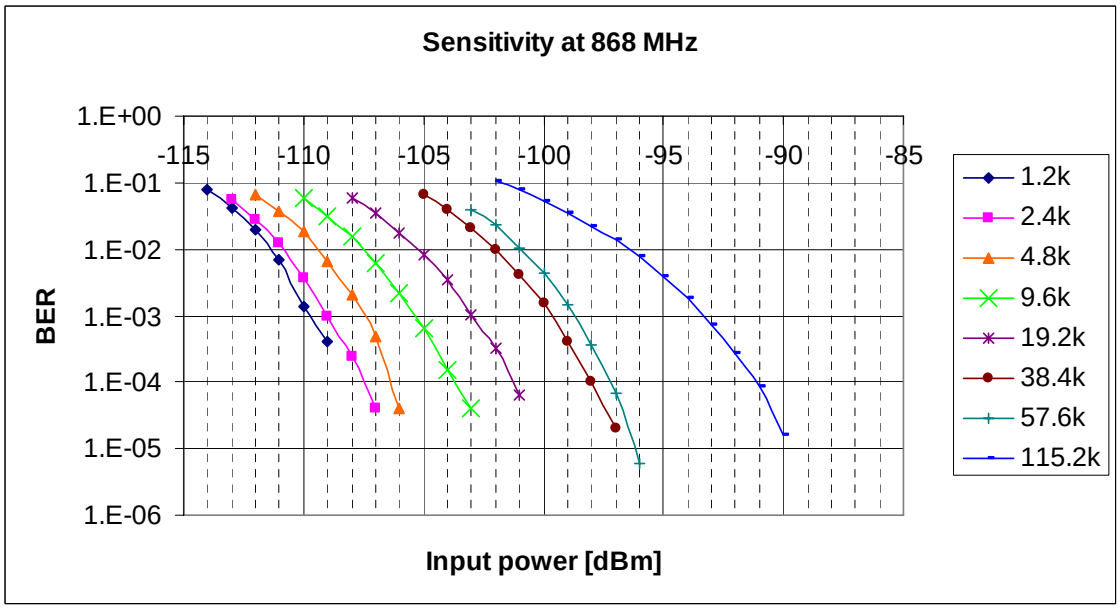


(Measured under typical conditions: T_{op} = 27 °C; V_{dd} = V_{oc} = 2.7 V)

BER Curves in 433 MHz Band:



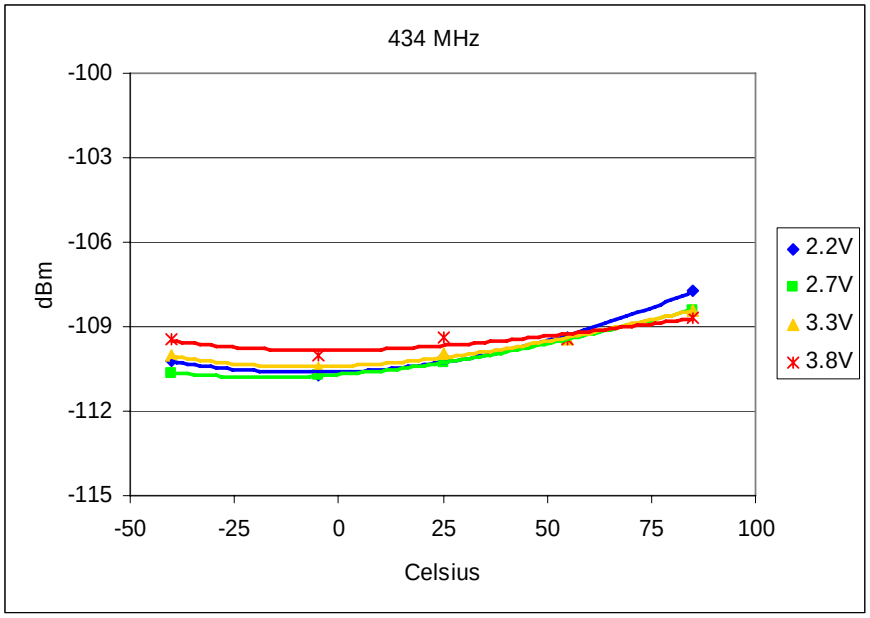
BER Curves in 868 MHz Band:



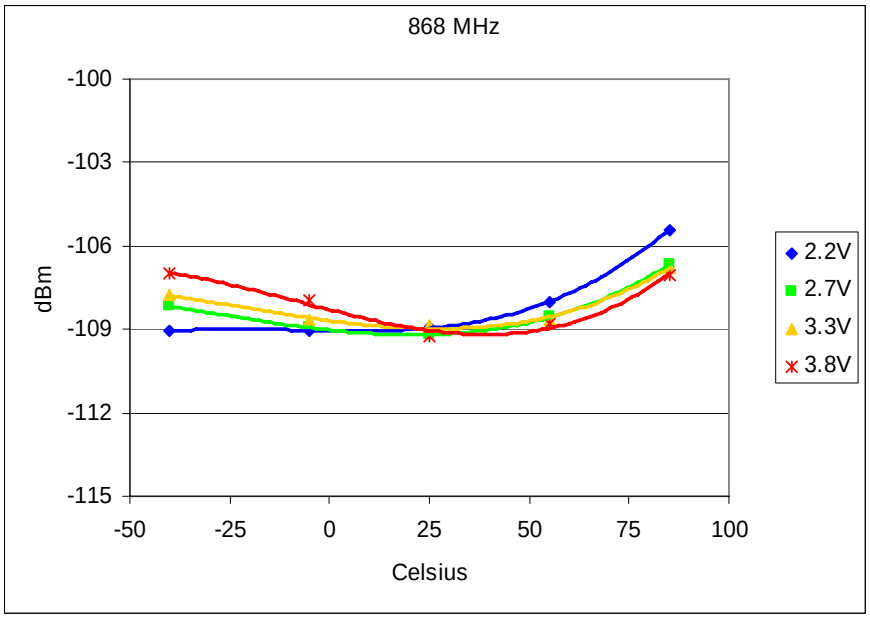
The table below shows the optimal receiver baseband bandwidth (BW) and transmitter deviation frequency (dFfsk) settings for different data-rates supposing no transmit receive offset frequency. If TX/RX offset (for example due to Xtal tolerances) have to be taken into account, increase the BW accordingly.

1.2 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115.2 kbps
BW=67 kHz δf_{FSK} =45 kHz	BW=67 kHz δf_{FSK} =45 kHz	BW=67 kHz δf_{FSK} =45kHz	BW=67 kHz δf_{FSK} =45 kHz	BW=67 kHz δf_{FSK} =45 kHz	BW=134 kHz δf_{FSK} =90 kHz	BW=134 kHz δf_{FSK} =90 kHz	BW=200 kHz δf_{FSK} =120 kHz

Receiver Sensitivity over Ambient Temperature (433 MHz, 9.6 kbps, δf_{FSK}: 45 kHz, BW: 67 kHz):



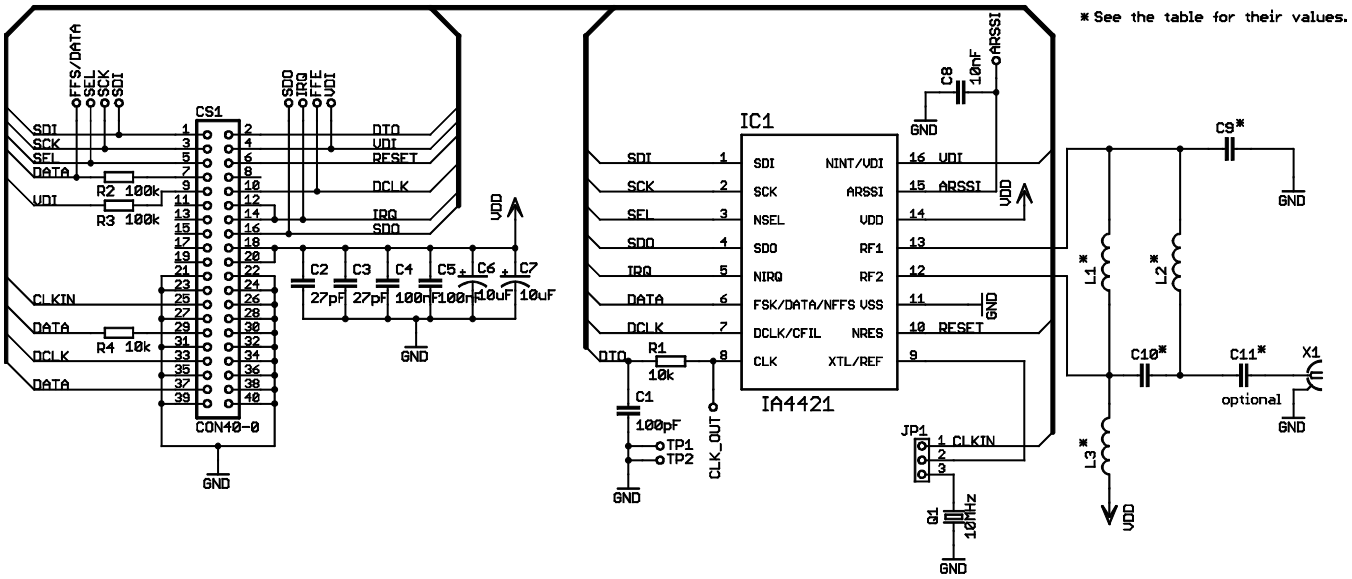
Receiver Sensitivity over Ambient Temperature (868 MHz, 9.6 kbps, δf_{FSK}: 45 kHz, BW: 67 kHz):



REFERENCE DESIGNS

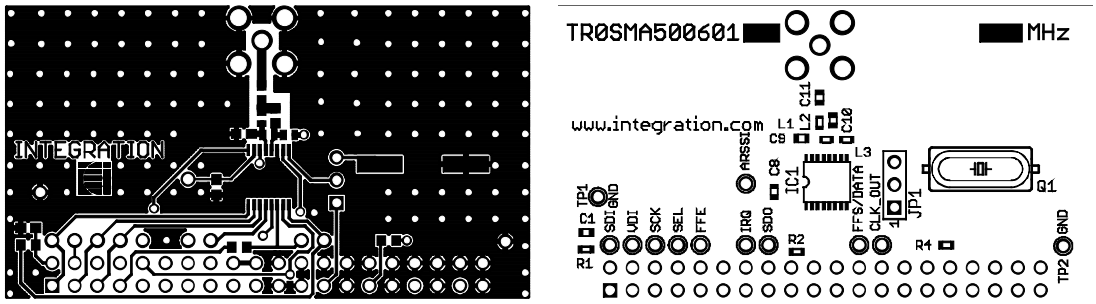
50 Ohm Matching Network

Schematics

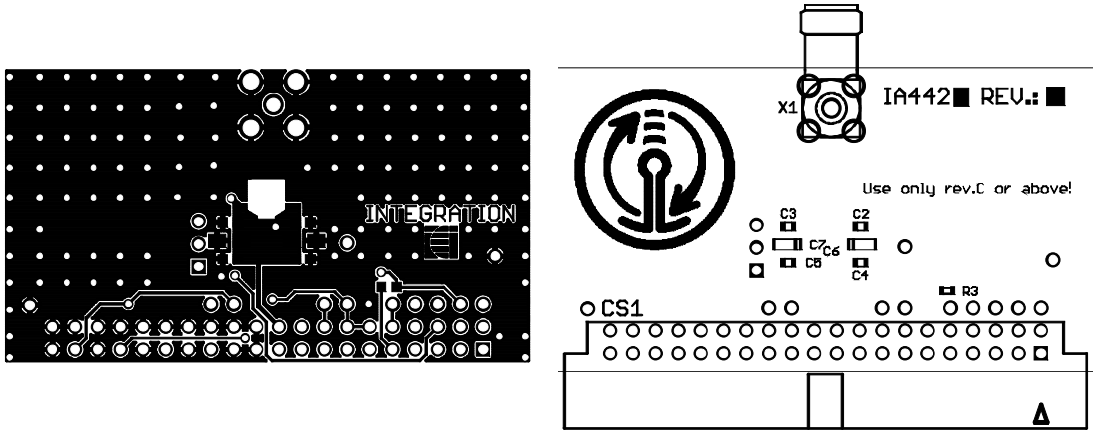


f [MHz]	L1 [nH]	L2 [nH]	L3 [nH]	C9 [pF]	C10 [pF]	C11 [pF]
434	36	47	390	5.1	2.7	68..100
868	8.7	22	100	2.7	1.2	27...56
915	8.7	22	100	2.7	1.2	27...56

PCB Layout



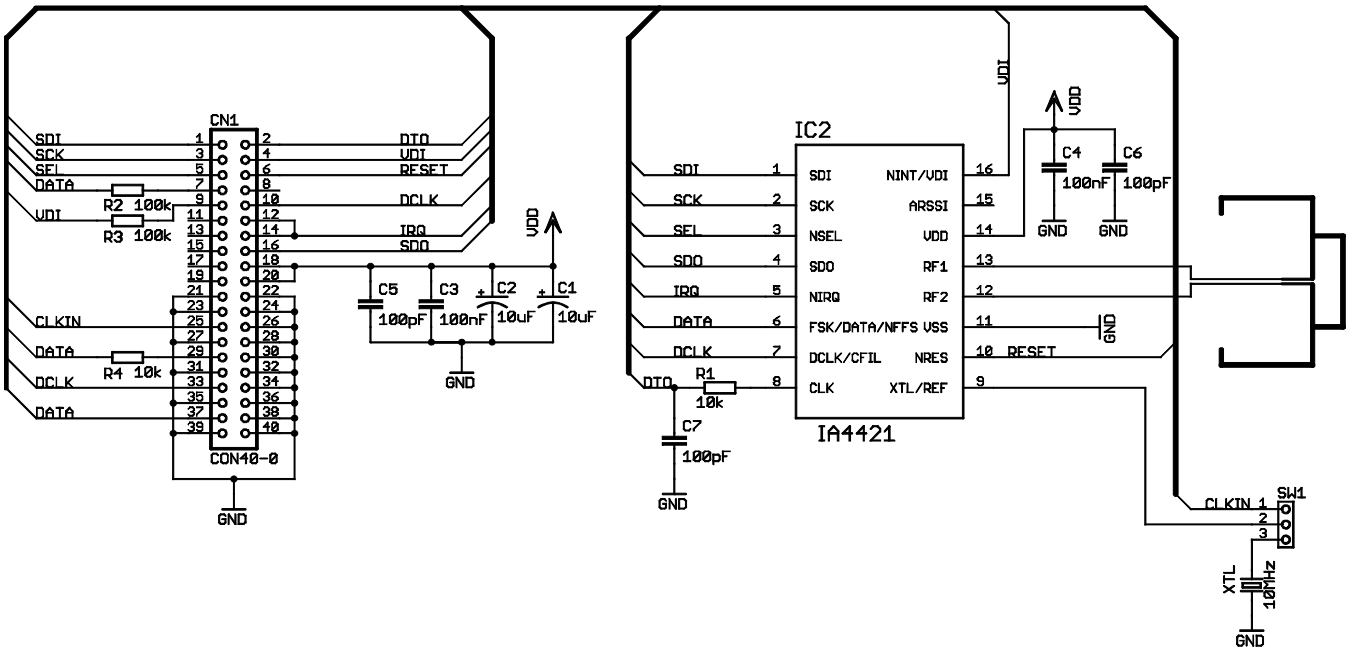
Top View



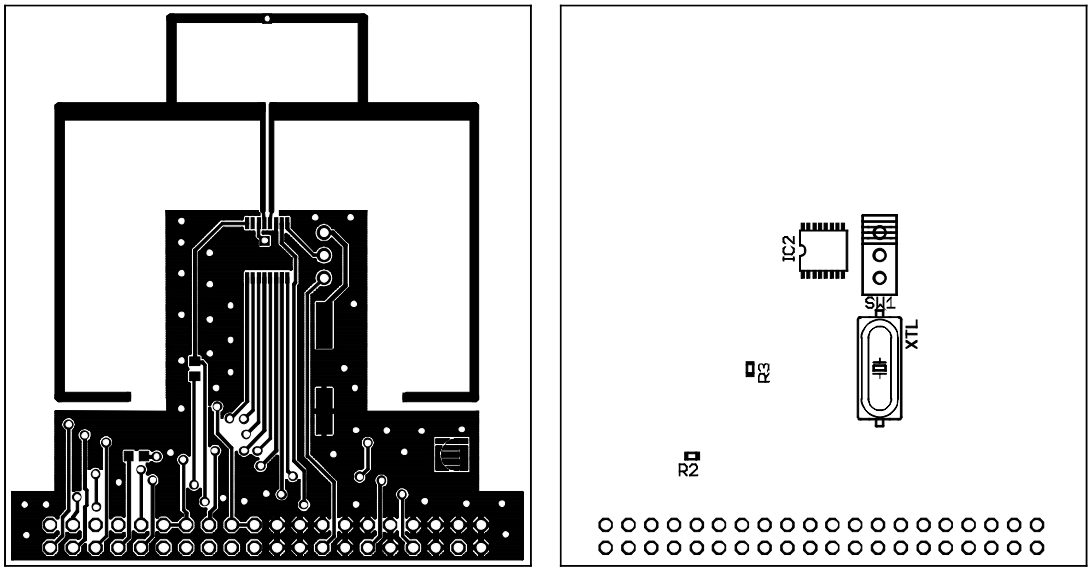
Bottom View

Resonant PCB Antenna (BIFA)

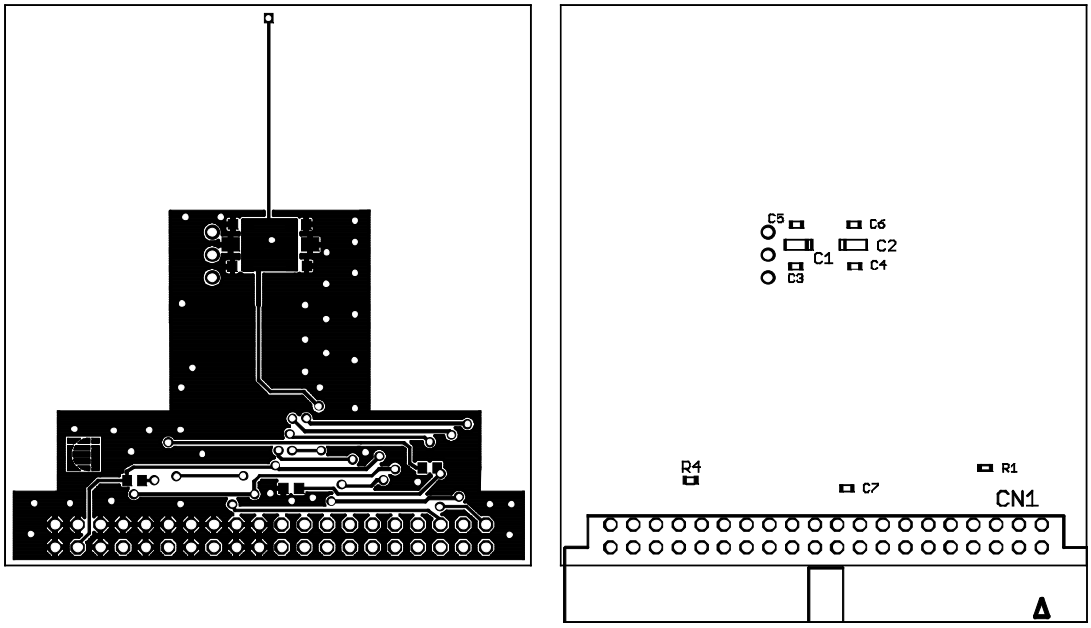
Schematics



PCB Layout (Antenna designed for 870 MHz band)



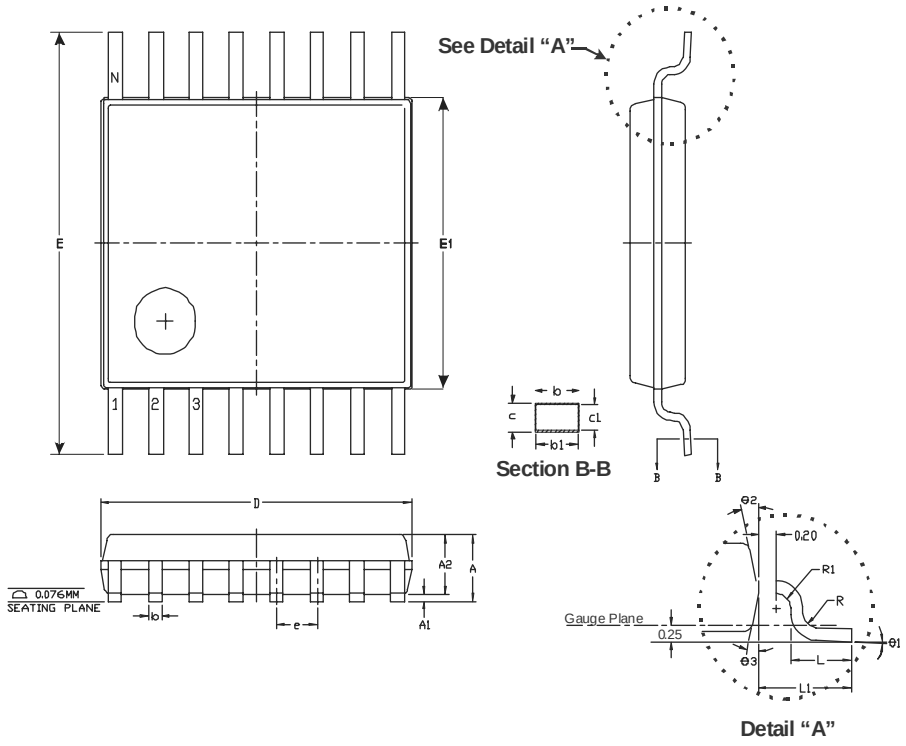
Top View



Bottom View

Package Information

16-pin TSSOP



Symbol	Dimensions in mm			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			1,20			0,047
A1	0,05		0,15	0,002		0,006
A2	0,80	0,90	1,05	0,031	0,035	0,041
b	0,19		0,30	0,007		0,012
b1	0,19	0,22	0,25	0,007	0,009	0,010
c	0,09		0,20	0,004		0,008
c1	0,09		0,16	0,004		0,006
D	4,90	5,00	5,10	0,193	0,197	0,201
e	0.65 BSC.			0.026 BSC.		
E	6.40 BSC.			0.252 BSC.		
E1	4,30	4,40	4,50	0,169	0,173	0,177
L	0,50	0,60	0,75	0,020	0,024	0,030
L1	1.00 REF.			0.39 REF.		
R	0,09			0,004		
R1	0,09			0,004		
θ1	0		8	0		8
θ2	12 REF.			12 REF.		
θ3	12 REF.			12 REF.		

RELATED PRODUCTS AND DOCUMENTS

IA4421 Universal ISM Band FSK Transceiver

DESCRIPTION	ORDERING NUMBER	
IA4421 16-pin TSSOP	IA4421-IC CC16	Revision #

Demo Boards and Development Kits

DESCRIPTION	ORDERING NUMBER
Development Kit	IA ISM – DK
ISM Repeater Demo	IA ISM – DARP

Related Resources

DESCRIPTION	ORDERING NUMBER
Antenna Selection Guide	IA ISM – AN1
Antenna Development Guide	IA ISM – AN2
IA4221 Universal ISM Band FSK Transmitter	See www.integration.com for details
IA4320 Universal ISM Band FSK Receiver	See www.integration.com for details

Note: Volume orders must include chip revision to be accepted.

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