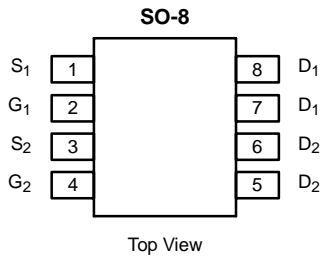




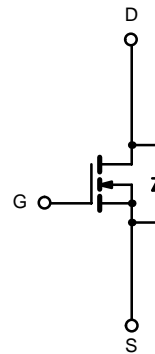
## Dual N-Channel 80-V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
80	0.075 @ $V_{GS} = 10$ V	3.7
	0.095 @ $V_{GS} = 6.0$ V	3.2

**TrenchFET<sup>®</sup>**  
Power MOSFETs



Ordering Information: Si4980DY  
Si4980DY-T1 (with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	80	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	$I_{DM}$	30	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.7	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	62.5	$^\circ\text{C/W}$

Notes  
a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

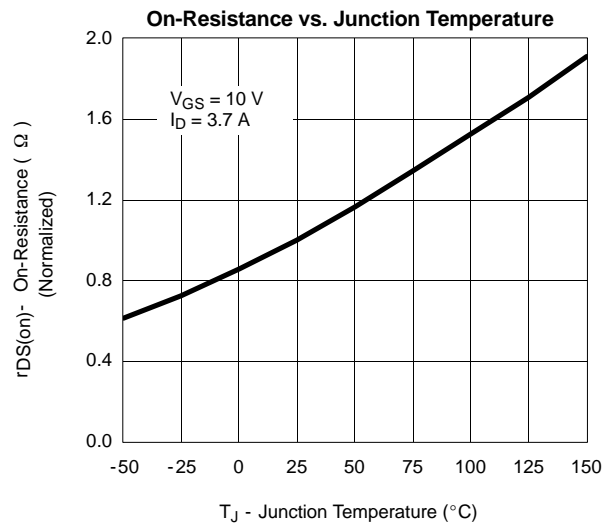
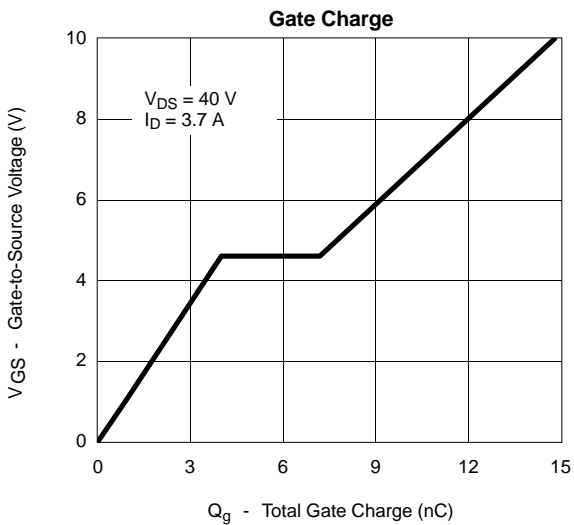
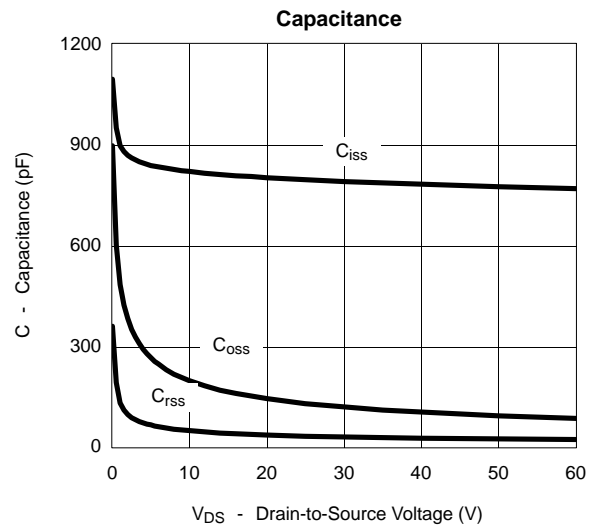
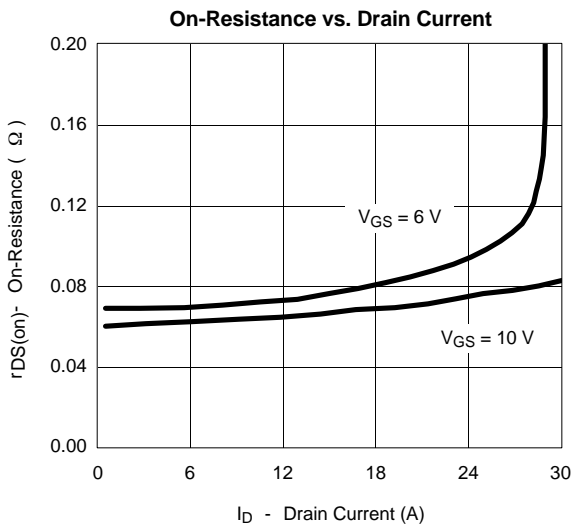
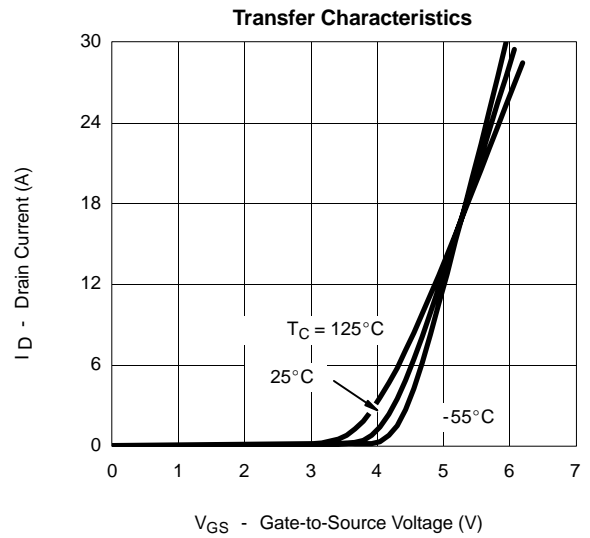
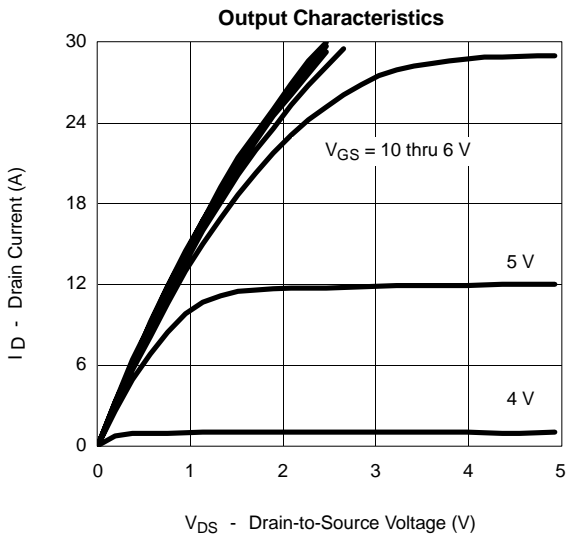
SPECIFICATIONS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
		$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			20	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 3.7\ \text{A}$		0.062	0.075	$\Omega$
		$V_{GS} = 6.0\ \text{V}, I_D = 3.2\ \text{A}$		0.071	0.095	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\ \text{V}, I_D = 3.7\ \text{A}$		12		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 1.7\ \text{A}, V_{GS} = 0\ \text{V}$			1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 40\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 3.7\ \text{A}$		15	30	nC
Gate-Source Charge	$Q_{gs}$		4			
Gate-Drain Charge	$Q_{gd}$		3.2			
Gate Resistance	$R_g$		1		5.1	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\ \text{V}, R_L = 40\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		10	20	ns
Rise Time	$t_r$			10	20	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	$t_f$			10	20	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		75	110	

## Notes

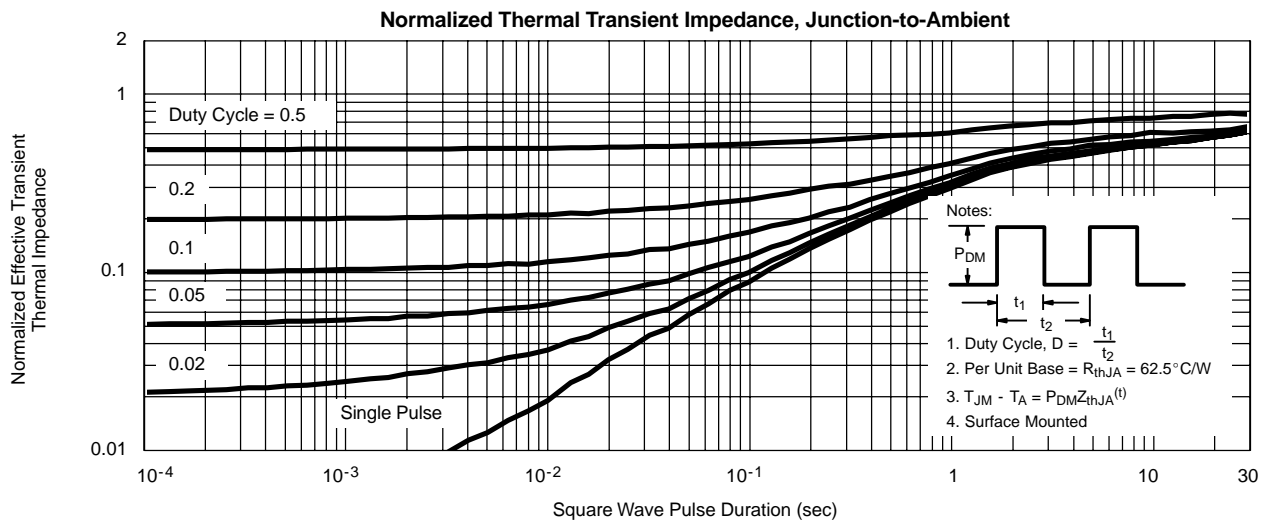
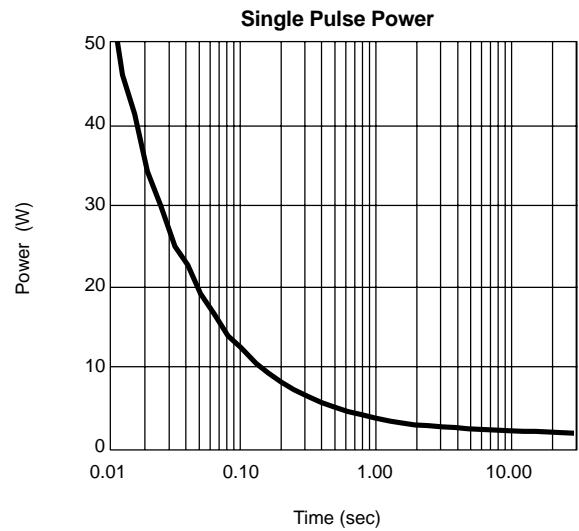
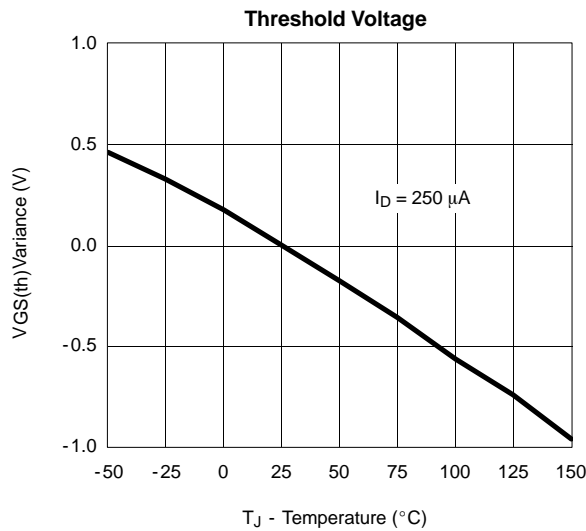
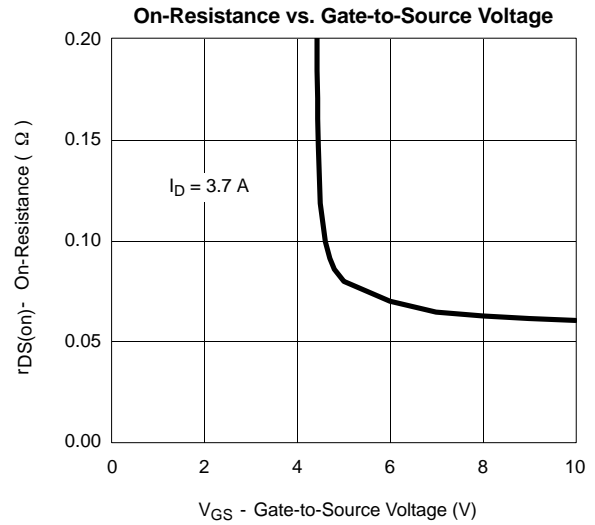
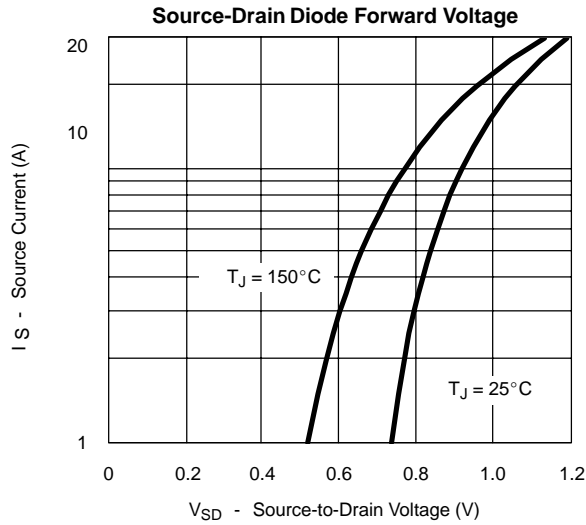
- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. For design aid only; not subject to production testing.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



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