



PD - 94006

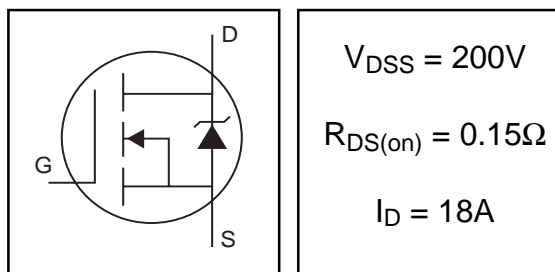
IRF640N
IRF640NS
IRF640NL

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements

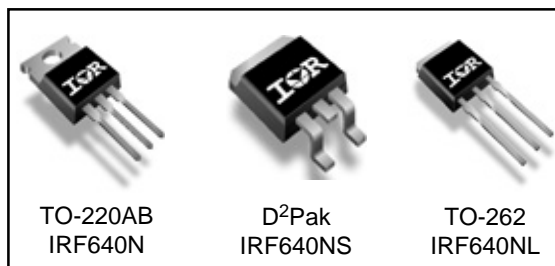
HEXFET® Power MOSFET

Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.



The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



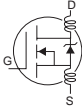
The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF640NL) is available for low-profile application.

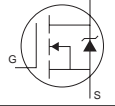
Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---------------------------------|--|------------------------|-------|
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 18 | A |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 13 | |
| I_{DM} | Pulsed Drain Current ① | 72 | |
| $P_D @ T_C = 25^\circ\text{C}$ | Power Dissipation | 150 | W |
| | Linear Derating Factor | 1.0 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy② | 247 | mJ |
| I_{AR} | Avalanche Current① | 18 | A |
| E_{AR} | Repetitive Avalanche Energy① | 15 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 8.1 | V/ns |
| T_J | Operating Junction and Storage Temperature Range | -55 to +175 | °C |
| T_{STG} | | | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting torque, 6-32 or M3 screw④ | 10 lbf•in (1.1N•m) | |

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--|--------------------------------------|------|------|------|-------|--|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 200 | — | — | V | V _{GS} = 0V, I _D = 250μA |
| ΔV _{(BR)DSS} /ΔT _J | Breakdown Voltage Temp. Coefficient | — | 0.25 | — | V/°C | Reference to 25°C, I _D = 1mA |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | — | 0.15 | Ω | V _{GS} = 10V, I _D = 11A ③ |
| V _{GS(th)} | Gate Threshold Voltage | 2.0 | — | 4.0 | V | V _{DS} = V _{GS} , I _D = 250μA |
| g _{fs} | Forward Transconductance | 6.8 | — | — | S | V _{DS} = 50V, I _D = 11A ③ |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | V _{DS} = 200V, V _{GS} = 0V |
| | | — | — | 250 | | V _{DS} = 160V, V _{GS} = 0V, T _J = 150°C |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | V _{GS} = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | V _{GS} = -20V |
| Q _g | Total Gate Charge | — | — | 67 | nC | I _D = 11A |
| Q _{gs} | Gate-to-Source Charge | — | — | 11 | | V _{DS} = 160V |
| Q _{gd} | Gate-to-Drain ("Miller") Charge | — | — | 33 | | V _{GS} = 10V, See Fig. 6 and 13 |
| t _{d(on)} | Turn-On Delay Time | — | 10 | — | ns | V _{DD} = 100V |
| t _r | Rise Time | — | 19 | — | | I _D = 11A |
| t _{d(off)} | Turn-Off Delay Time | — | 23 | — | | R _G = 2.5Ω |
| t _f | Fall Time | — | 5.5 | — | | R _D = 9.0Ω, See Fig. 10 ③ |
| L _D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| L _S | Internal Source Inductance | — | 7.5 | — | |  |
| C _{iss} | Input Capacitance | — | 1160 | — | pF | V _{GS} = 0V |
| C _{oss} | Output Capacitance | — | 185 | — | | V _{DS} = 25V |
| C _{rss} | Reverse Transfer Capacitance | — | 53 | — | | f = 1.0MHz, See Fig. 5 |

Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|-----------------|---|--|------|------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | 18 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode)① | — | — | 72 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.3 | V | T _J = 25°C, I _S = 11A, V _{GS} = 0V ③ |
| t _{rr} | Reverse Recovery Time | — | 167 | 251 | ns | T _J = 25°C, I _F = 11A |
| Q _{rr} | Reverse Recovery Charge | — | 929 | 1394 | nC | di/dt = 100A/μs ③ |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D) | | | | |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|------------------|---------------------------------------|------|------|-------|
| R _{θJC} | Junction-to-Case | — | 1.0 | °C/W |
| R _{θCS} | Case-to-Sink, Flat, Greased Surface ④ | 0.50 | — | |
| R _{θJA} | Junction-to-Ambient④ | — | 62 | |
| R _{θJA} | Junction-to-Ambient (PCB mount)⑤ | — | 40 | |

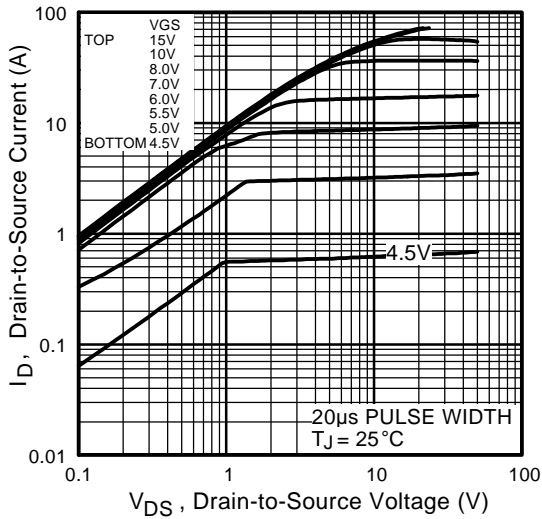


Fig 1. Typical Output Characteristics

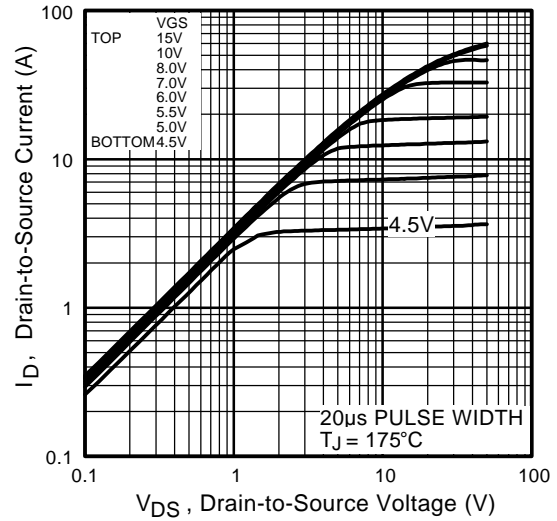


Fig 2. Typical Output Characteristics

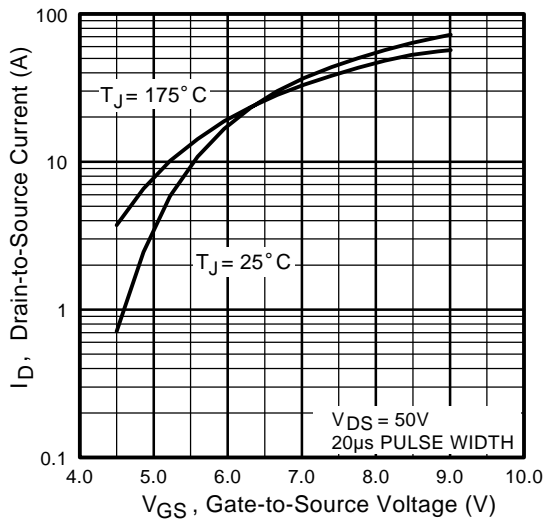


Fig 3. Typical Transfer Characteristics

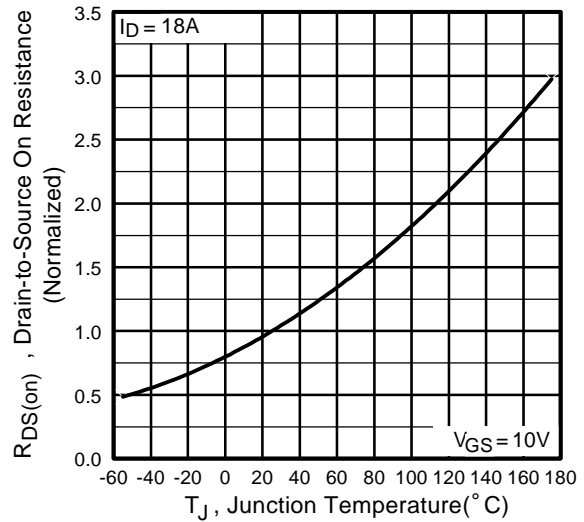


Fig 4. Normalized On-Resistance Vs. Temperature

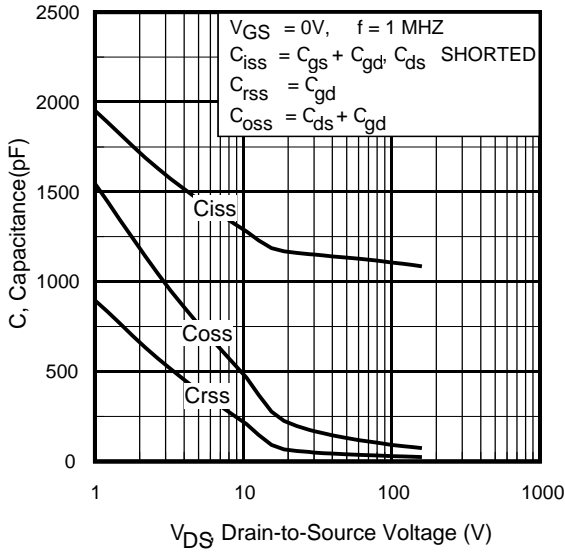


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

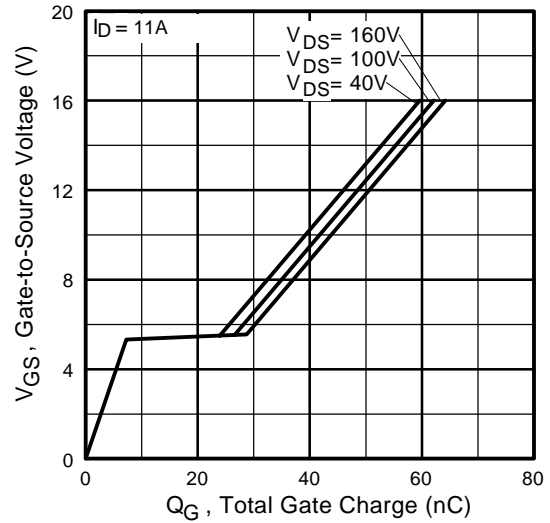


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

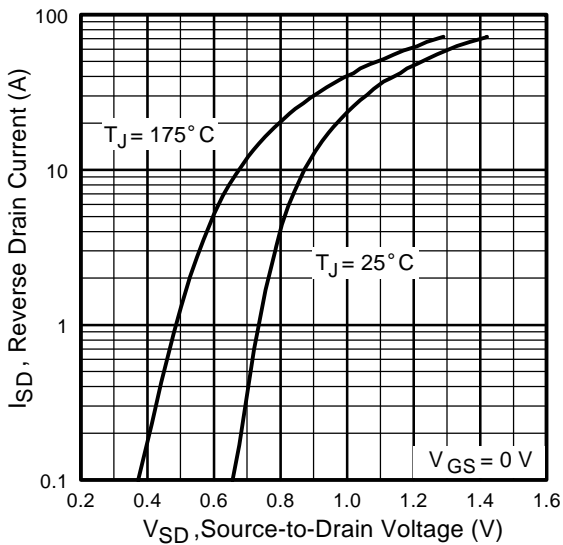


Fig 7. Typical Source-Drain Diode Forward Voltage

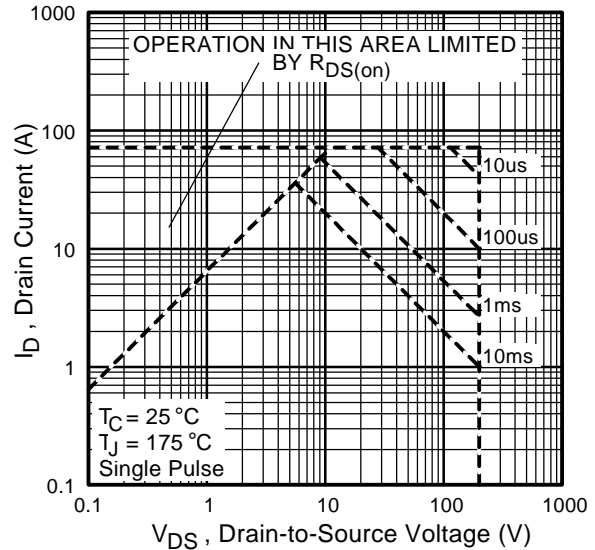


Fig 8. Maximum Safe Operating Area

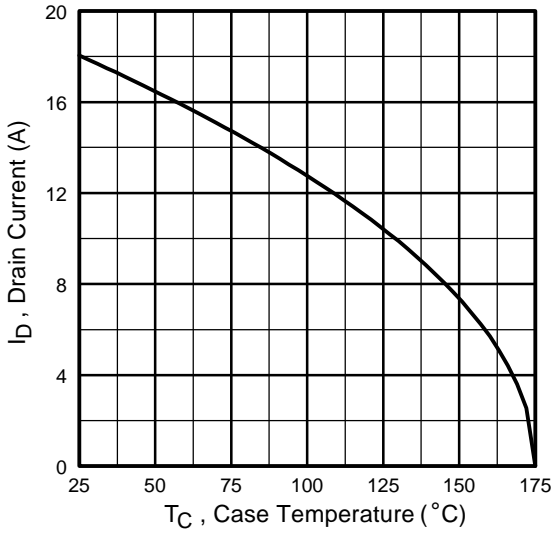


Fig 9. Maximum Drain Current Vs. Case Temperature

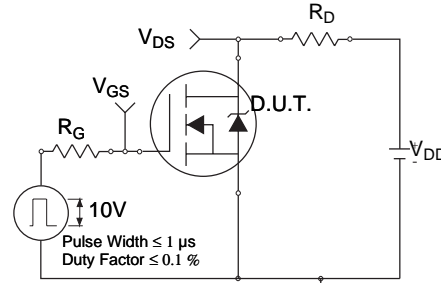


Fig 10a. Switching Time Test Circuit

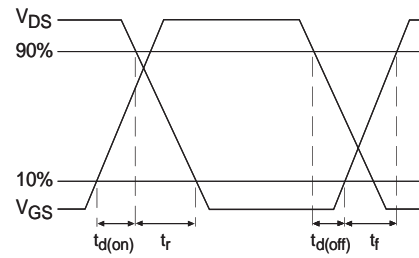


Fig 10b. Switching Time Waveforms

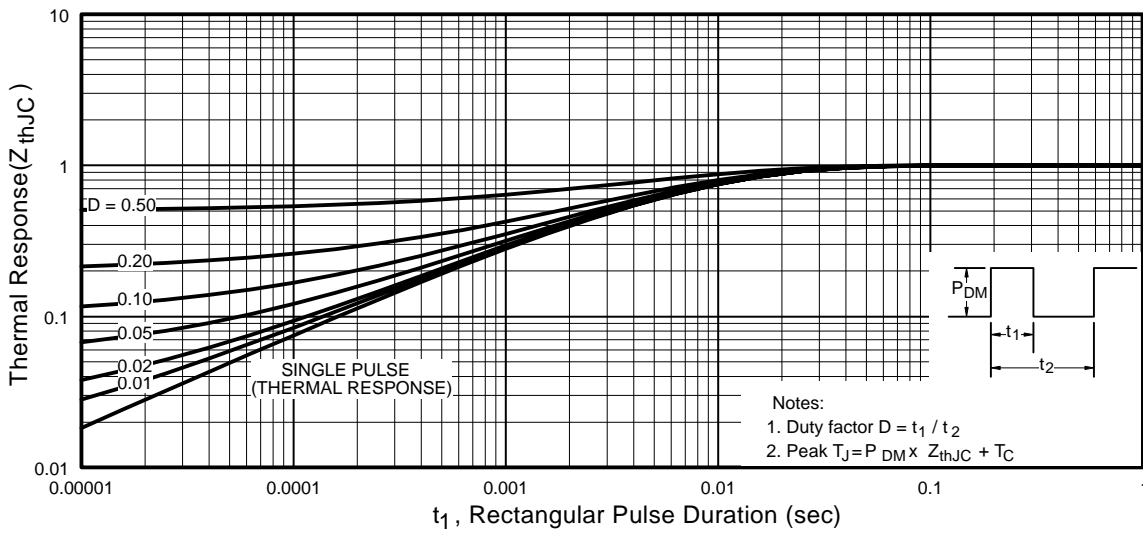


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRF640N/S/L

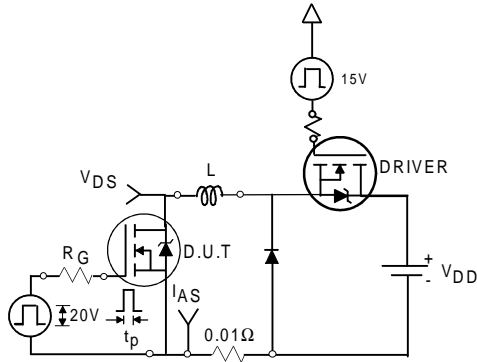


Fig 12a. Unclamped Inductive Test Circuit

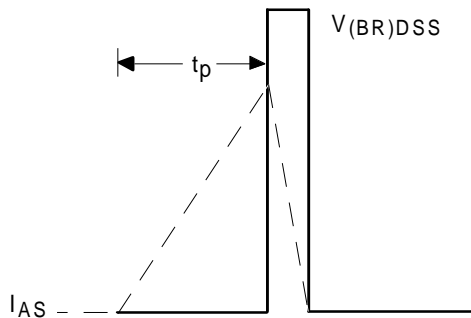


Fig 12b. Unclamped Inductive Waveforms

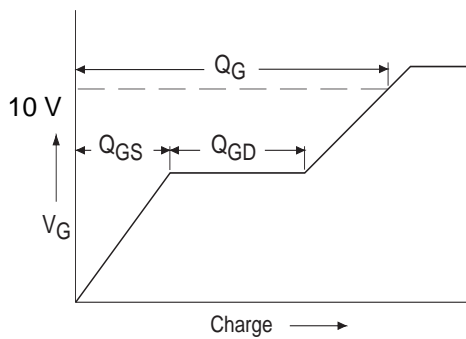


Fig 13a. Basic Gate Charge Waveform

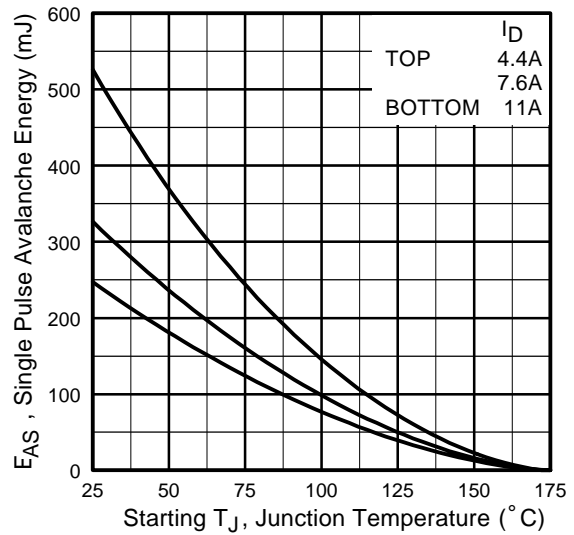


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

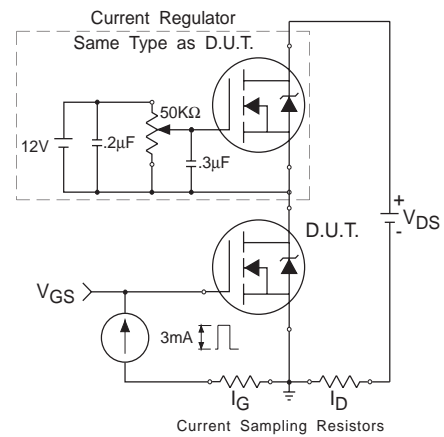
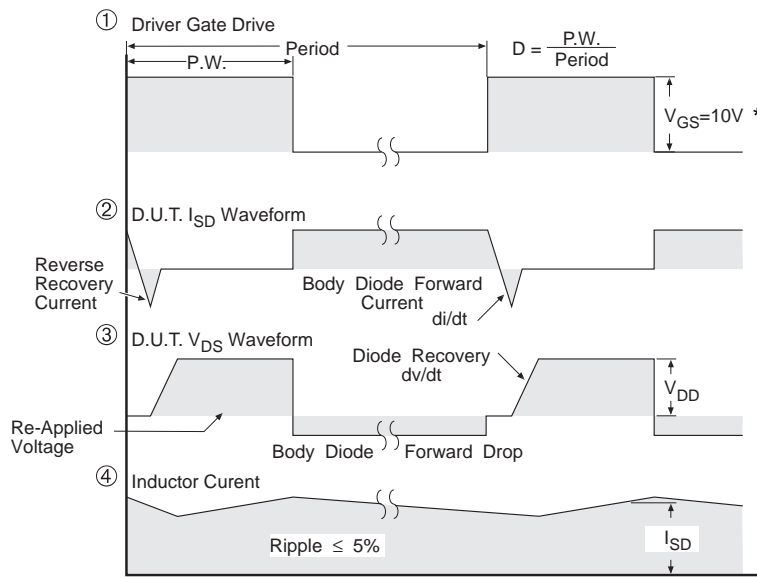
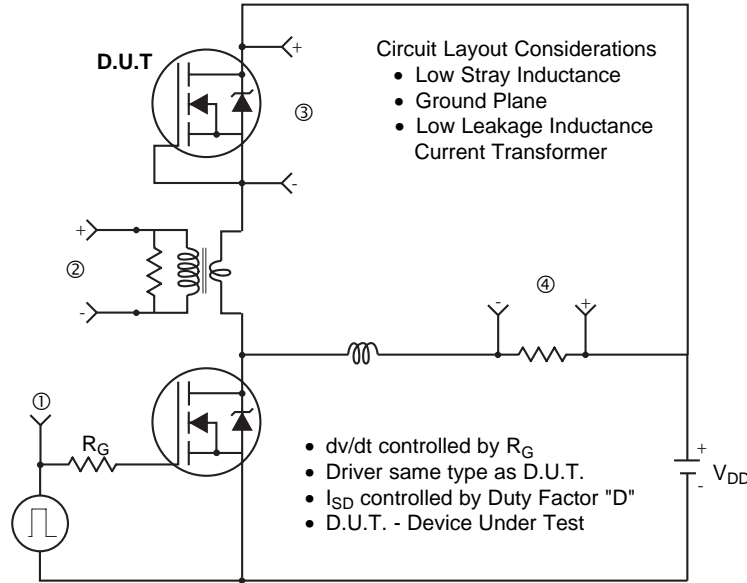


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



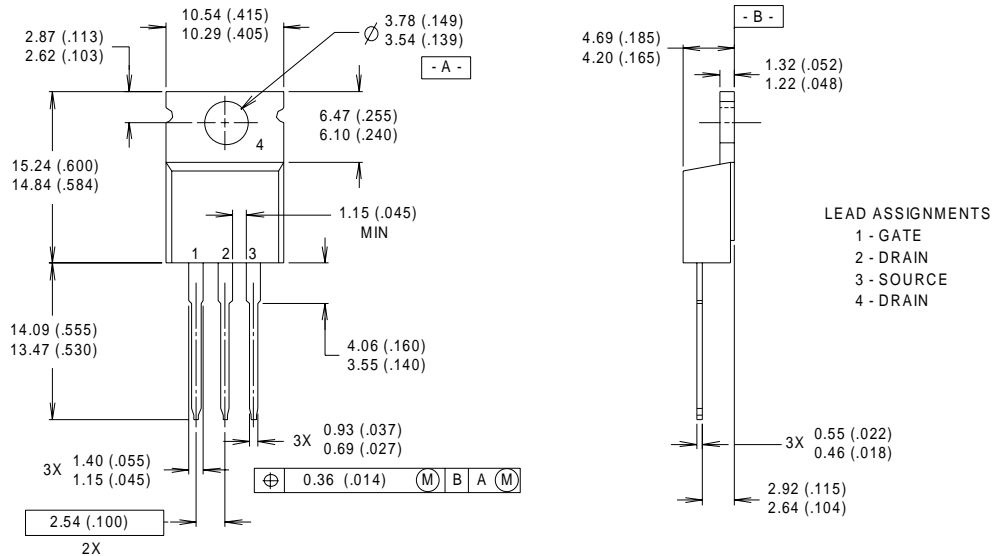
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

IRF640N/S/L

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

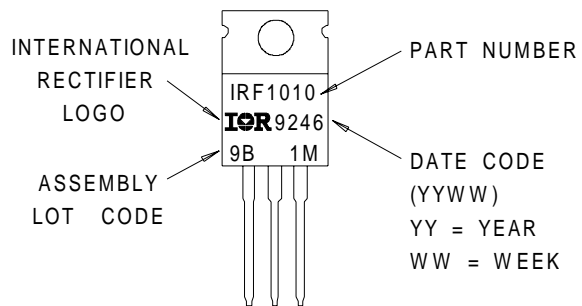


NOTES:

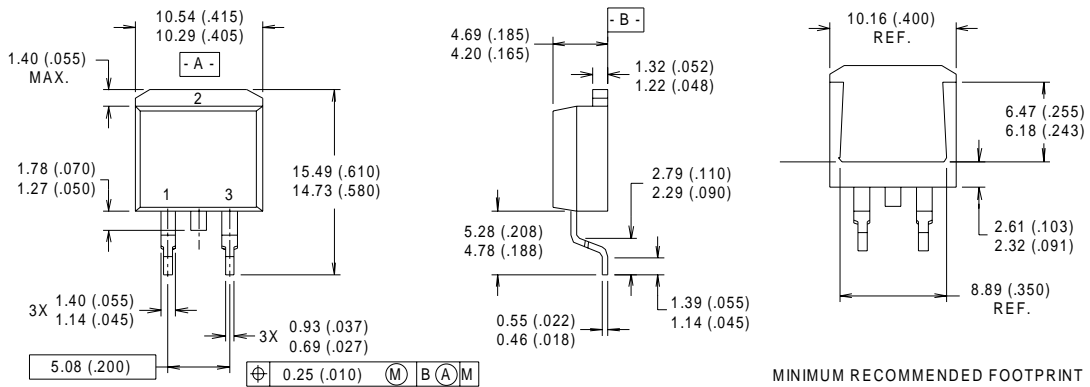
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



D²Pak Package Outline

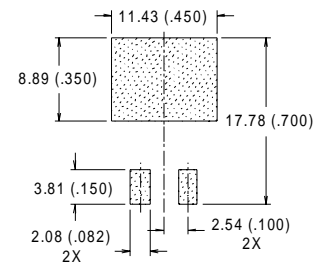


NOTES:

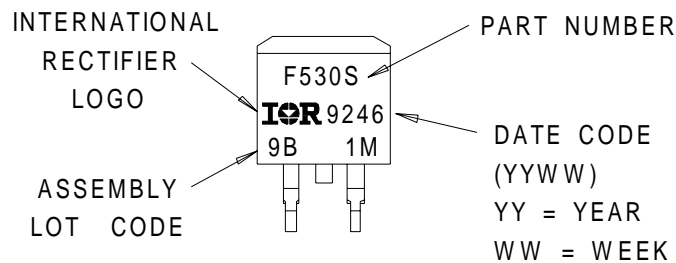
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

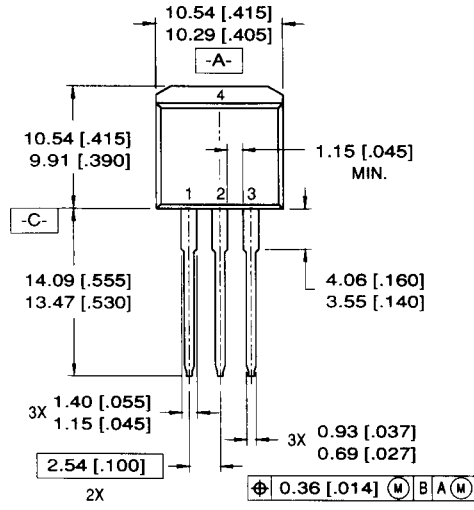


D²Pak Part Marking Information

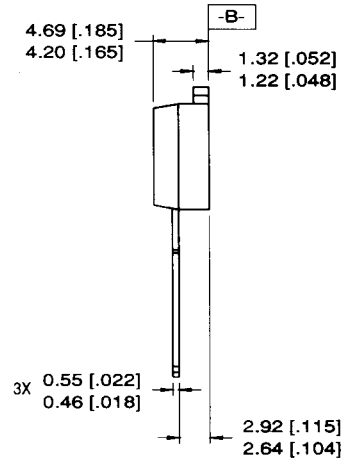


IRF640N/S/L

TO-262 Package Outline



LEAD ASSIGNMENTS
 1 = GATE 3 = SOURCE
 2 = DRAIN 4 = DRAIN

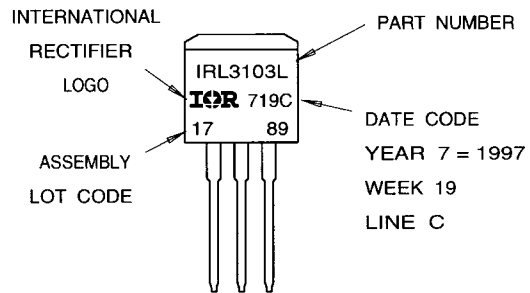


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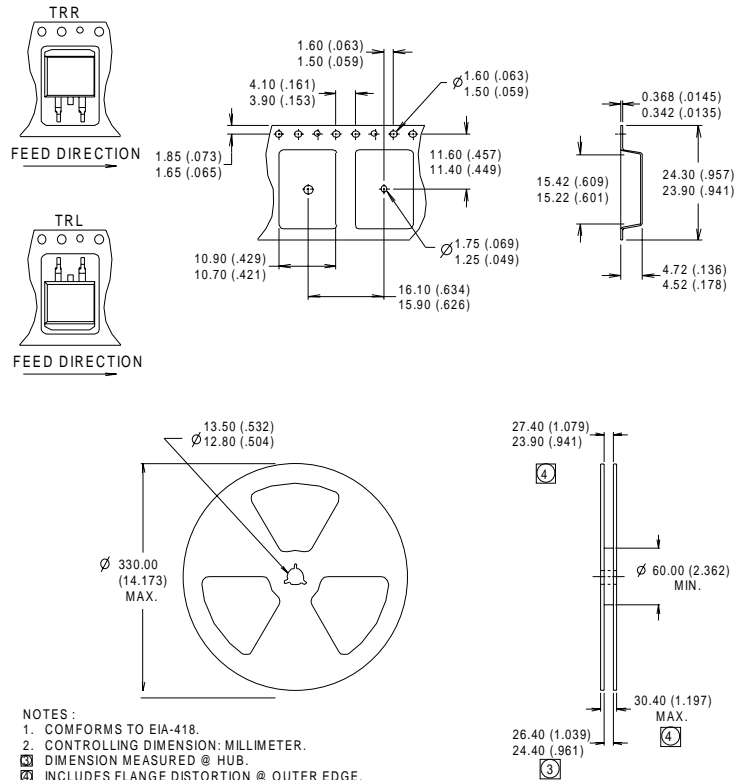
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 4.2\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 11\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ This is only applied to TO-220AB package.
- ⑤ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥ $I_{SD} \leq 11\text{A}$, $di/dt \leq 344\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$