
HD66841

LVIC-II (LCD Video Interface Controller)

HITACHI

ADE-207-315(Z)
'99.9
Rev. 0.0

Description

The HD66841 LCD video interface controller (LVIC-II) converts standard RGB video signals for CRT display into LCD data. It enable a CRT display system to be replaced by an LCD system without any changes, and it also enables software originally intended for CRT display to control an LCD.

Since the LVIC-II can control TFT-type LCDs in addition to current TN-type or STN-type LCDs, it can support 8-color display as well as monochrome, 8-level gray-scale display. It can program screen size and can control a large-panel LCD of 720×512 dots.

The LVIC-II thanks to a gray-scale palette, any 8-levels can be selected from 13 gray-scale levels, depending on the LCD panel used.

Features

- Conversion of RGB video signals used for CRT display into LCD data
 - Monochrome display data
 - 8-level gray-scale data
 - 8-color display data
- Selectable LVIC-II control method
 - Pin programming method
 - Internal register programming method (either with MPU or ROM)
- Programmable screen size
 - 640 or 720 dots (80 or 90 characters) wide by 200, 350, 400, 480, 512, or 540 dots (lines) high, using the pin programming method
 - 32 to 4048 dots (4 to 506 characters) wide by 4 to 1024 dots (lines) high, using internal register programming method

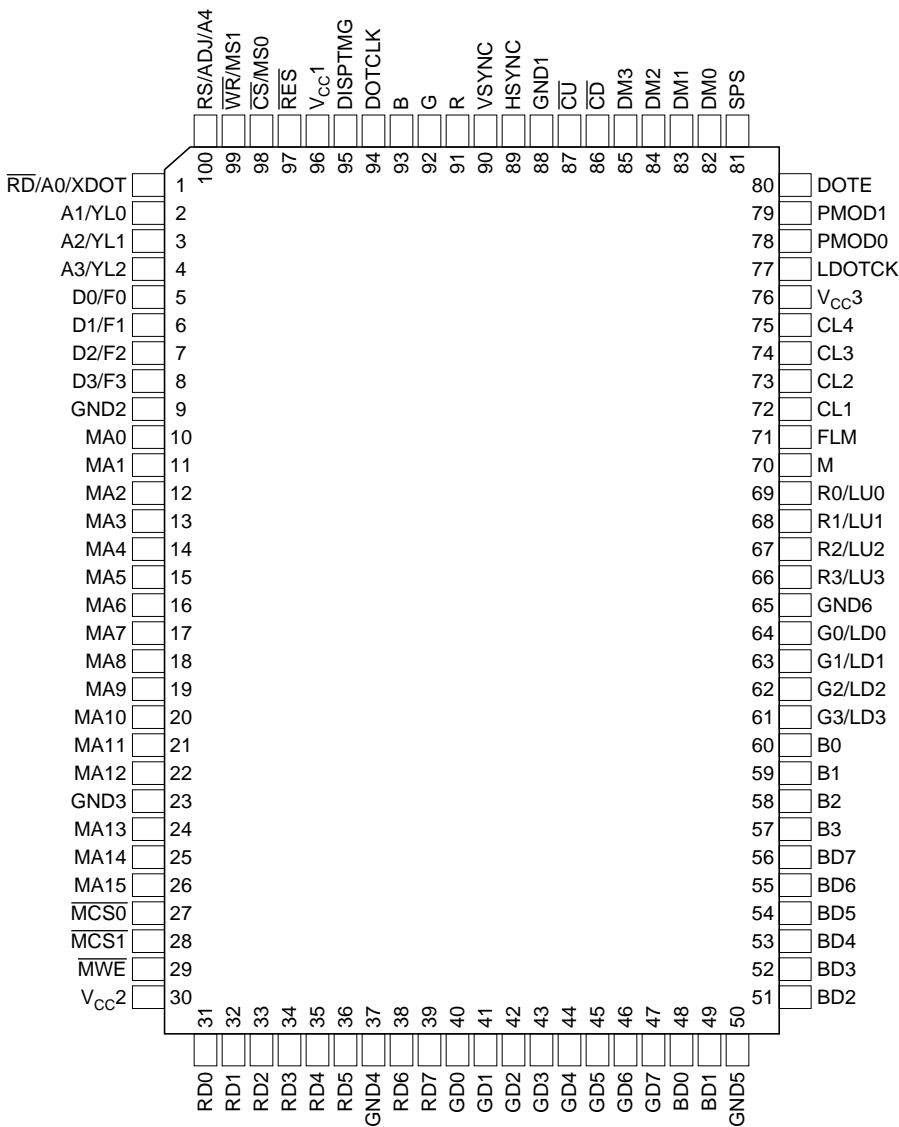
HD66841

- Double-height display capability
- Generation of display timing signal (DISPTMG) from horizontal synchronization (HSYNC) and vertical synchronization (VSYNC) signals
- Control of TN-type, STN-type LCDs and TFT-type LCDs
- Internal PLL circuit capable of generating a CRT display dot clock (DOTCLK) (external charge pump, low pass filter (LPF), and voltage controlled oscillator (VCO) required)
- Gray-scale level selection from gray-scale palette
- Maximum operating frequency (dot clock for CRT display)
 - 30 MHz
- LCD driver interface
 - 4-, 8-, or 12-bit (4 bits each for R, G, and B) parallel data transfer
- Recommended LCD drivers
 - HD66110ST and HD66120T (column)
 - HD66113T and HD66115T (common)
- 1.3 μ m CMOS process
- Single power supply
 - +5 V \pm 10%

Ordering Information

Type No.	Dot Clock	Package
HD66841FS	30 MHZ	100-pin plastic QFP (FP-100A)

Pin Arrangement



(Top view)

Pin Description

The HD66841’s pins are listed in Table 1 and their functions are described below.

Table 1 Pin Description

Classification	Symbol	Pin Number	I/O	Pin Name	Notes
Power supply	V _{CC} 1–V _{CC} 3	96, 30, 76	—	V _{CC} 1, V _{CC} 2, V _{CC} 3	
	GND1–GND6	88, 9, 23, 37, 50, 65	—	Ground 1 to ground 6	
Video signal interface	R, G, B	91, 92, 93	I	Red, green, and blue serial data	1
	HSYNC	89	I	Horizontal synchronization	
	VSYNC	90	I	Vertical synchronization	
	DISPTMG	95	I	Display timing	2
	DOTCLK	94	I	Dot clock	
LCD interface	R0–R3	69–66	O	LCD red data 0–3	3
	LU0–LU3	69–66	O	LCD upper panel data 0–3	4
	G0–G3	64–61	O	LCD green data 0–3	3, 5
	LD0–LD3	64–61	O	LCD lower panel data 0–3	4, 5
	B0–B3	60–57	O	LCD blue data 0–3	3, 6
	CL1	72	O	LCD data line select clock	
	CL2	73	O	LCD data shift clock	
	CL3	74	O	Y-driver shift clock 1	7
	CL4	75	O	Y-driver shift clock 2	7
	FLM	71	O	First line marker	
	M	70	O	LCD driving signal alternation	
	LDOTCK	77	I	LCD dot clock	
Buffer memory interface	MCS0, MCS1	27, 28	O	Memory chip select 0, 1	8
	MWE	29	O	Memory write enable	8
	MA0–MA15	10–22, 24–26	O	Memory address 0–15	8
	RD0–RD7	31–36, 38, 39	I/O	Memory red data 0–7	8
	GD0–GD7	40–47	I/O	Memory green data 0–7	8, 9
	BD0–BD7	48, 49, 51–56	I/O	Memory blue data 0–7	8, 9

Table 1 Pin Description (cont)

Classification	Symbol	Pin Number	I/O	Pin Name	Notes
Mode setting	PMOD0, PMOD1	78, 79	I	Program mode 0, 1	
	DOTÉ	80	I	Dot clock edge change	
	SPS	81	I	Synchronization polarity select	
	DM0–DM3	82–85	I	Display mode 0–3	
	MS0, MS1	98, 99	I	Memory select 0, 1	10, 11
	XDOT	1	I	X-dot	10
	YL0–YL2	2–4	I	Y-line 0–2	10, 12
	ADJ	100	I	Adjust	10
	F0–F3	5–8	I	Fine adjust 0–3	10
MPU interface	$\overline{\text{CS}}$	98	I	Chip select	10, 11
	$\overline{\text{WR}}$	99	I	Write	10, 11, 13
	$\overline{\text{RD}}$	1	I	Read	10, 13
	RS	100	I	Register select	10
	D0–D3	5–8	I/O	Data 0–3	10
	$\overline{\text{RES}}$	97	I	Reset	14
ROM interface	A0–A3, A4	1–4, 100	O	Address 0–4	10
	D0–D3	5–8	I	Data 0–3	10
PLL interface	$\overline{\text{CD}}$	86	O	Charge down	
	$\overline{\text{CU}}$	87	O	Charge up	

Notes: 1. Fix G and B pins low if CRT display data is monochrome.

2. Fix high or low if the display timing signal is generated internally.

3. For 8-color display modes.

4. For monochrome or 8-level gray-scale display modes.

5. Leave disconnected in 4-bit/single-screen data transfer modes.

6. Leave disconnected in monochrome or 8-level gray-scale display modes.

7. Leave disconnected in TN-type LCD modes.

8. Leave disconnected if no buffer memory is used.

9. Pull up with a resistor of about 20k Ω in monochrome display modes.

The HD66841 writes the OR of RGB signals into R-plane RAM, so no RAM is required for the G and B planes in these modes. (If G- or B-plane RAM is connected in monochrome display modes, the HD66841 writes G or B signals into each RAM. However, this does not affect the display or the contents of R-plane RAM.)

10. Multiplexed pins.

11. Fix high or low when using the ROM programming method.

12. Fix high or low when using the MPU programming method.

13. Do not set pins $\overline{\text{WR}}$ and $\overline{\text{RD}}$ low simultaneously.

14. A reset signal must be input after power-on.

Pin Functions

Power Supply

V_{CC}1–V_{CC}3: Connect V_{CC}1–V_{CC}3 with +5V.

GND1–GND6: Ground GND1–GND6.

CRT Display Interface

R, G, B: Input CRT display R, G, B signals on R, G and B respectively.

HSYNC: Input the CRT horizontal synchronization on HSYNC.

VSYN: Input the CRT vertical synchronization on VSYNC.

DISPTMG: Input the display timing signal, which announces the horizontal or vertical display period, on DISPTMG.

DOTCLK: Input the dot clock for CRT display on DOTCLK.

LCD Interface

R0–R3: R0–R3 output R data for the LCD.

LU0–LU3: LU0–LU3 output LCD up panel data.

G0–G3: G0–G3 output G data for the LCD.

LD0–LD3: LD0–LD3 output LCD down panel data.

B0–B3: B0–B3 output B data for the LCD.

CL1: CL1 outputs the line select clock for LCD data.

CL2: CL2 outputs the shift clock for LCD data.

CL3: CL3 outputs the line select and shift clock when a Y-driver is set on one side of an LCD screen (see “LCD System Configuration”).

CL4: CL4 outputs the line select and shift clock when Y-drivers are set on both sides of an LCD screen (see “LCD System Configuration”).

FLM: FLM outputs the first line marker for a Y-driver.

M: The M output signal converts the LCD drive signal to AC.

LDOTCK: LDOTCK outputs the LCD dot clock.

Buffer Memory Interface

$\overline{\text{MCS0}}$, $\overline{\text{MCS1}}$: $\overline{\text{MCS0}}$ and $\overline{\text{MCS1}}$ output the buffer memory chip select signal.

$\overline{\text{MWE}}$: $\overline{\text{MWE}}$ outputs the write enable signal of buffer memories.

MA0–MA15: MA0–MA15 output buffer memory addresses.

RD0–RD7: RD0–RD7 transfer data between R data buffer memory and the LVIC.

GD0–GD7: GD0–GD7 transfer data between G data buffer memory and the LVIC.

BD0–BD7: BD0–BD7 transfer data between B data buffer memory and the LVIC.

Mode Setting

PMOD0, PMOD1: The PMOD0–PMOD1 input signals select a programming method (Table 6).

NOTE: The DOTE input signal switches the timing of the data latch. The LVIC latches R, G and B signal at the falling edge of DOTCLK when DOTE is high, and at the rising edge when low.

SPS: The SPS input signal selects the polarity of VSYNC. (The polarity of HSYNC is fixed.) VSYNC is high active when SPS is high, and low active when low.

DM0–DM3: The DM0–DM3 input signals select a display mode (Table 8).

MS0–MS1: The MS0–MS1 input signals select the kind of buffer memories (Table 2).

XDOT: The XDOT input signal specifies the number of horizontal displayed characters. The number is 90 when XDOT is high, and 80 when low.

YL0–YL2: The YL0–YL2 input signals specify the number of vertical displayed lines (Table 3).

ADJ: The ADJ input signal determines whether F0–F3 pins adjust the number of vertical displayed lines or the display timing signal. F0–F3 pins adjust the display timing signal when ADJ is high, and adjust the number of vertical displayed lines when low.

F0–F3: F0–F3 input data for adjusting the number of vertical displayed lines (Table 4), or the display timing signal (see “Fine Adjustment of Display Timing Signal”).

MPU Interface

- \overline{CS} :** The MPU selects the LVIC when \overline{CS} is low.
- \overline{WR} :** The MPU inputs the \overline{WR} write signal to write data into internal registers of the LVIC. The MPU can write data when \overline{WR} is low and cannot write data when high.
- \overline{RD} :** The MPU inputs the \overline{RD} read signal to read data from internal registers of the LVIC. The MPU can read data when \overline{RD} is low and cannot read data when high.
- RS:** The MPU inputs the RS signal together with \overline{CS} to select internal registers. The MPU selects data registers (R0–R15) when RS is high and \overline{CS} is low, and selects the address register (AR) when RS is low and \overline{CS} is low.
- D0–D3:** D0–D3 transfer internal register data between the MPU and LVIC.
- \overline{RES} :** \overline{RES} inputs the external reset signal.

ROM Interface

- A0–A4:** A0–A4 output address 0 to address 4 to an external ROM.
- D0–D3:** D0–D3 input data from an external ROM to internal registers.

PLL Circuit Interface

- \overline{CD} :** \overline{CD} outputs the charge down signal to an external charge pump.
- \overline{CU} :** \overline{CU} outputs the charge up signal to an external charge pump.

Table 2 Programming Method Selection

PMOD 1	PMOD 0	Programming Method	
0	0	Pin programming	
0	1	Internal register	MPU
1	0	programming	ROM
1	1	Prohibited*	

Note: * This combination is for test mode: it disables display.

Table 3 Memory Type Selection

MS1	MS0	Memory Type
0	0	No memory
0	1	8-kbytes memory
1	0	32-kbytes memory
1	1	64-kbytes memory

Table 4 Number of Vertical Displayed Lines

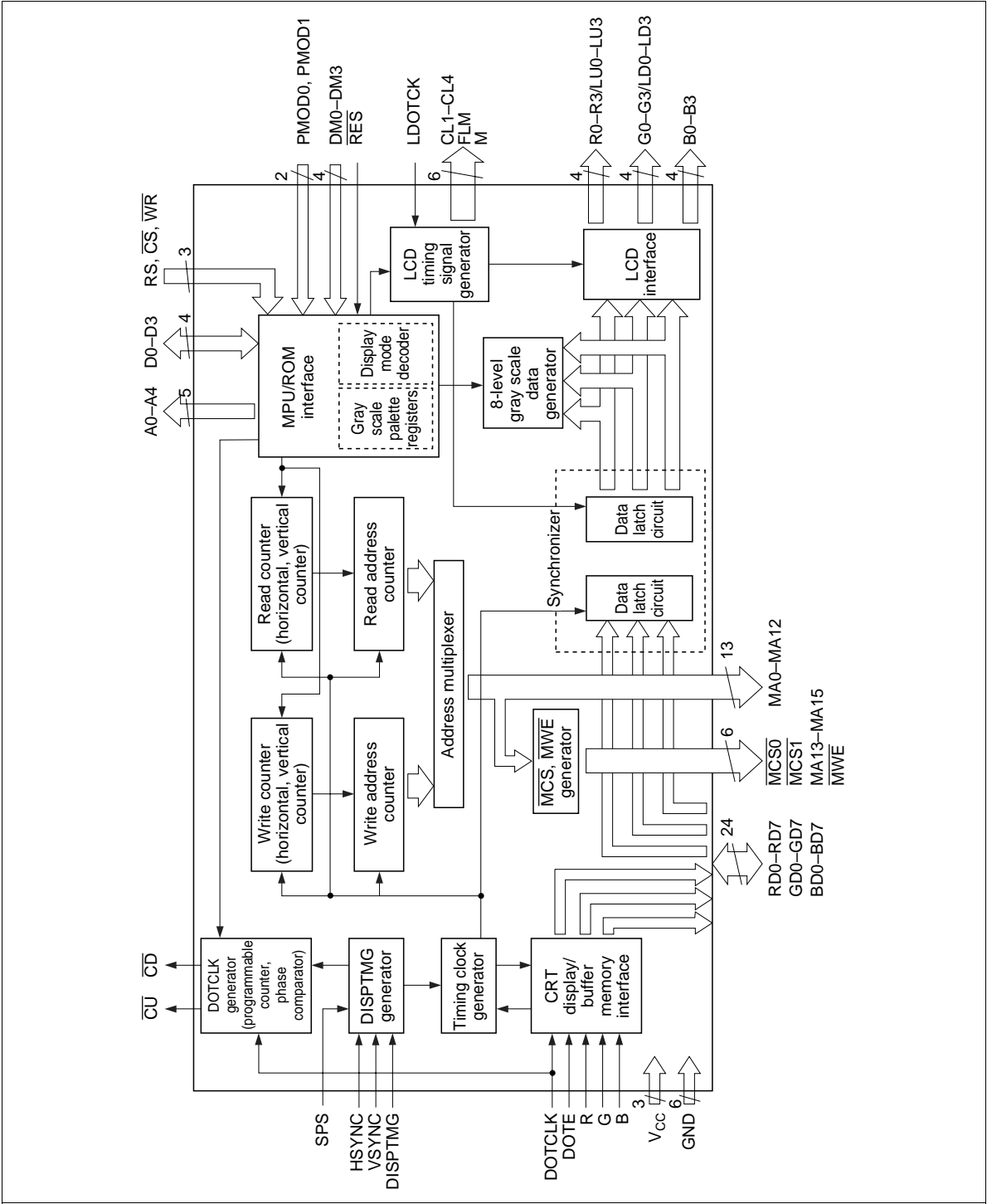
YL2	YL1	YL0	Number of Vertical Displayed Lines
0	0	0	200
0	0	1	350
0	1	0	400
0	1	1	480
1	0	0	512
1	0	1	540
1	1	0	Prohibited *
1	1	1	

Note: * 480 lines are displayed, but they are practically indistinguishable.

Table 5 Fine Adjustment of Vertical Displayed Lines

F3	F2	F1	F0	Number of Adjusted Lines
0	0	0	0	±0
0	0	0	1	+1
0	0	1	0	+2
.
.
.
1	1	1	0	+14
1	1	1	1	+15

Block Diagram



Registers

The HD66841's registers are listed in Table 6 and the bit assignments within the registers are shown in Figure 1.

Table 6 Register List

CS	RS	Reg. Address				Reg. No.	Register Name	Program Unit	Specified Value Symbol	Read/Write* ²	Notes
		PS* ¹	3	2	1	0					
1	—	—	—	—	—	—	—	—	—	—	
0	0	—	—	—	—	AR	Address register	—	—	W	3
0	1	0	0	0	0	R0	Control register 1	—	—	R/W	
0	1	0	0	0	0	1	R1	Control register 2	—	—	R/W
0	1	0	0	0	1	0	R2	Vertical displayed lines register (middle-order)	Line	Nvd	R/W 4
0	1	0	0	0	1	1	R3	Vertical displayed lines register (low-order)	Line	Nvd	R/W 4
0	1	0	0	1	0	0	R4	Vertical displayed lines register (high-order)/ CL3 period register (high-order)	Line/Chars	Nvd/Npc	R/W 4, 5, 6
0	1	0	0	1	0	1	R5	CL3 period register (low-order)	Chars.	Npc	R/W 4, 5, 6
0	1	0	0	1	1	0	R6	Horizontal displayed characters register (high-order)	Chars.	Nhd	R/W 6
0	1	0	0	1	1	1	R7	Horizontal displayed characters register (low-order)	Chars.	Nhd	R/W 6
0	1	0	1	0	0	0	R8	CL3 pulse width register	Chars.	Npw	R/W 6
0	1	0	1	0	0	1	R9	Fine adjust register	Dots	Nda	R/W 7
0	1	0	1	0	1	0	R10	PLL frequency-division ratio register (high-order)	—	N _{PLL}	R/W 8
0	1	0	1	0	1	1	R11	PLL frequency-dividing ratio register (low-order)	—	N _{PLL}	R/W 8
0	1	0	1	1	0	0	R12	Vertical backporch register (high-order)	Lines	Ncvbp	R/W 4, 9
0	1	0	1	1	0	1	R13	Vertical backporch register (low-order)	Lines	Ncvbp	R/W 4, 9
0	1	0	1	1	1	0	R14	Horizontal backporch register (high-order)	Dots	Nchbp	R/W 4, 9
0	1	0	1	1	1	1	R15	Horizontal backporch register (low-order)	Dots	Nchbp	R/W 4, 9

Table 6 Register List (cont.)

CS	RS	PS*1	Reg. Address				Reg. No.	Register Name	Program Unit	Value Symbol	Specified Read/Write*2	Notes
			3	2	1	0						
0	1	1	0	0	0	1	P1	Black palette register	—	—	R/W	
0	1	1	0	0	1	0	P2	Blue palette register	—	—	R/W	
0	1	1	0	0	1	1	P3	Red palette register	—	—	R/W	
0	1	1	0	1	0	0	P4	Magenta palette register	—	—	R/W	
0	1	1	0	1	0	1	P5	Green palette register	—	—	R/W	
0	1	1	0	1	1	0	P6	Cyan palette register	—	—	R/W	
0	1	1	0	1	1	1	P7	Yellow palette register	—	—	R/W	
0	1	1	1	0	0	0	P8	White palette register	—	—	R/W	
0	1	1	1	0	0	1		Reserved				
.				
.				
.				
0	1	1	1	1	1	1		Reserved				

- Notes:
- 1. Corresponds to bit 2 of control register 1 (R0)
 - 2. W indicates that the register can only be written to; R/W indicates that the register can both be read from and written to.
 - 3. Attempting to read data from this register when RS = 0 drives the bus to high-impedance state; output data becomes undefined.
 - 4. Write (the specified value–1) into this register.
 - 5. Valid only in 8-color display modes with horizontal stripes.
 - 6. One character consists of eight horizontal dots.
 - 7. Valid only if the display timing signal is supplied externally.
 - 8. Valid only if the dot clock signal is generated internally.
 - 9. Valid only if the display timing signal is generated internally.

			Reg. Address				Reg. No.	Data Bit				
CS	RS	PS ^{*1}	3	2	1	0		3	2	1	0	
1	—	—	—	—	—	—	—	*2				
0	0	—	—	—	—	—	AR					← Address register
0	1	—	0	0	0	0	R0	DIZ	PS	DSP	DCK	← Control register 1
0	1	0	0	0	0	1	R1	MC	DON	MS1	MS0	← Control register 2
0	1	0	0	0	1	0	R2					← Vertical displayed lines register
0	1	0	0	0	1	1	R3					
0	1	0	0	1	0	0	R4					
0	1	0	0	1	0	1	R5					← CL3 period register
0	1	0	0	1	1	0	R6 ^{*3}					← Horizontal displayed characters register
0	1	0	0	1	1	1	R7					
0	1	0	1	0	0	0	R8					← CL3 pulse width register
0	1	0	1	0	0	1	R9					← Fine adjust register
0	1	0	1	0	1	0	R10					← PLL frequency-division ratio register
0	1	0	1	0	1	1	R11					
0	1	0	1	1	0	0	R12					← Vertical backporch register
0	1	0	1	1	0	1	R13					
0	1	0	1	1	1	0	R14					← Horizontal backporch register
0	1	0	1	1	1	1	R15					
0	1	1	0	0	0	1	P1 ^{*4}	0	0	0	0	← Black palette register
0	1	1	0	0	1	0	P2 ^{*4}	0	0	1	0	← Blue palette register
0	1	1	0	0	1	1	P3 ^{*4}	0	1	0	1	← Red palette register
0	1	1	0	1	0	0	P4 ^{*4}	0	1	1	0	← Magenta palette register
0	1	1	0	1	0	1	P5 ^{*4}	0	1	1	1	← Green palette register
0	1	1	0	1	1	0	P6 ^{*4}	1	0	0	0	← Cyan palette register
0	1	1	0	1	1	1	P7 ^{*4}	1	0	1	0	← Yellow palette register
0	1	1	1	0	0	0	P8 ^{*4}	1	0	0	0	← White palette register
0	1	1	1	0	0	1	—	*5				← Reserved register
⋮	⋮	⋮	⋮	⋮	⋮	⋮	—					
0	1	1	1	1	1	1	—					

- Notes: 1. Corresponds to bit 2 of control register 1 (R0).
2. Invalid bits. Attempting to read data from these bits returns undefined data.
3. The most significant bit is invalid in dual-screen configuration modes.
4. Bit values shown are default values at reset.
5. Reserved bits. Any Attempt to write data into the register is invalid, although it has no affect on LSI operations. Any attempt to read data from the register returns undefined data.

Figure 1 Register Bit Assignment

System Configuration

Figure 2 is a block diagram of a system in which the HD66841 is used outside a personal computer.

The HD66841 converts the RGB serial data sent from the personal computer into parallel data and temporarily writes it to the buffer memory. It then reads out the data in order and outputs it to LCD drivers to drive the LCD. In this case, the CRT display dot clock (DOTCLK), which is a latch clock for serial data, is generated by the PLL circuit from the horizontal synchronization signal (HSYNC). The DOTCLK signal frequency is specified by the PLL frequency-division ratio register (R10, R11).

The system can be configured without a VCO and LPF if the DOTCLK signal is supplied externally, and it can be configured without an MPU if the LVIC-II is controlled by the pin programming method.

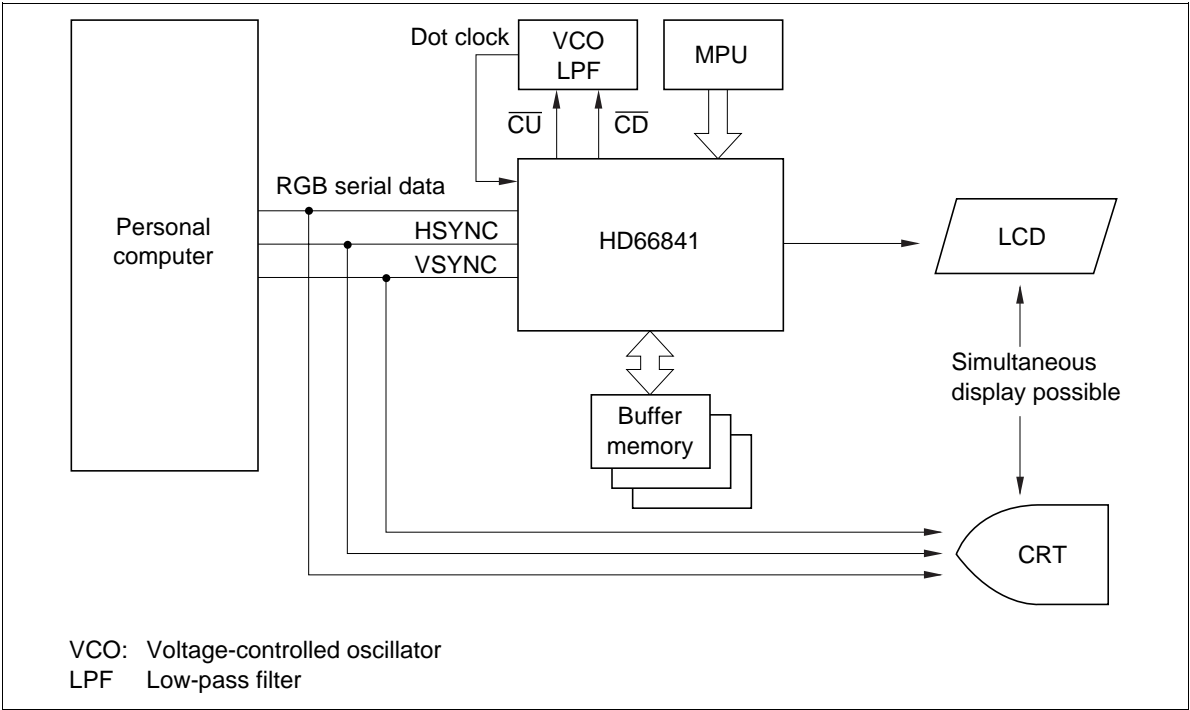


Figure 2 System Block Diagram
(with MPU Programming Method and DOTCLK Generated Internally)

Functional Description

Programming Method

The user may select one of two methods to control the HD66841 functions: by pin programming method or by internal registers (internal register programming method). The internal register programming method can be divided into the MPU programming method and the ROM programming method. The MPU writes data into internal registers in the MPU programming method and ROM writes the data in the ROM programming method. Table 7 lists the relation between programming method and pins.

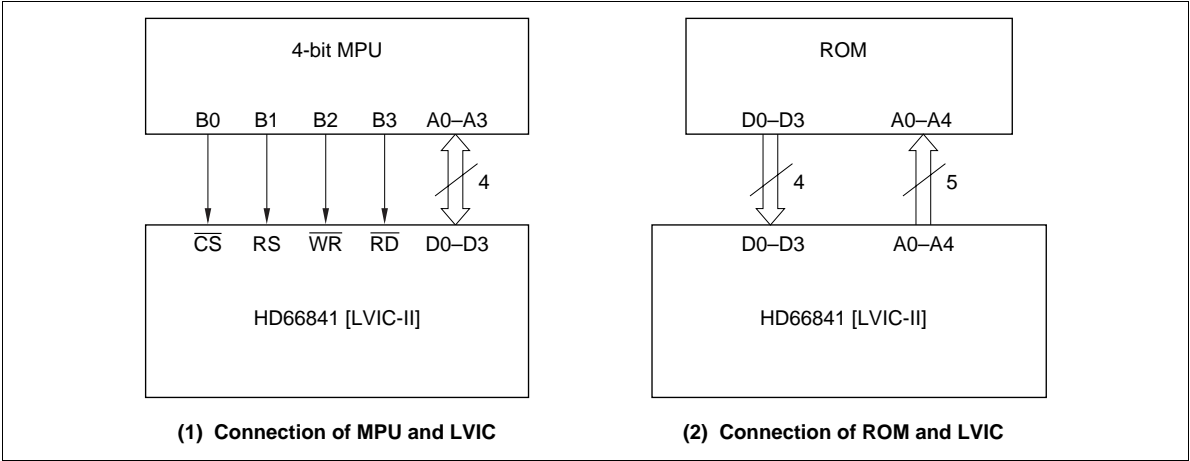
Pin Programming Method: HD66841 mode setting pins control functions in the pin programming method.

Internal Register Programming Method: In the internal register programming method, an MPU or ROM writes data into internal registers to control functions. Figure 3 illustrates the connections of MPU or ROM and the LVIC. Figure 2 (1) is an example of using a 4-bit microprocessor, but since the HD66841 MPU bus is compatible with the 4-MHz 80-family controller bus, it can also be connected directly with the bus of host MPU.

Table 7 Programming Method Selection

Pins		Programming Method
PMOD1	PMOD0	
0	0	Pin programming
0	1	Internal register programming
1	0	
1	1	Prohibited*

Note: * This combination is for a test mode and disables display.



Screen Size

Screen size can be programmed either by pins or internal registers.

In the pin programming method, either 640 dots or 720 dots (80 characters or 90 characters) can be selected with the XDOT pin as the number of horizontal displayed characters, and either 200, 350, 400, 480, 512, or 540 lines can be selected with the YL2–YL0 pins as the number of vertical displayed lines. The number of vertical displayed lines can be adjusted by from +0 to +15 lines with the ADJ and F3–F0 pins.

In the internal register programming method, any even number of characters from 4 to 506 (from 32 to 4048 dots) can be selected with the horizontal displayed characters register (R6, R7), and any even number of lines from 4 to 1028 can be selected with the vertical displayed lines register (R2, R3 and the high-order two bits of R4). However, note that an odd number of lines can also be selected if the screen configuration is single-screen and Y-driver (scan drivers) are positioned on one side of the LCD screen.

The relationship between the LCD screen and the pins and internal registers controlling screen size is shown in Figure 4.

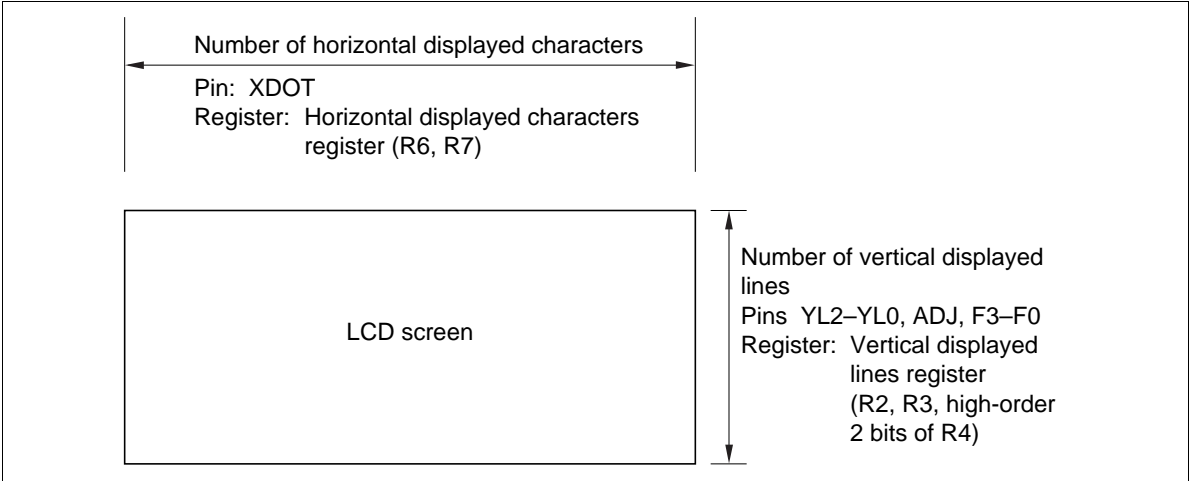


Figure 4 Relationship between LCD Screen and Pins and Internal Registers

Memory Selection

8-, 32-, or 64-kbyte SRAMs can be selected as buffer memory for the HD66841. Since the HD66841 has a chip select circuit for memory, no external decoder is required. The memory type can be selected with the MS1 and MS0 pins or the MS1 and MS0 bits of control register 2 (R1). Memory types and corresponding pin address assignments are listed in Table 8.

The memory capacity required depends on screen size and can be obtained from the following expression:

Memory capacity (bytes) = Nhd × Nvd

Nhd: Number of horizontal displayed characters (where one character consists of 8 horizontal dots)
Nvd: Number of vertical displayed lines

For example, a screen of 640 × 200 dots requires 16-kbytes memory capacity since 80 characters × 200 lines is 16 kbytes. Consequently, each plane requires two HM6264s (8-kbytes memories) in 8-level gray-scale display modes. The MCS0 pin must be connected to the CS pin of one of the memory chips in each plane, and the MCS1 pin must be connected to the CS pin of the remaining memory chip in each plane. (Figure 5 (a))

A screen of 640 × 400 dots requires a 32-kbytes (256-kbit) memory capacity, so each plane requires an HM62256, which is a 32-kbytes memory. In this case, the MCS0 pin must be connected to the CS pin of each memory chip. (Figure 5 (b))

Table 8 Memories and Pin Address Assignments

Pins or Bits		Memory	Address Pins	Chip Select Pins	Address Assignment
MS1	MS0				
0	0	No memory*	—	—	—
0	1	8-kbyte	MA0-MA12	MCS0	\$0000-\$1FFF
				MCS1	\$2000-\$3FFF
				MA13	\$4000-\$5FFF
				MA14	\$6000-\$7FFF
				MA15	\$8000-\$9FFF
1	0	32-kbyte	MA0-MA14	MCS0	\$00000-\$07FFF
				MCS1	\$08000-\$0FFFF
				MA15	\$10000-\$17FFF
1	1	64-kbyte	MA0-MA15	MCS0	\$00000-\$0FFFF
				MCS1	\$10000-\$1FFFF

Note: * There are some limitations if no memory is used. Refer to the User Notes section for details.

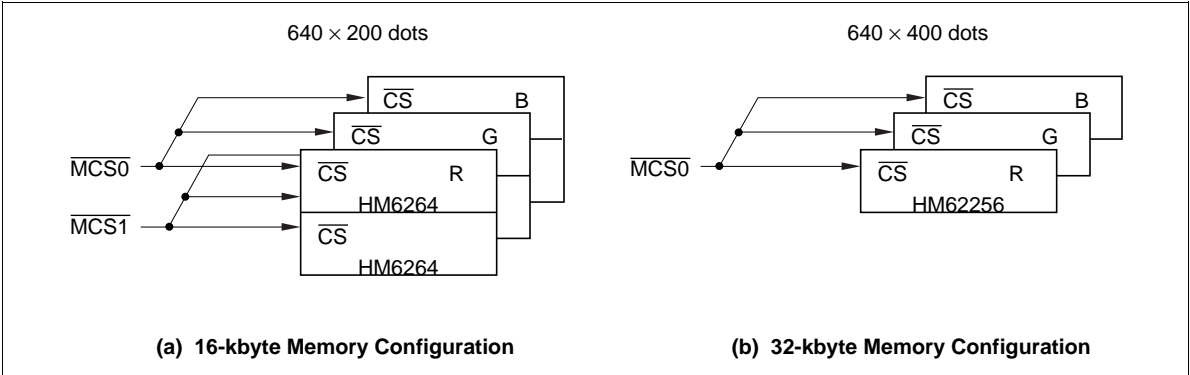


Figure 5 Screen Size and Memories Configuration

Display Modes

The HD66841 supports 16 display modes, depending on the state of the DM3–DM0 pins. The display mode consists of display color, type of LCD data output, how to set LCD drivers around an LCD screen, how to arrange color data (= type of stripes), and how to output M signal (= type of alternating signal). Table 9 lists display modes.

Table 9 Modes List

Mode No.	Pins				Display Color	LCD Data Output		LCD Driver Setting		Stripe* ⁴	Alternating
	DM3	DM2	DM1	DM0		Data Transfer	Screen Config.	X-Driver* ²	Y-Driver* ³		
1	0	0	0	0	Monochrome	4-bits	Dual	One side	One side	—	Every frame
2	0	0	0	1			Single				
3* ¹	0	0	1	0							
4	0	0	1	1		8-bits					
5* ¹	0	1	0	0							
6	0	1	0	1	8-level gray scale	4-bits	Dual	One side			
7	0	1	1	0			Single				
8	0	1	1	1		8-bits					
9* ¹	1	0	0	0	8-color	12-bits (4 bits for R,G,B each)		Both sides	Vertical	Every line	
10* ¹	1	0	0	1							
11* ¹	1	0	1	0							
12* ¹	1	0	1	1							
13* ¹	1	1	0	0							
14* ¹	1	1	0	1							
15* ¹	1	1	1	0			Both sides	One side	Horizontal		
16	1	1	1	1		Dual	One side	One side		Vertical	Every frame

- Notes: 1. For TFT-type LCD
 2. Data output driver
 3. Scan driver
 4. Refer to “Display Color, 8-Color Display”

Display Color

The HD66841 converts the RGB color data normally used for CRT display into monochrome, 8-level gray scale, or 8-color display data.

Monochrome Display (Mode 1 to 5): The HD66841 displays two colors: black (display on) and white (display off). As shown in Table 10, the CRT display RGB data is ORed to determine display on/off.

8-Level Gray Scale Display (Mode 6 to 8): The HD66841 thins out data on certain lines or dots to provide an 8-level gray-scale display based on CRT display color (luminosity). The relationship between CRT display color (luminosity) and LCD gray scale (contrast) is shown in Table 11.

This relationship corresponds to the default values in palette registers; the correspondence between color and gray scale can be changed by writing data into palette registers.

Table 10 Monochrome Display

CRT Display Data				LCD	
R	G	B	CRT Display Color	On/Off	Color
1	1	1	White	On	Black
1	1	0	Yellow	On	Black
0	1	1	Cyan	On	Black
0	1	0	Green	On	Black
1	0	1	Magenta	On	Black
1	0	0	Red	On	Black
0	0	1	Blue	On	Black
0	0	0	Black	Off	White

Table 11 8-Level Gray Scale Display

CRT Display Data			CRT		LCD	
R	G	B	Color	Luminosity	Color	Contrast
1	1	1	White	High	Black	Strong
1	1	0	Yellow			
0	1	1	Cyan			
0	1	0	Green			
1	0	1	Magenta			
1	0	0	Red			
0	0	1	Blue			
0	0	0	Black			
0	0	0	Black	Low	White	Weak

8-Color Display (Mode 9 to 16): The HD66841 displays 8 colors through red (R), green (G), and blue (B) filters placed on liquid-crystal cells. The eight colors are the same as those provided by a CRT display. As shown in Figure 6, 8-color display has two stripe modes: horizontal stripe mode in which the HD66841 arranges RGB data horizontally for horizontal filters and vertical stripe mode in which it arranges RGB data vertically for vertical filters. Three cells express one dot in both modes.

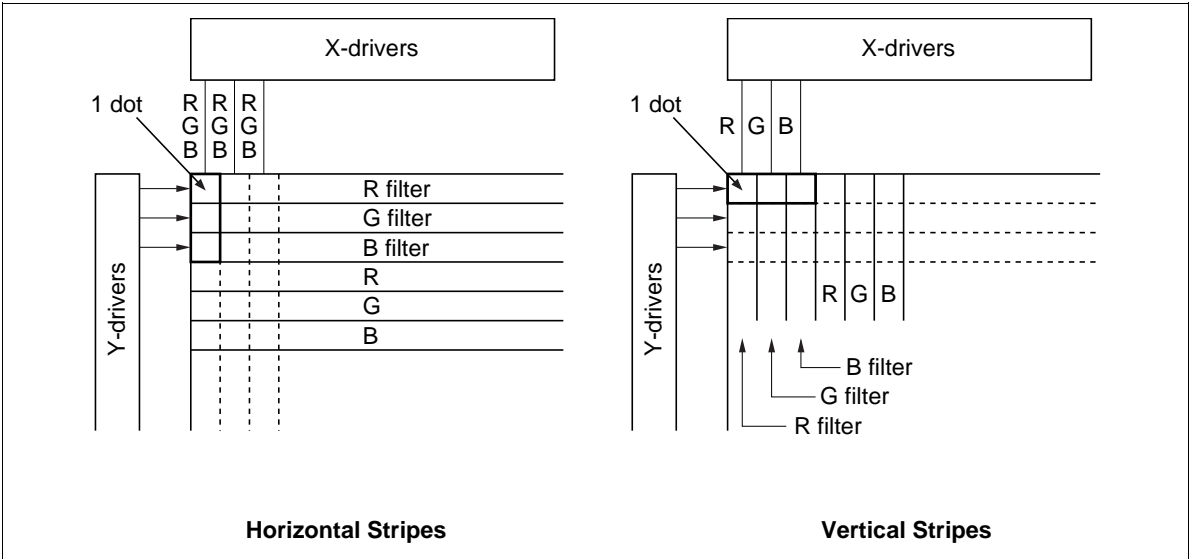


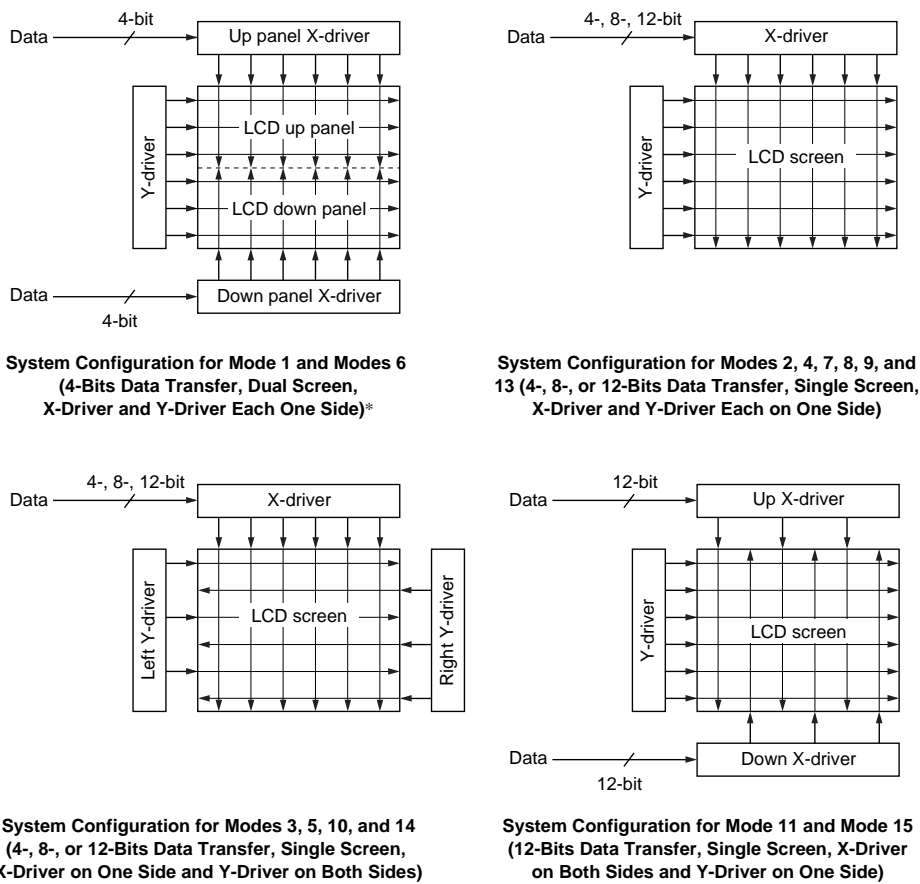
Figure 6 Stripe Modes in 8-Color Display

LCD System Configuration

The LVIC-II supports the following LCD system configurations:

- Types of LCD data output
 - Data transfer: 4-bit, 8-bit, or 12-bits (4 bits each for R, G, and B)
 - Screen configuration: Single or dual
- LCD driver positions around LCD screen
 - X-drivers: On one side or on both sides
 - Y-drivers: On one side or on both sides

System configurations for different modes are shown in Figure 7, and configurations of X- and Y-drivers positioned on both sides an LCD screen are shown in Figure 8.



Note: * Since the LCD upper panel and lower panel are each regarded as one screen, the X-drivers are considered to be positioned on one side, not on both sides.

Figure 7 System Configurations by Mode

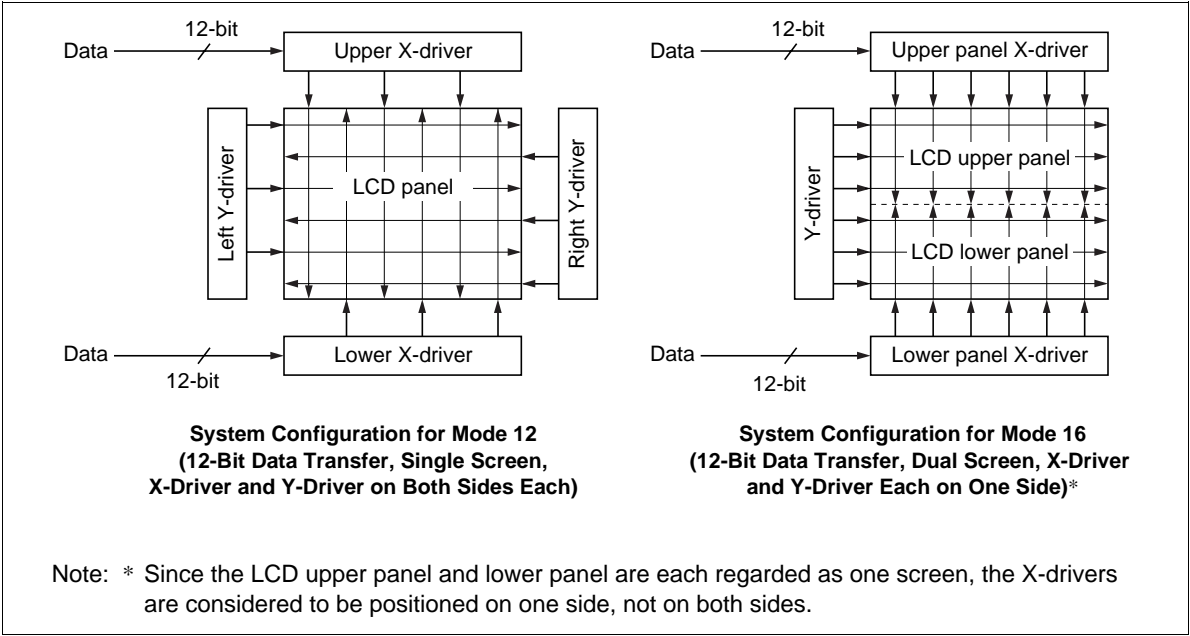


Figure 7 System Configurations by Mode (cont)

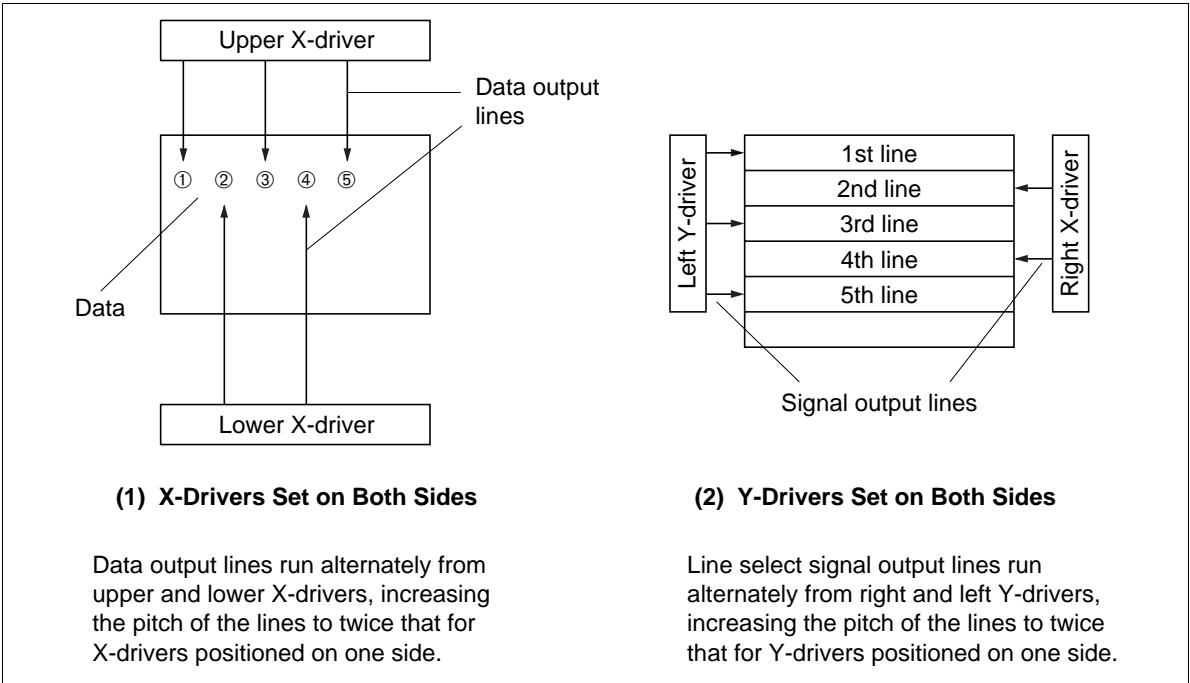


Figure 8 X- and Y-Drivers Set on Both Sides

LDOTCK Frequency Calculation

The frequency f_L of the LCD dot clock (LDOTCK) can be obtained from the following equation:

$$f_L = (Nhd + 6/m) \times 8 \times Nvd \times f_F$$

Nhd: Number of horizontal characters displayed on LCD

Nvd: Number of vertical lines displayed on LCD

m: Parameter which decided by LCD mode

Screen Configuration	Mode No.	m
Dual	1, 6	2
Single	Other modes	1

f_F : FLM frequency

In this case, f_L must satisfy the following relation, where f_D is the frequency of the dot clock for CRT display (DOTCLK):

$$f_L < f_D \times 15/16 \text{ or}$$

$f_L = f_D$ (The phase of LDOTCK must be same to that of DOTCLK when DOTE is high, the phase of LDOTCK must be opposite to that of DOTCLK when DOTE is low. Condition of timing between LDOTCK and DOTCLK must be observed are shown in Figure 9.)

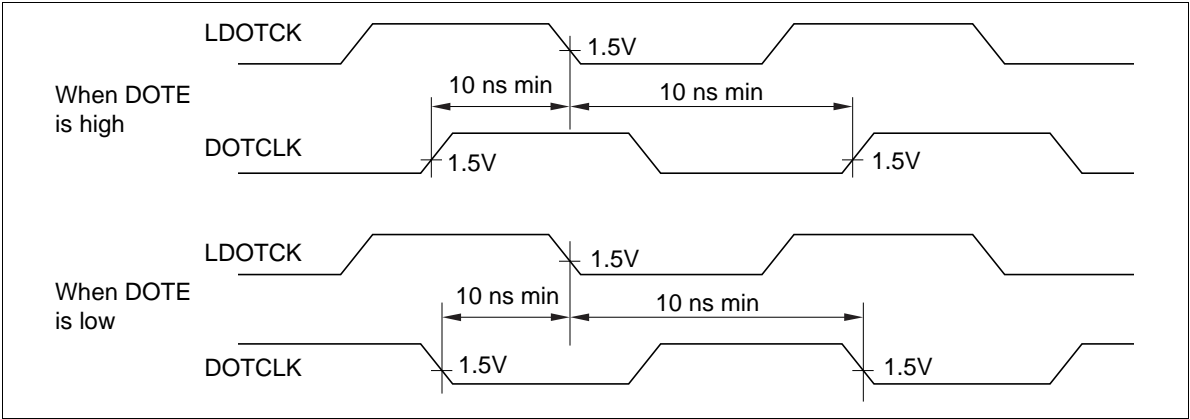


Figure 9 Relationships between DOTE and LDOTCK, DOTCLK

Display Timing Signal Generation

CRT display data is classified into display period data and retrace period data. Only display period data is necessary for LCD. Therefore, the HD66841 needs a signal announcing whether the CRT display data transferred is for the display period or not. This signal is the display timing signal.

The HD66841 can generate the display timing signal from HSYNC and VSYNC. Figure 10 illustrates the relation between HSYNC, VSYNC, the display timing signal (DISPTMG), and display data. Y lines and X dots in the figure are specified by the vertical backporch register (R12, R13) and the horizontal backporch register (R14, R15) respectively.

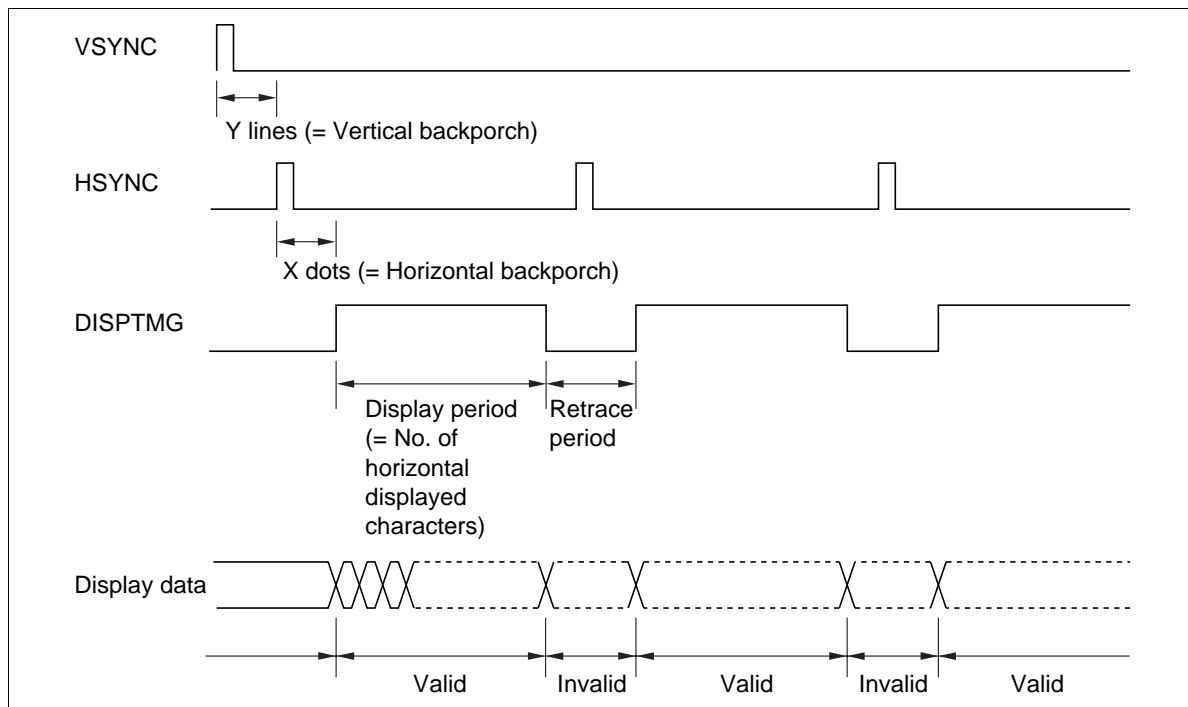


Figure 10 Relation between HSYNC, VSYNC, DISPTMG, and Display Data

Dot Clock Generation

The dot clock, which is a data latch clock, is not a standard video signal, so it is not usually output from the CRT display plug. Therefore, the HD66841 must generate it. The HD66841 has a programmable counter and a phase comparator which are parts of a phase-locked loop (PLL) circuit, and it can generate the dot clock from the HSYNC signal if a charge pump, a low-pass filter (LPF), and a voltage-controlled oscillator (VCO) are externally attached.

A block diagram of the PLL circuit is shown in Figure 11. A PLL circuit is a feedback controller that generates a clock whose frequency and phase are the same as those of a basic clock. The basic clock is the HSYNC signal in this case.

At power-on, the VCO outputs to the programmable counter a signal whose frequency is determined by the voltage at the time. The counter divides the frequency of the signal according to the value in the PLL frequency-dividing ratio register (R10, R11) and outputs it to the phase comparator. This is the frequency-divided clock.

The comparator compares the edges of the clock pulses and the HSYNC signal pulses and output the \overline{CU} or \overline{CD} signal to the charge pump and LPF according to the result. The comparator outputs the \overline{CU} signal if the frequency of the clock is lower than that of the HSYNC signal or if the phase of the clock is behind that of the HSYNC signal; otherwise it outputs the \overline{CD} signal. The charge pump and LPF apply a voltage to the VCO according to the \overline{CU} or \overline{CD} signal.

This operation is repeated until the phase and frequency of the frequency-divided clock match those of the HSYNC signal, making it a stable dot clock.

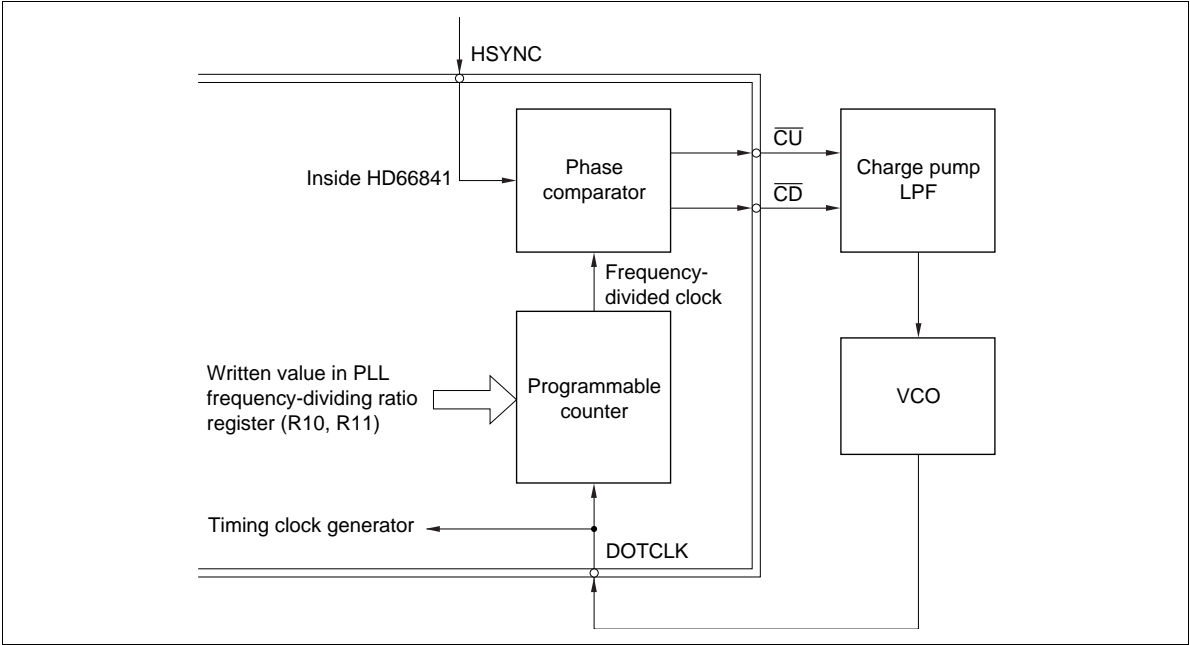


Figure 11 PLL Circuit Block Diagram

Gray-Scale Palette

The HD66841 thins out LCD data on certain dots or lines of an LCD panel every frame, changing integral voltages applied to liquid-crystal cells, to generate intermediate levels of luminosities. Consequently the difference in depth between adjacent gray-scale shades may not be uniform in some cases since voltage-transmittance characteristics vary with different panels. To allow for this, the HD66841 is designed to generate 13 gray-scale levels and provide palette registers that assign desired levels to certain of the eight CRT display colors.

The relationships between gray scales and corresponding effective applied voltages are shown in Figure 12 (a). Each gray scale is displayed according to the characteristics of its effective applied voltage and the optical transmittance of the panel (Figure 12 (b)). Using the palette registers to select any 8 out of 13 levels of applied voltages enables an optimal gray-scale display conforming to the characteristics of the LCD panel. The palette registers can also be used to provide 4-level grayscale display and reverse display.

Table 12 Default Values of Palette Registers

Register No.	CRT Display Data			Register Name	Default Value			
	R	G	B					
P1	0	0	0	Black palette	0	0	0	0
P2	0	0	1	Blue palette	0	0	1	0
P3	1	0	0	Red palette	0	1	0	1
P4	1	0	1	Magenta palette	0	1	1	0
P5	0	1	0	Green palette	0	1	1	1
P6	0	1	1	Cyan palette	1	0	0	0
P7	1	1	0	Yellow palette	1	0	1	0
P8	1	1	1	White palette	1	1	0	0

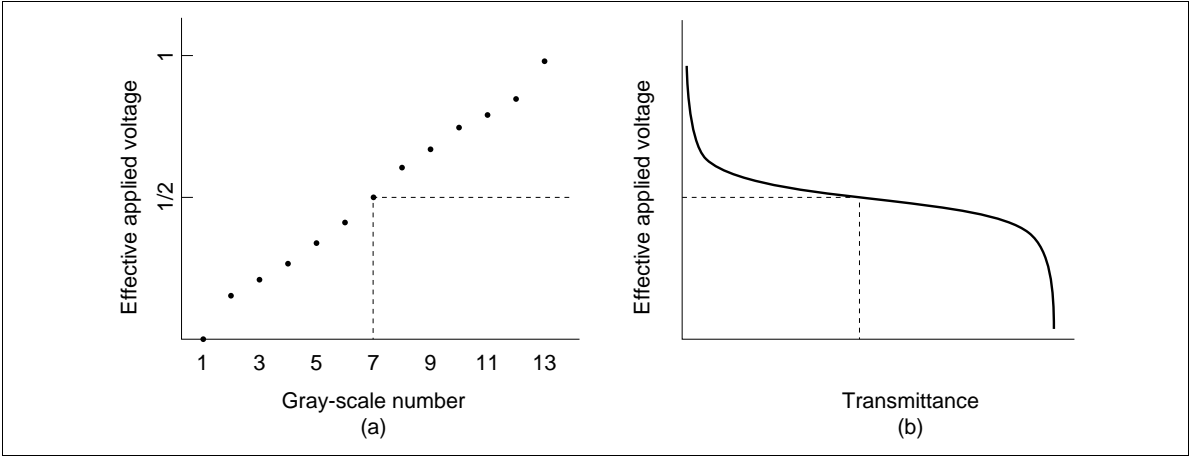


Figure 12 Relationships between Gray Scale, Transmittance, and Effective Applied Voltage

Pin Programming Method

The palette registers cannot be changed from the default value in the pin programming method.

MPU Programming Method

To change the contents of palette registers in the MPU programming method, set bit 2 (the PS bit) of control register 1 (R0), to 1. Since data registers (R1–R15) cannot be accessed while this bit is 1, set in to 0 before accessing the data registers again. However, note that control register 1 (R0) can be accessed regardless of the setting of the PS bit if \$0 is set in the address register (AR).

ROM Programming Method

In the ROM programming method, the HD66841 accesses ROM sequentially from address \$0000 to \$001F. In this case, write 0 to bit 2 of address \$0000 (PS bit) before writing data register values to addresses \$0001–\$000F, and write 1 to bit 2 of address \$0010 (PS bit) before writing palette register values to addresses \$0011–\$0018.

DIZ Function

The HD66841 thins out data on certain lines or dots every frame to enable gray-scale display. If a checker-board pattern consisting of alternately arranged gray scales of different levels (Figure 13) is displayed by a simple dot-basis gray-scale display control method. The display might sometimes seem to “flow” horizontally, depending on the gray-scale and LCD panel characteristics.

The HD66841 automatically checks for such a checker-board section and changes the gray-scale display control method of dot-based data thinning to that of frame-based data thinning, to reduce display flow. Setting bit 3 (DIZ) of control register 1 (R0) to 1 enables this function. In frame-based data thinning, however, flickering might appear with some LCD panels; in that case, select the control method that generates the better display.

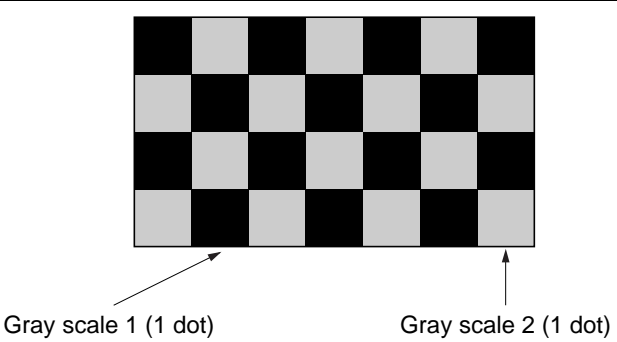


Figure 13 Checker-Board Display

Double-Height Display

The HD66841 provides double-height display which doubles the vertical size of characters and pictures (Figure 14).

In the TN-type LCD modes (display modes 1, 2, 4, and 6–8), the CL3 signal period is half as long as the CL1 signal period, as shown in Figure 15. Consequently, using the CL3 signal instead of the CL1 signal (Figure 16) as a line shift clock enables two lines to be selected while X-drivers (data output drivers) are outputting identical data, thus realizing double-height display. However, it should be noted that this display requires the following procedure since the HD66841 displays twice as many lines as specified by pins or internal registers:

1. Have the LCD dot clock (LDOTCK) frequency calculated from the number of vertical displayed lines of the LCD panel.
2. Specify half the number of vertical displayed lines of the LCD panel as the number of vertical displayed lines. (For instance, if the number of vertical displayed lines of the LCD panel is 400, specify 200 with the YL2–YL0 pins or the vertical displayed lines register.)

This function is available only in the TN-type LCD modes; it is disabled in the TFT-type LCD modes.

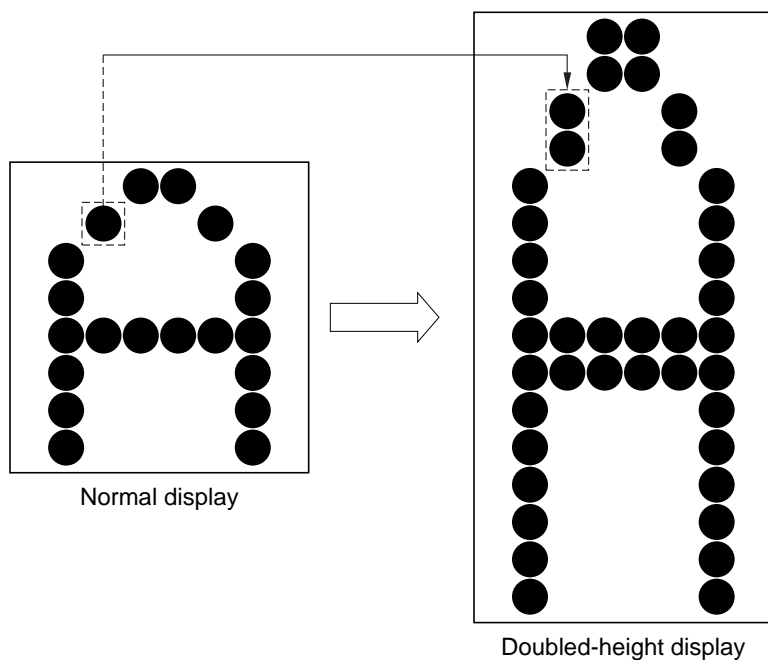


Figure 14 Doubled-Height Display Example

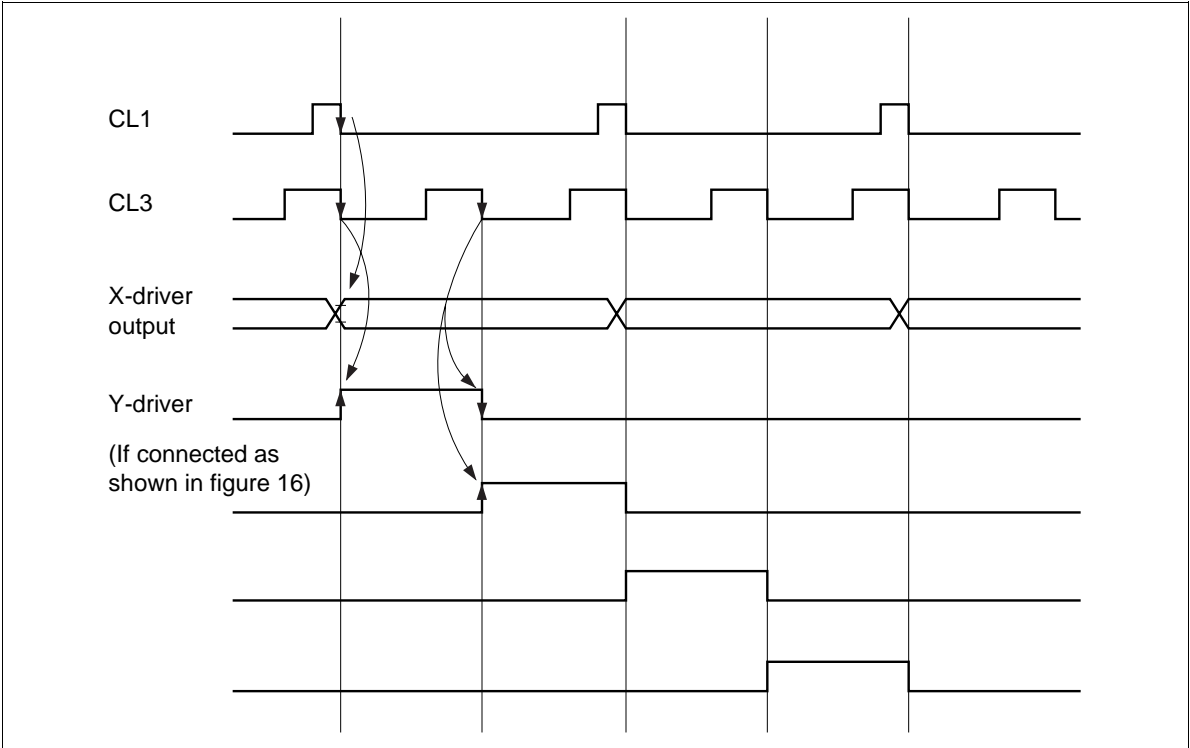


Figure 15 Relationship between CL1 and CL3 in Modes 1, 2, 4, 6, 7, and 8

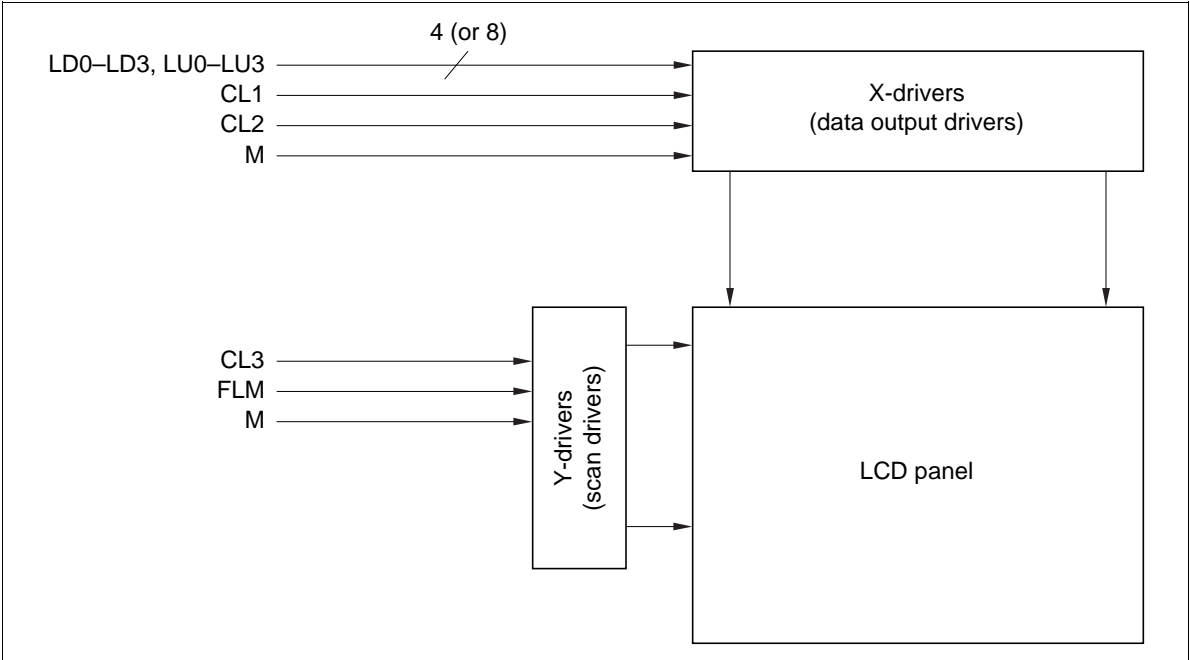


Figure 16 Connection for Double-Height Display

Display Timing Signal Fine Adjustment

If the display timing signal is supplied externally, a phase shift between CRT data and the display timing signal may appear. This is because each signal has its own specific lag. The HD66841 can adjust the display timing signal according to pins F0–F3 or the fine adjust register (R9) to correct the phase shift.

The relationships between pins F3–F0, data bits 3 to 0 of the fine adjust register, and the resultant fine adjustments are shown in Table 13. The polarity of the number of dots adjusted is given by – (minus) indicates advancing the phase of the display timing signal or + (plus) indicating delaying it. Pin F3 or data bit 3 of R9 selects the polarity. The adjustment reference point is the display start position.

Examples of adjusting the display timing signal are shown in Figure 17. Since the signal is two dots ahead of the display start position in case (1), F3, F2, F1, and F0 or data bits 3, 2, 1, and 0 of R9 should be set to (1, 0, 1, 0) to delay the signal by two dots. Conversely, since the signal is two dots behind the display start position in case (2), they should be set to (0, 0, 1, 0) to advance the signal by two dots. If there is no need to adjust the signal, a settings of either (0, 0, 0, 0) or (1, 0, 0, 0) will do.

Table 13 Pins, Data Bits of R9, and Fine Adjustment

Pin:	F3	F2	F1	F0	Number of Dots Adjusted
R9 Bit:	3	2	1	0	
0	0	0	0	0	0
		0	0	1	–1
	
	
	
		1	1	0	–6
1		1	1	1	–7
	0	0	0	0	0
		0	0	1	+1
	
	
	
		1	1	0	+6
		1	1	1	+7

Note: To use pins to adjust the display timing signal, set the ADJ pin to 1.

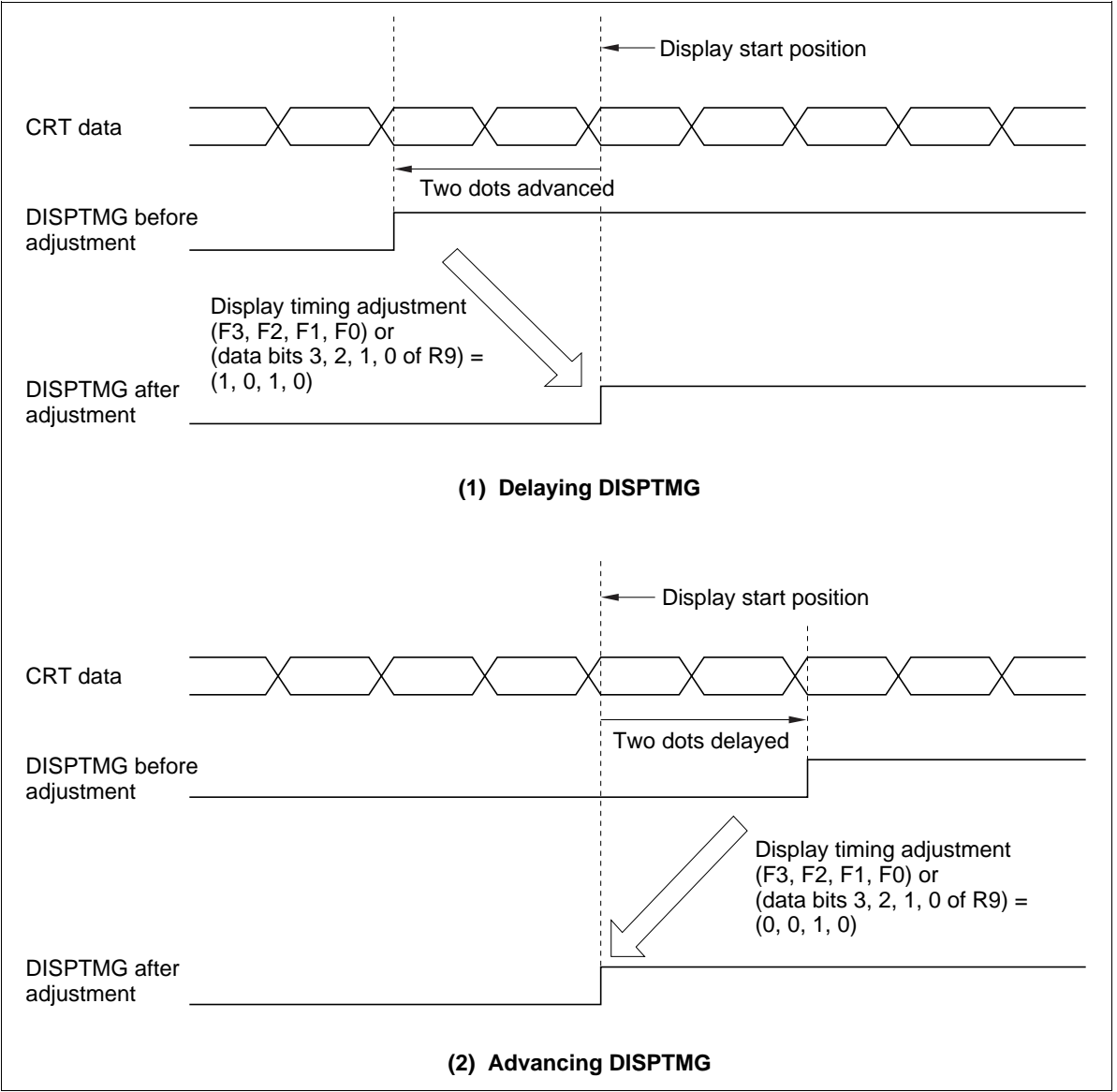


Figure 17 Adjustment of Display Timing Signal

Internal Registers

The HD66841 has an address register (AR) and 16 data registers (R0–R15), HD66841 has 8 palette registers (P1–P8). Write the address of a register to be used into the address register (AR). (HD66841: but only after setting the PS bit of control register 1 (R0) to 0 for a data register or 1 for a palette register.)

The MPU transfers data to the register corresponding to the written address.

Registers are valid only in the internal register programming method, they are invalid (don't care) in the pin programming method.

1. Address Registers (AR)

The address register (Figure 18) is used to select one of the 16 data registers or 8 palette registers. It can select any data register (or palette register) according to the register address written to it by the MPU. The address register itself is selected if the RS signal is set low.

2. Control Registers 1 (R0)

Control register (Figure 19) is composed of 4 bits whose functions are described below. Reading from and writing into invalid bits are possible. However, these operations do not affect the LSI function.

- DCK bit
DCK = 1: The DOTCLK signal generated internally.
DCK = 0: The DOTCLK signal is supplied externally.
- DSP bit
DSP = 1: The DISPTMG signal is generated internally.
DCK = 0: The DSPTMG signal is supplied externally. (However, note that if DCK is 1, the DISPTMG signal is generated internally even if DSP is 0.)

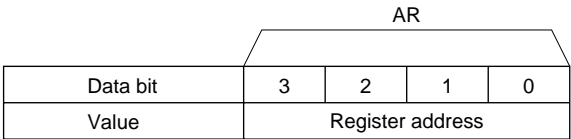


Figure 18 Address Register

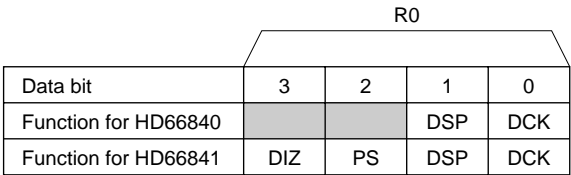


Figure 19 Control Register 1

- PS bit
Specifies access to data registers (R0–R15) or palette registers (P1–P8).
 - In MPU programming mode
 - PS = 0: Specifies access to data registers (R0–R15)
 - PS = 1: Specifies access to palette registers (P1–P8)
 - This register can be always accessed regardless of the PS bit setting, but it cannot be read after the PS bit is set to 1. Read it when PS is 0.
 - In ROM programming mode
 - Data for HD66841 internal data registers can be written into \$0001 to \$000F when bit 2 (the PS bit) of \$0000 is set to 0. Data be set into palette registers can be written into \$0011 to \$0018 when the PS bit of \$0010 is set to 1 (Figure 20).
- DIZ bit
Changes the method used to control the gray-scale display of a checker-board pattern.
 - DIZ = 0: Data thinned out on a dot basis every frame
 - DIZ = 1: Data thinned out on a frame basis every frame

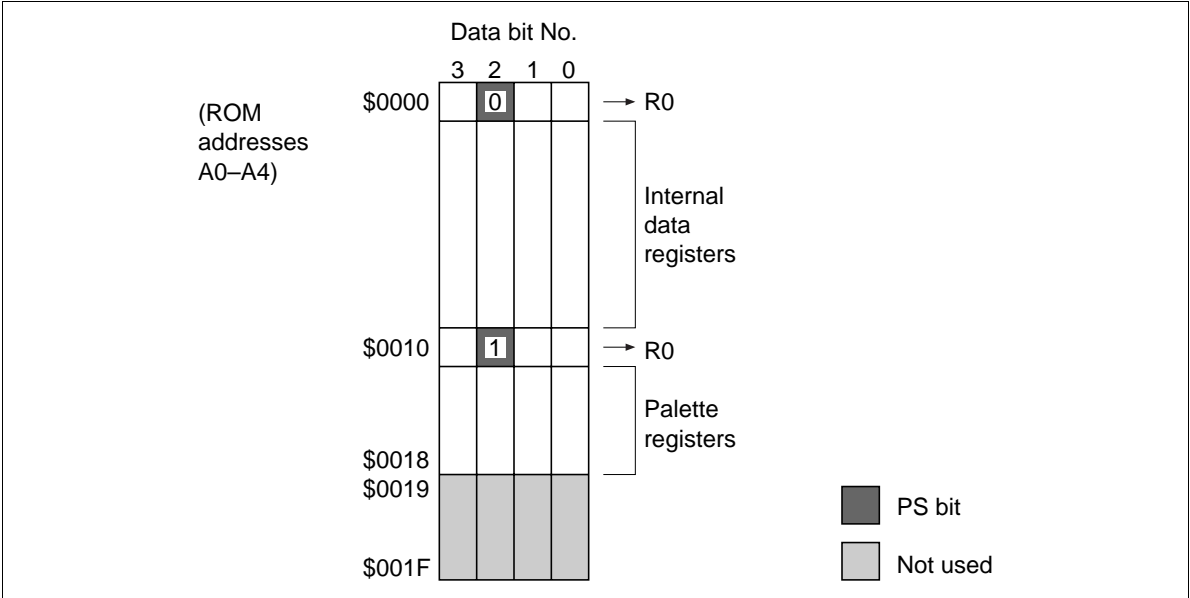


Figure 20 PS Bit Functions in ROM Programming Method

3. Control Register 2 (R1)

Control register 2 (Figure 21) is composed of four bits whose functions are described below.

- MC bit
Specifies M signal alternation.
MC = 1: The M signal alternates every line.
MC = 0: The M signal alternates every frame.
- DON bit
Specifies whether the LCD is on or off.
DON = 1: LCD on
DON = 0: LCD off
- MS1, MS0 bits
Specify buffer memory type.
(MS1, MS0) = (0, 0): No memory
(MS1, MS0) = (0, 1): 8-kbytes memory
(MS1, MS0) = (1, 0): 32-kbytes memory
(MS1, MS0) = (1, 1): 64-kbytes memory

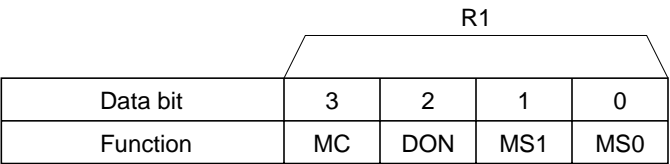


Figure 21 Control Register 2

4. Vertical Displayed Lines Register (R2, R3, High-Order 2 Bits of R4)

The vertical displayed lines register (Figure 22) is composed of ten bits (R2, R3, and the high-order two bits of R4). It specifies the number of lines displayed from top to bottom of the screen, called the number of vertical displayed lines. This register can specify both even and odd numbers in single screen modes with Y-drivers positioned on one side, i.e., in display modes 2, 4, and 7-9, but can specify only even numbers in other modes. The value to be written into this register is $Nvd - 1$, where Nvd is the number of vertical displayed lines.

5. CL3 Period Register (Low-Order 2 Bits of R4, R5)

The CL3 period register (Figure 22), is composed of six bits (R5 and the low-order two bits of R4). It specifies the CL3 signal period in 8-color display modes with horizontal stripes (display modes 13–15), so it is invalid in other modes. CL3 is the clock signal used by the HD66841 to output RGB data separately to LCD drivers. The value to be written into this register is $Npc - 1$, i.e., $(Nhd + 6) \times 1/3 - 1$, where Nhd is the number of horizontal displayed dots $\times 1/8$. If $(Nhd + 6)$ is not divisible by 3, rounded it off.

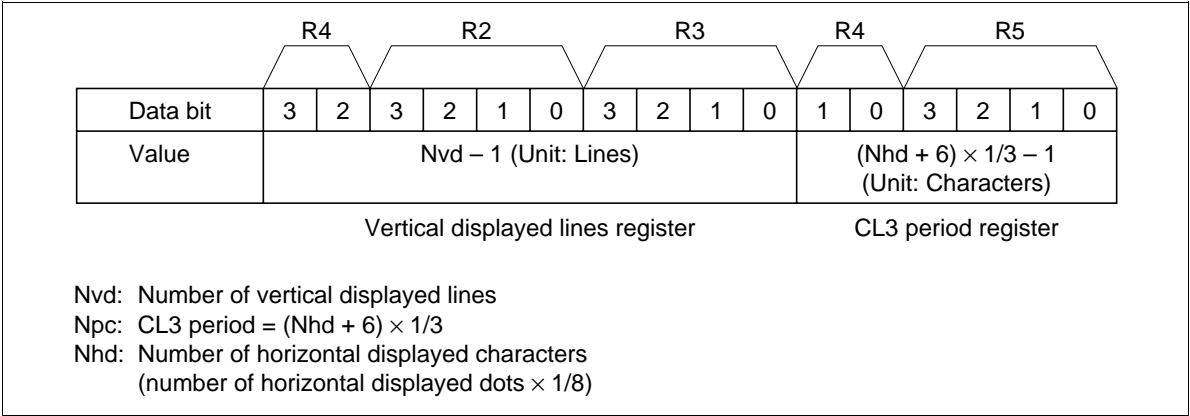


Figure 22 Vertical Displayed Lines Register and CL3 Period Register

6. Horizontal Displayed Characters Register (R6, R7)

The horizontal displayed characters register (Figure 23) is composed of eight bits (R6, R7). It specifies the number of characters displayed on one horizontal line, called the number of horizontal line, called the number of horizontal displayed characters.

This register can specify even numbers only. In dual-screen modes (display modes 1, 6, and 16), the most significant bit of this register is invalid. When writing into this register, shift (Nhd - 1) in the low-order direction for one bit to cut off the least significant bit. Figure 24 shows how to write a value into the register when Nhd = 90.

7. CL3 Pulse Width Register (R8)

The 4-bit CL3 pulse width register (Figure 25) specifies the high-level pulse width of the CL3 signal. In TFT-type LCD modes, a data hold time is necessary and it is determined by the high-level pulse width of the CL3 signal. The CL3 signal is output with the high-level pulse width specified by this register even when the HD66841 is not in a TFT-type LCD mode.

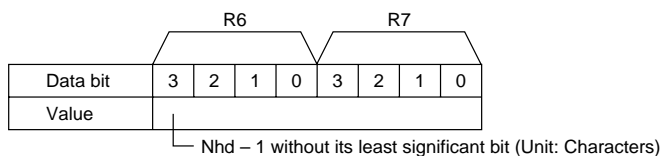


Figure 23 Horizontal Displayed Characters Register

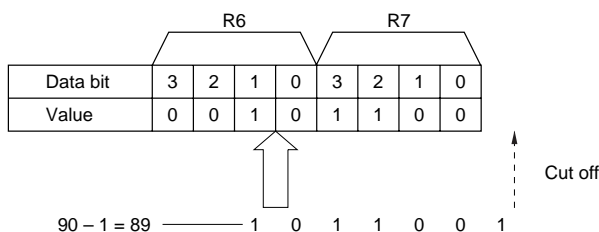
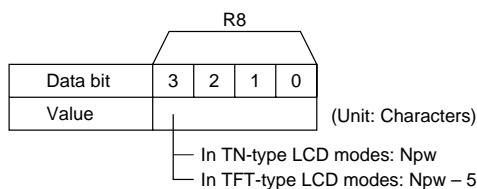


Figure 24 How to Write the Number of Horizontal Displayed Characters



Npw: High-level pulse width of the CL3 signal
(number of dots while the CL3 signal is high $\times 1/8$)

Figure 25 CL3 Pulse Width Register

8. Fine Adjust Register (R9)

The 4-bit fine adjust register (Figure 26) adjusts the externally supplied display timing signal (DISPTMG) to synchronize its phase with that of LCD data. The value to be written into this register depends on the interval between the rising edge of the DISPTMG signal and the display start position. For more details, refer to the Display Timing Signal Fine Adjustment section and Table 13. This register is invalid if the DISPTMG signal is generated internally, that is, if either the DCK bit or the DSP bit of control register 1 (R0) is 1.

9. PLL Frequency-Division Ratio Register (R10, R11)

The 8-bit PLL frequency-dividing ratio register (Figure 27) specifies the PLL frequency-division ratio used for generating dot clock pulses by a PLL circuit. The PLL frequency-division ratio is the ratio of the DOTCLK signal's frequency to the horizontal synchronization signal's (HSYNC) frequency. The LVIC-II generates the DOTCLK signal according to this ratio. This register is invalid if the DOTCLK signal is supplied externally, i.e., it is valid only in the internal register programming method when the DCK bit of control register 1 (R0) is 0.

The value to be written into this register is $N_{PLL} - 731$, where N_{PLL} is the PLL frequency-division ratio which can be obtained from the following expression:

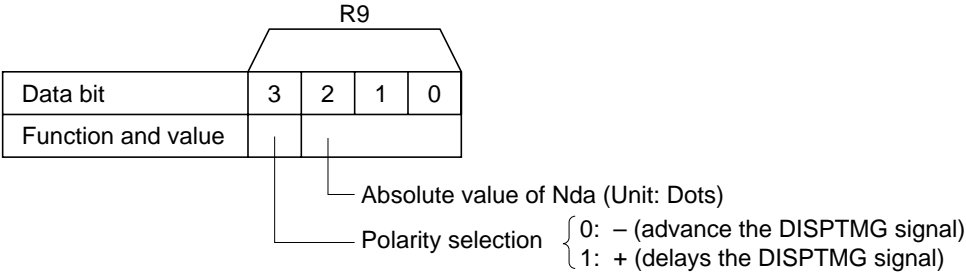
$$N_{PLL} - 731 = N_{cht} \times n - 731$$

Ncht: Total number of horizontal characters on CRT (total number of horizontal dots on CRT \times 1/n)

n: Horizontal character pitch (number of horizontal dots making up a character)

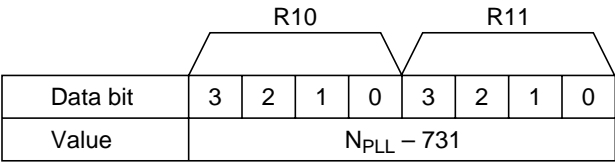
Ncht can be also obtained from the CRT monitor specifications as follows:

$$N_{cht} = 1/n \times (\text{DOTCLK frequency} / \text{HSYNC frequency})$$



Nda: Number of dots adjusted

Figure 26 Fine Adjust Register



N_{PLL} : PLL frequency-division ratio = DOTCLK frequency/HSYNC frequency

Figure 27 PLL Frequency-Division Ratio Register

10. Vertical Backporch Register (R12, R13)

The 8-bit vertical backporch register (Figure 28) specifies the vertical backporch which is the number of lines between the active edge of the vertical synchronization signal (VSYNC) and the rising edge of the display timing signal (DISPTMG), if the DISPTMG signal is generated internally. For details on the vertical backporch, refer to the Display Timing Signal Generation section and Figure 10.

This register is invalid if the DISPTMG signal is supplied externally. It is valid only in the internal register programming method when the DSP bit of control register 1 (R0) is 1. However, note that if the DCK bit of control register 1 (R0) is 1, the DISPTMG signal will always be regenerated internally so this register is enabled even if the DSP bit of control register 1 (R0) is 0.

11. Horizontal Backporch Register (R14, R15)

The 8-bit horizontal backporch register (Figure 29) specifies the horizontal backporch which is the number of dots between the rising edge of the HSYNC signal and that of the display timing signal (DISPTMG), if the DISPTMG signal is generated internally. For details on the horizontal backporch, refer to Display Timing Signal Generations section and Figure 10.

This register is invalid if the DISPTMG signal is supplied externally. It is valid only in the internal register programming method when the DSP bit of control register 1 (R0) is 1. However, note that if the DCK bit of control register 1 (R0) is 1, the DISPTMG signal will always be generated internally so this register is enabled even if the DSP bit of control register 1 (R0) is 0.

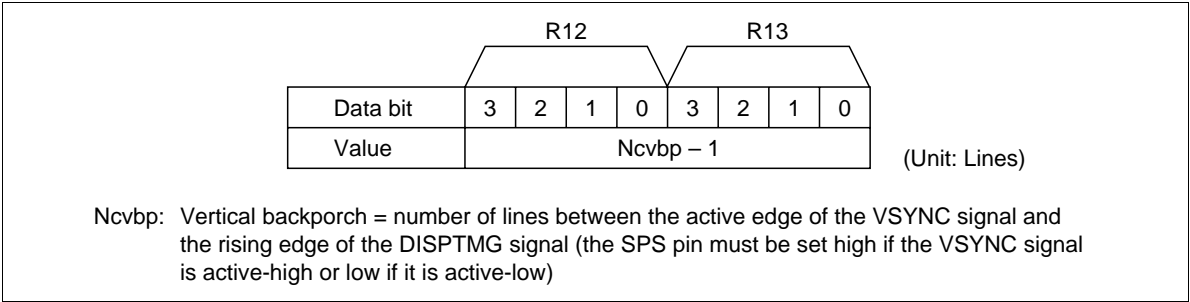


Figure 28 Vertical Backporch Register

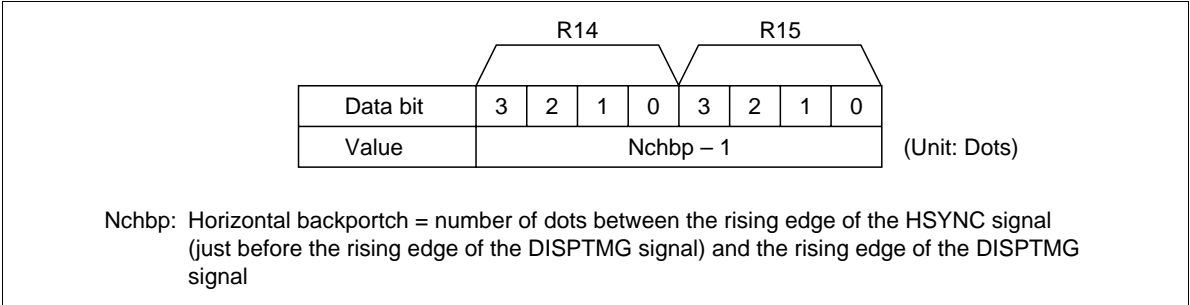


Figure 29 Horizontal Backporch Register

12. Palette Registers (P1–P8)

The eight 4-bit palette registers (Figure 30) each specify one of 13 gray-scale levels for one of the eight colors provided by RGB signals. Use these registers to enable an 8-level gray-scale display appropriate to the characteristics of the LCD panel.

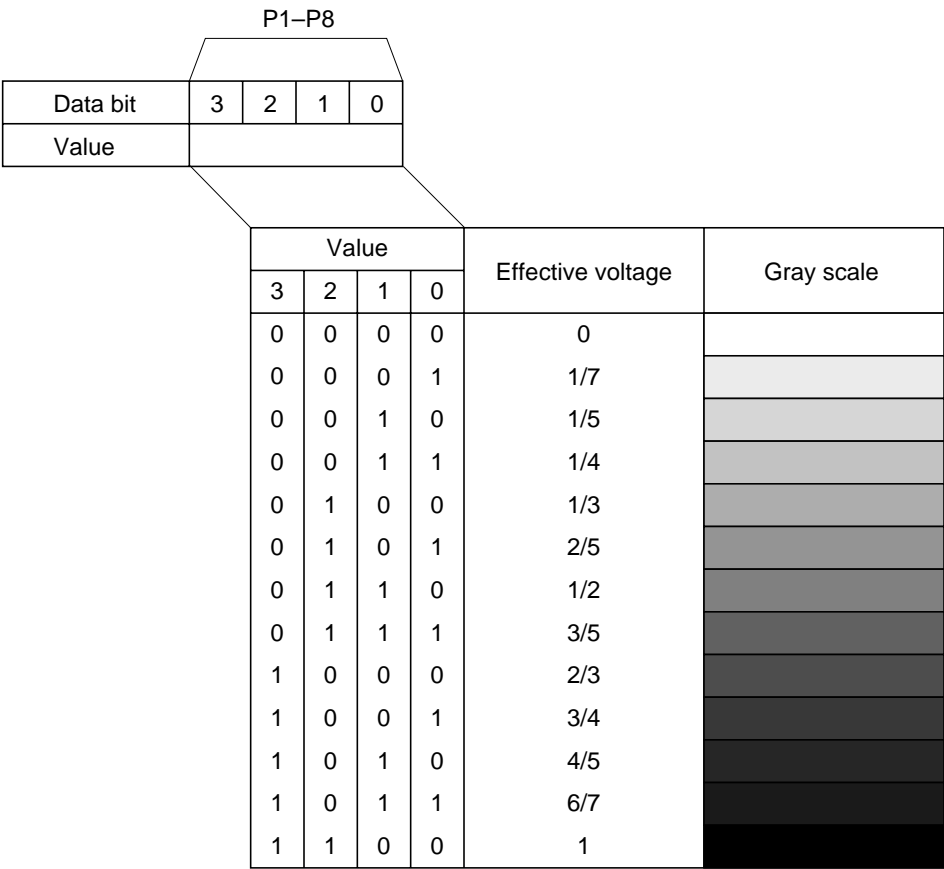


Figure 30 Palette Registers

Reset

The $\overline{\text{RES}}$ signal resets and starts the LVIC-II. The reset signal must be held low for at least 1 μs after power-on.

Reset is defined as shown in Figure 31.

State of Pins after Reset

In principle, the $\overline{\text{RES}}$ signal does not control output signals and it operates regardless of other input signals. Output signals can be classified into the following five groups, depending on their reset states:

- Retains pre-reset state: CL2, A0–A4
- Driven to high-impedance state (or fixed low if no memory is used): RD0–RD7, GD0–GD7, BD0–BD7
- Fixed high: $\overline{\text{MWE}}$, CL4, M, $\overline{\text{CU}}$, $\overline{\text{CD}}$, $\overline{\text{MCS1}}$
- Fixed low: MA0–MA12, R0–R3, G0–G3, B0–B3, CL3, FLM
- Fixed high or low, depending on the memory used (Table 14): MA13–MA15, $\overline{\text{MCS0}}$

State of Registers after Reset

The $\overline{\text{RES}}$ signal does not affect data register contents, so the MPU can both read from and write to data registers, even after reset. Registers will retain their pre-reset contents until they are rewritten.

The HD66841's palette registers, are usually set to their default values by a reset. For the default values, refer to the Gray-Scale Palette section and Table 12.

Memory Clear Function

After a reset, the HD66841 writes 0s in the memory area specified by pins or register bits MS0 and MS1 (Table 8).

Table 14 State of Pins after Reset and Memory Type

Memory Type	MA13	MA14	MA15	MCS0
No memory	Low	Low	High	High
8-kbytes memory	High	High	High	Low
32-kbytes memory	Low	Low	High	Low
64-kbytes memory	Low	Low	Low	Low

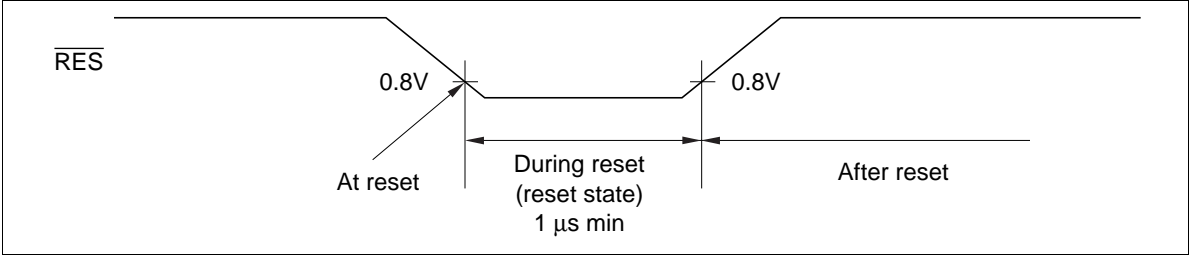


Figure 31 Reset Definition

User Notes

1. The following limitations are imposed if no memory is used ($MS = 0$, $MS1 = 0$).
 - a. Dual-screen display modes are disabled.
(modes 1, 6 and 16)
 - b. LCD systems with Y-drivers on both sides are disabled, even if a mode for system with Y-drivers on both sides is selected.
(modes 3, 5, 10, 12, or 14)
The HD66841 operates in exactly the same way as in the corresponding mode for a system with Y-drivers on one side.
(modes 2, 4, 9, 11, or 13)
The CL4 pin must be left disconnected in this case.
2. With the internal register programming method, the operation of the HD66841 after a reset cannot be guaranteed until its internal registers have been written to.
3. The memory clear function might not work normally at power-on or after a reset if the MS0 and MS1 pins or bits are not set correctly to the value corresponding to the type memory being used.
4. Since the HD66841 are a CMOS LSI, input pins must not be left disconnected. Refer to the Pin Description and Table 1 for details on pin handling.

Programming

The values written in internal registers have the limits listed in Table 15. The symbols in the table are defined as shown in Table 16 and Figure 32.

Table 15 Limits on Register Values

Item	Limits	Notes	Applicable Registers
Screen configuration	$4 \leq Nvd \leq (Ncvbp + Ncvsp) - 1 \leq 1024$ $4 \leq Nhd \leq (Nchbp \times 1/n + Nchsp) - 1 \leq 506$	1, 2	R2, R3, R4, R6, R7
	$(Nhd + 6) \times n \times Nvd \times f_{FLM} \leq f_{DOTCLK} \leq 30 \text{ MHz}$	1, 3	R2, R3, R4, R6, R7
CL3 signal control	$1 \leq Npw \leq (Nhd + 6)/2 - 1$	4	R4, R5, R6, R7, R8
	$1 \leq Npw \leq Nhd$	5	
	$1 \leq Npw \leq Npc - 1$	6	
	$Npc \leq (Nhd + 6)/2 - 1$		
DISPTMG signal generation	$1 \leq Nchbp \leq 256$	7	R12, R13
	$1 \leq Ncvbp \leq 256$	7	R13, R15
No memory	$4 \leq Nhd \leq Nchsp - 4$	8	R2, R3, R4
	$4 \leq Nvd \leq Ncvsp - 1$	8	R6, R7

- Notes:
1. Lowercase n indicates the horizontal character pitch which is the number of horizontal dots composing a character.
 2. $Nhd \leq 250$ in the dual screen modes (display modes 1, 6, and 16).
 3. f_{FLM} is the FLM signal frequency and f_{DOTCLK} is the CRT display dot clock (DOTCLK) frequency.
 $f_{LDOTCK} < f_{DOTCLK} \times 15/16$ or $f_{LDOTCK} = f_{DOTCLK}$
 $(f_{LDOTCK}$ is the LCD dot clock (LDOTCK) frequency)
 4. In display modes 1, 2, 4, and 6–8
 5. In display modes 3, 5, and 9–12 when $Npw = (\text{value in R8}) + 5$
 6. In display modes 13–15 when $Npw = (\text{value in R8}) + 5$
 7. $(\text{Value in R14 and R15}) \leq (Nchsp \times n + Nchbp) - Nhd \times n - 2$
 $(n = \text{horizontal character pitch})$
 $(\text{Value in R12 and R13}) \leq (Ncvsp + Ncvbp) - Nvd - 2$
 8. $Nht = Nchsp + (Nchbp \times 1/n)$, $Nvd < Ncvbp + Ncvsp$
 $(Nht = (Nhd + 6) \text{ if buffer memory is used})$
 $(n = \text{horizontal character pitch})$

Table 16 Symbol Definitions

Symbol	Definition
Nchd	Number of horizontal displayed characters on the CRT display (number of horizontal displayed dots on the CRT display $\times 1/8$)
Nchsp	Number of characters between the rising edge of the DISPTMG signal and that of the HSYNC signal (number of dots between the rising edge of the DISPTMG signal and that of the HSYNC signal $\times 1/8$) (= horizontal synchronization position)
Nchbp	Number of dots between the rising edge of the HSYNC signal and that of the DISPTMG signal (just after the rising edge of the HSYNC signal) (= horizontal backporch)
Ncvbp	Number of lines between the active edge of the VSYNC signal and the rising edge of the DISPTMG signal (just after the active edge of the VSYNC signal) (= vertical backporch)
Ncvsp	Number of lines between the rising edge of the DISPTMG signal and the active edge of the VSYNC signal (= vertical synch position)
Ncvd	Number of vertical displayed lines on the CRT display
Nhd	Number of horizontal displayed characters on the LCD (number of horizontal displayed dots on the LCD $\times 1/8$)
Npc	Number of characters during one CL3 signal period (number of dots during one CL3 signal period $\times 1/8$)
Npw	Number of characters while the CL3 signal is high (number of dots while the CL3 signal is high $\times 1/8$)
Nht	Number of characters during a CN1 signal period (number of dots during a CL1 signal period $\times 1/8$)
Nvd	Number of vertical displayed lines on the LCD

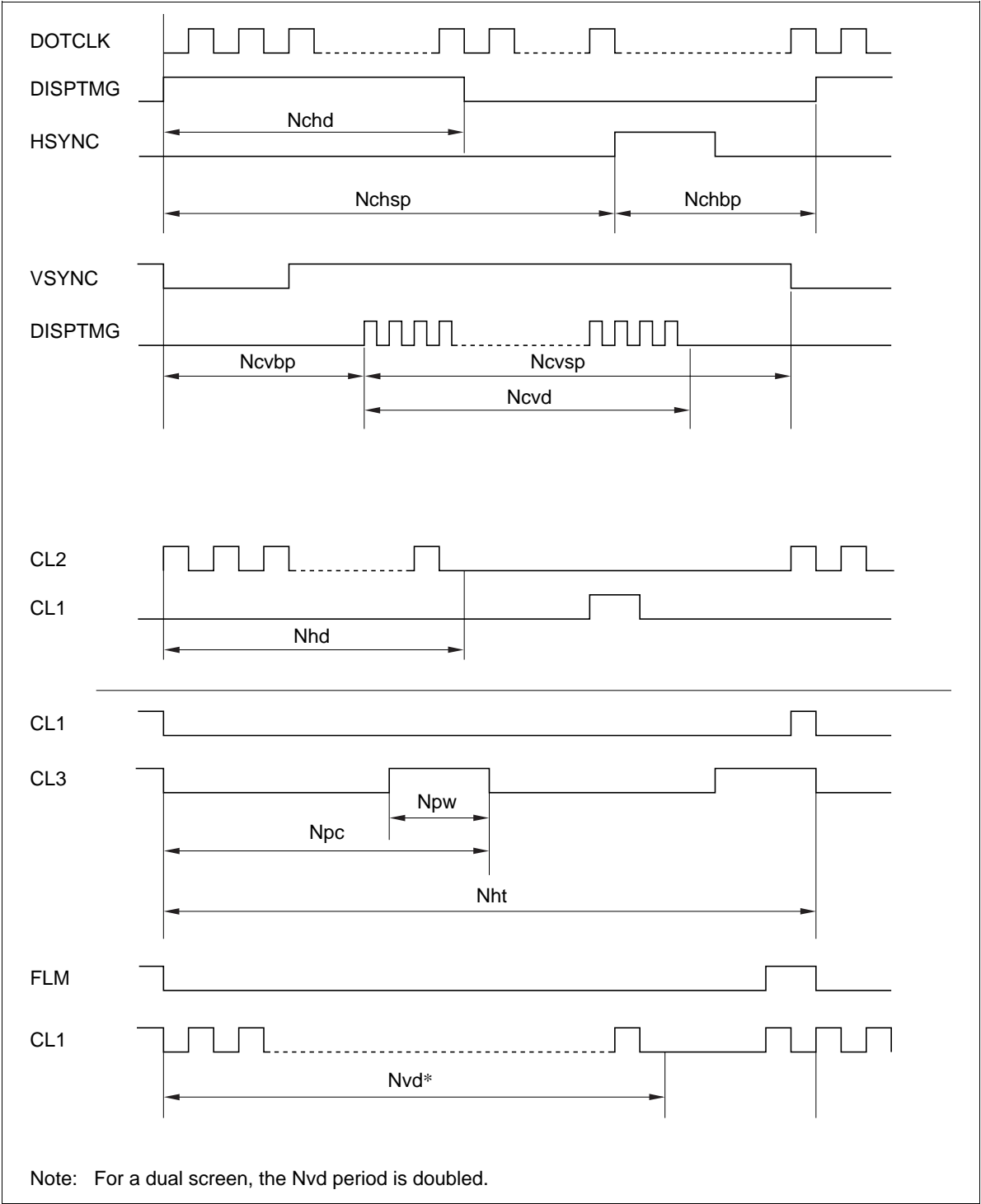


Figure 32 Symbol Definitions

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{in}	−0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	−20 to +75	°C
Storage temperature	T_{stg}	−55 to +125	°C

- Notes:
1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions ($V_{CC} = 5.0V \pm 10\%$, $GND = 0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$). If these conditions are exceeded, it could affect reliability of the LSI.
 2. All voltages are referenced to $GND = 0V$.

Electrical Characteristics

DC Characteristics ($V_{CC} = 5.0V \pm 10\%$, $GND = 0V$, $T_a = -20^\circ C$ to $+75^\circ C$, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Condition
Input high voltage	\overline{RES}	V_{IH}	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V	
	TTL interface* ¹		2.0	$V_{CC} + 0.3$		
	TTL interface* ⁴		2.2	$V_{CC} + 0.3$		
	CMOS interface* ¹		$0.7 V_{CC}$	$V_{CC} + 0.3$		
Input low voltage	TTL interface* ¹ , \overline{RES}	V_{IL}	-0.3	0.8	V	
	TTL interface* ⁵		-0.3	0.6		
	CMOS interface* ¹		-0.3	$0.3 V_{CC}$		
Output high voltage	TTL interface* ²	V_{OH}	2.4	—	V	$I_{OH} = -200 \mu A$
	CMOS interface* ²		$V_{CC} - 0.8$	—		$I_{OH} = -200 \mu A$
Output low voltage	TTL interface* ²	V_{OL}	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$
	CMOS interface* ²		—	0.8		$I_{OL} = 200 \mu A$
Input leakage current	All inputs except I/O common pins* ³	I_{IL}	-2.5	2.5	μA	
Three state (off-state) leakage current	I/O common pins* ³	I_{TSL}	-10.0	10.0	μA	
Current consumption	—	I_{CC}	—	250	mW	$f_{DOTCLK} = 30 \text{ MHz}$ Output pins left disconnected

- Notes: 1. TTL interface inputs: R, G, B, HSYNC, VSYNC, DISPTMG, RD0–RD7, GD0–GD7, BD0–BD7, D0–D3, A0/ \overline{RD} /XDOT, \overline{RS} /ADJ/A4, \overline{CS} /MS0
CMOS interface inputs: DM0–DM3, DOTE, PMOD0, PMD1, A1/YL0–A2/YL2
2. TTL interface outputs: A0/ \overline{RD} /XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7, MA0–MA15, \overline{MCS} 0, \overline{MCS} 1, \overline{MWE} , \overline{RS} /ADJ/A4
CMOS interface outputs: \overline{CU} , \overline{CD} , R0/LU0–R3/LU3, G0/LD0–G3/LD3, B0–B3, M, FLM, CL1, CL2, CL3, CL4
3. I/O common pins: A0/ \overline{RD} /XDOT, A1/YL0–A3/YL2, D0–D3, RD0–RD7, GD0–GD7, BD0–BD7
Inputs except I/O common pins: HSYNC, VSYNC, PMOD0, PMOD1, \overline{RS} /ADJ, \overline{CS} /MS0, \overline{WR} /MS1, \overline{RES} , DOTE, DM0–DM3, LDOTCK, DOTCLK, R, G, B, DISPTMG
4. TTL interface: \overline{WR} /MS1, LDOTCK, DOTCLK
5. TTL interface: \overline{WR} /MS1

AC Characteristics ($V_{CC} = 5.0V \pm 10\%$, $GND = 0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$)

Video Signal Interface

Item	Symbol	Min	Max	Unit	Remark
DOTCLK cycle time	t_{CYCD}	33	1000	ns	
DOTCLK high-level pulse width	t_{WDH}	16.5	—	ns	
DOTCLK low-level pulse width	t_{WDL}	16.5	—	ns	
DOTCLK rise time	t_{Dr1}	—	5	ns	
DOTCLK fall time	t_{Df1}	—	5	ns	
RGB setup time	t_{VDS}	10	—	ns	
RGB hold time	t_{VDH}	10	—	ns	
DISPTMG setup time	t_{DTS}	10	—	ns	
DISPTMG hold time	t_{DTH}	10	—	ns	
HSYNC setup time	t_{HSS}	10	—	ns	
HSYNC hold time	t_{HSH}	10	—	ns	
Phase shift setup time	t_{PDS}	$2 t_{CYCD}$	—	ns	
Phase shift hold time	t_{PDH}	$2 t_{CYCD}$	—	ns	
Input signal rise time	t_{Dr2}	—	10	ns	Figure 33 except for DOTCLK
Input signal fall time	t_{Df2}	—	10	ns	

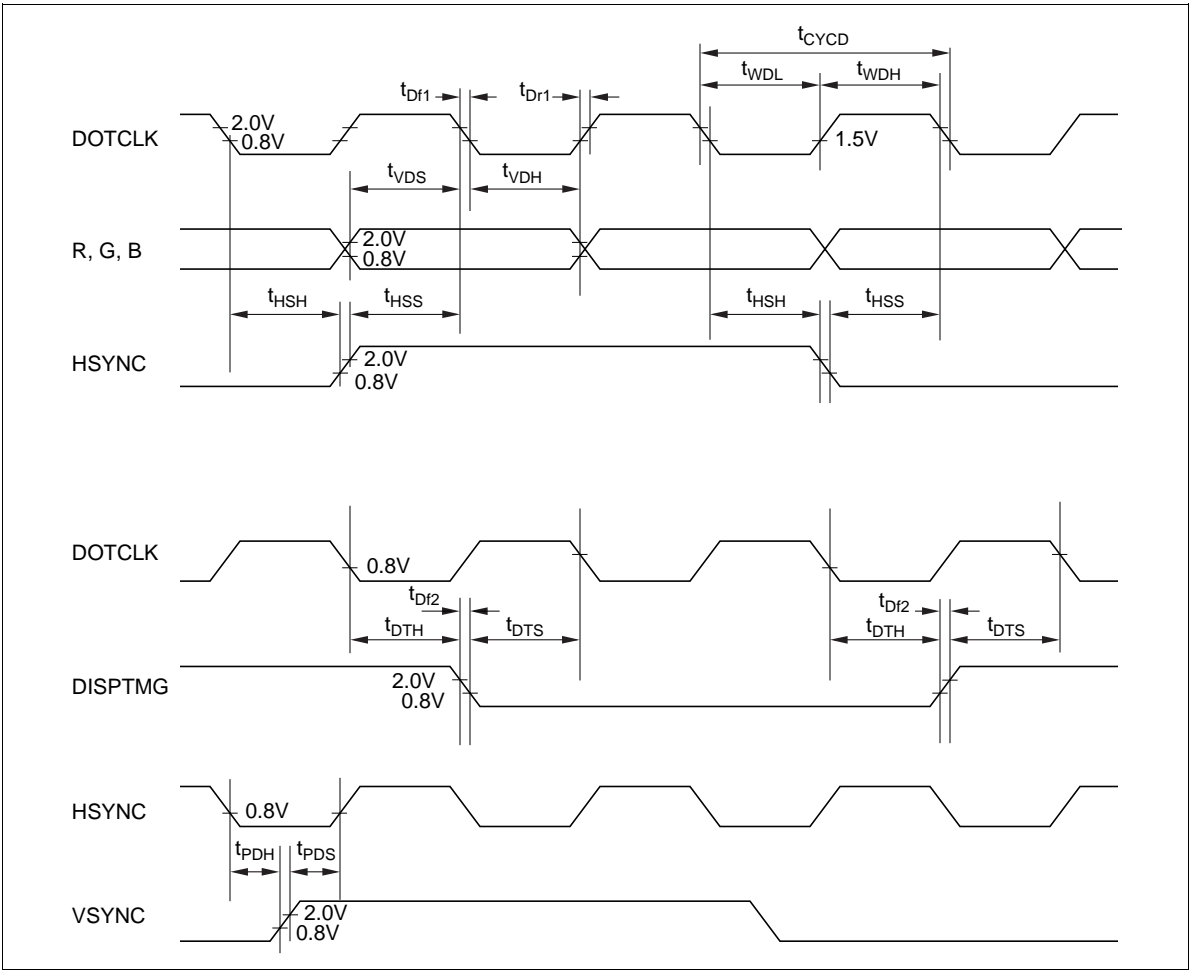


Figure 33 Video Signal Interface

Buffer Memory Interface

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	$5 t_{CYCD} - 50$	—	ns
RD0–RD7, GD0–GD7, BD0–BD7 data setup time	t_{SMD}	25	—	ns
RD0–RD7, GD0–GD7, BD0–BD7 data hold time	t_{HMD}	0	—	ns
Write cycle time	t_{WC}	$6 t_{CYCD} - 50$	—	ns
Address setup time	t_{AS}	$t_{CYCD} - 30$	—	ns
Address hold time	t_{WR}	$t_{CYCD} - 30$	—	ns
Chip select time	t_{CW}	$4 t_{CYCD} - 40$	—	ns
Write pulse width	t_{WP}	$4 t_{CYCD} - 40$	—	ns
RD0–RD7, GD0–GD7, BD0–BD7 output setup time	T_{SMDW}	$2 t_{CYCD} - 25$	—	ns
RD0–RD7, GD0–GD7, BD0–BD7 output hold time	t_{HMDW}	0	—	ns

Note: t_{CYCD} indicates DOTCLK cycle time (min 33 ns, max 1000 ns).

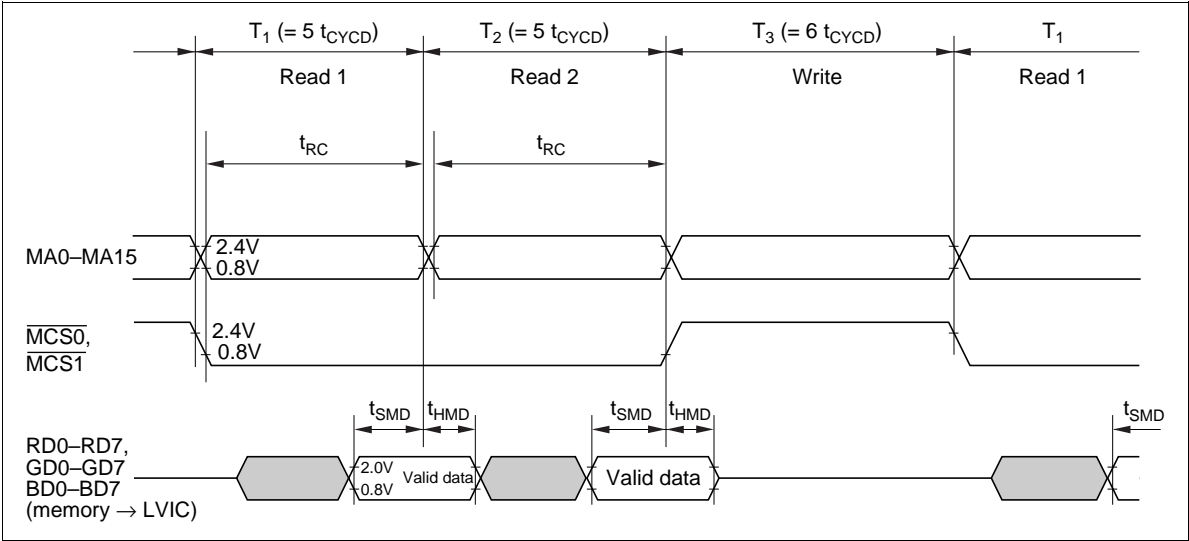


Figure 34 Buffer Memory Interface (RAM Read Timing)

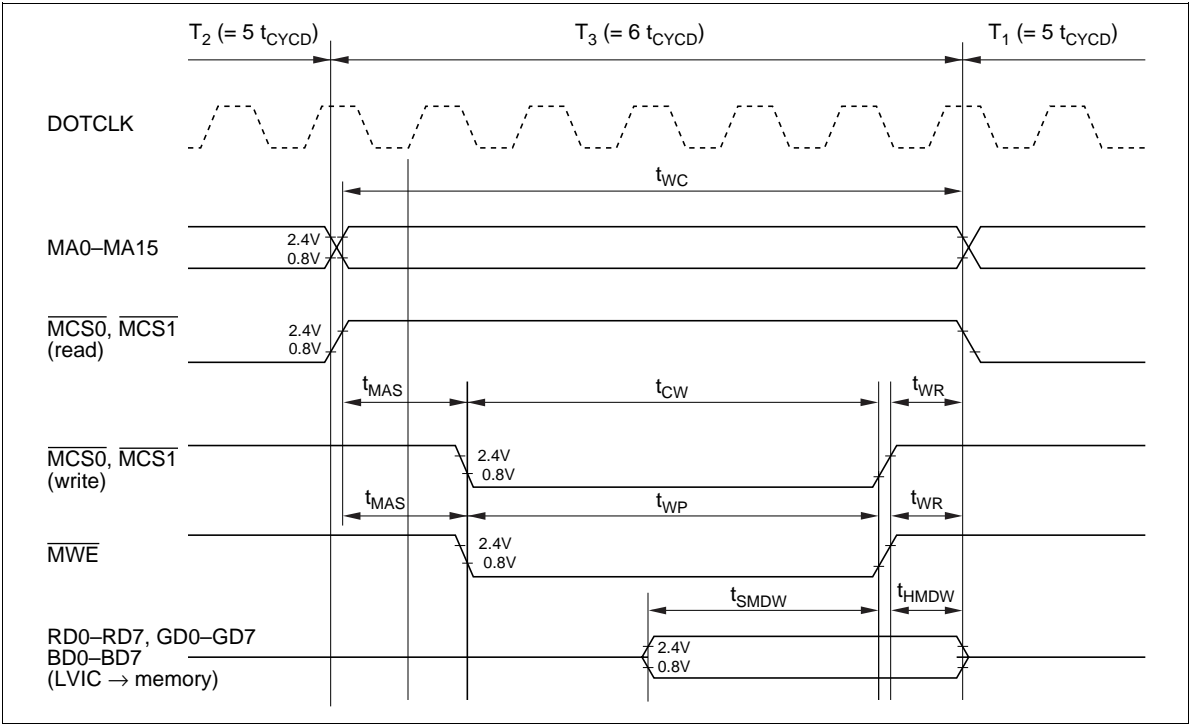


Figure 35 Buffer Memory Interface (RAM Write Timing)

LCD Driver Interface (TN-Type LCD Driver)

Item	Symbol	Min	Max	Unit
CL2 cycle time	t _{WCL2}	166	—	ns
CL2 high-level pulse width	t _{WCL2H}	50	—	ns
CL2 low-level pulse width	t _{WCL2L}	50	—	ns
CL2 rise time	t _{CL2r}	—	30	ns
CL2 fall time	t _{CL2f}	—	30	ns
CL1 high-level pulse width	t _{WCL1H}	200	—	ns
CL1 rise time	t _{CL1r}	—	30	ns
CL1 fall time	t _{CL1f}	—	30	ns
CL1 setup time	t _{SCL1}	500	—	ns
CL1 hold time	t _{HCL1}	200	—	ns
FLM hold time	t _{HF}	200	—	ns
M output delay time	t _{DM}	—	300	ns
Data delay time	t _{DD}	−20	20	ns
LDOTCK cycle time	t _{WLDOT}	41	—	ns

Note: All the values are measured at f_{CL2} = 6 MHz.

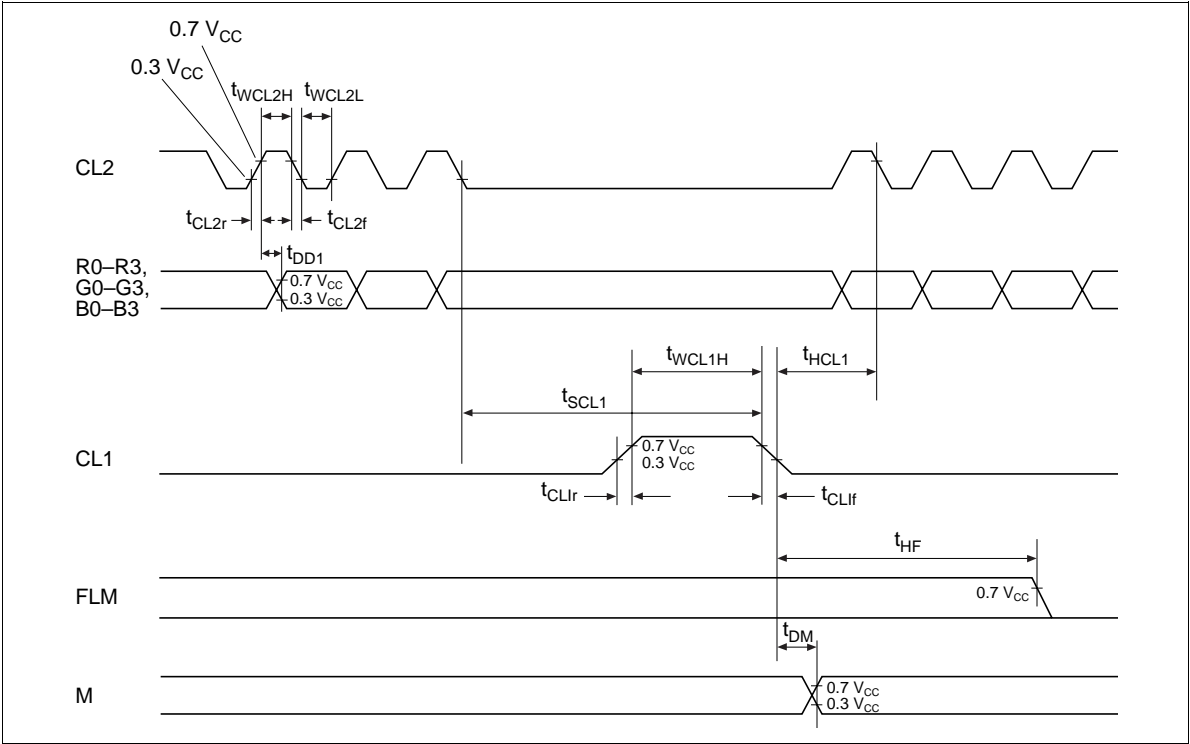


Figure 36 TN-Type LCD Driver Interface

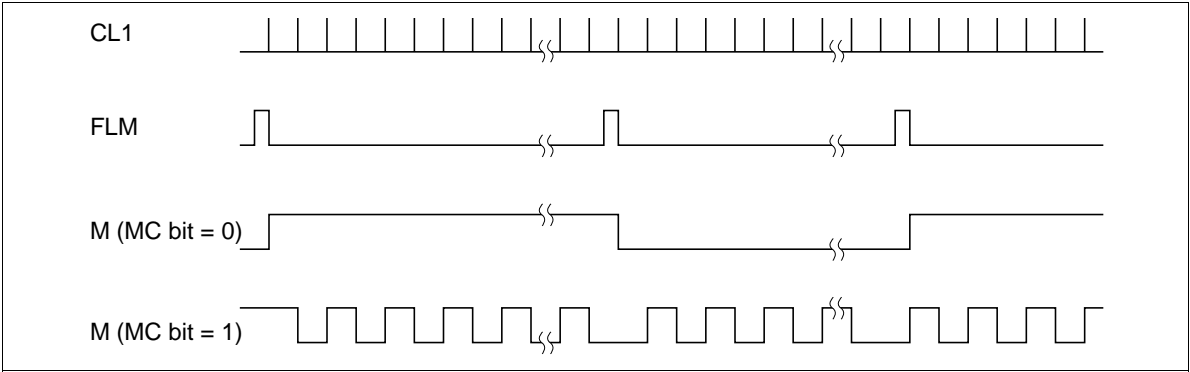


Figure 37 CL1, FLM, and M (Expanded Detail of Figure 34)

LCD Driver Interface (TFT-Type LCD Driver 2)

Item	Symbol	Min	Max	Unit	Remark
CL2 cycle time (X-drivers on one side)	t_{TCL2S}	133	—	ns	Figure 38, 39
CL2 high-level pulse width (X-drivers on one side)	t_{TCL2HS}	30	—	ns	
CL2 low-level pulse width (X-drivers on one side)	t_{TCL2LS}	30	—	ns	
CL2 cycle time (X-drivers on both sides)	t_{TCL2D}	266	—	ns	
CL2 high-level pulse width (X-drivers on both sides)	t_{TCL2HD}	80	—	ns	
CL2 low-level pulse width (X-drivers on both sides)	t_{TCL2LD}	80	—	ns	
CL2 rise time	t_{CL2r}	—	30	ns	
CL2 fall time	t_{CL2f}	—	30	ns	
CL1 high-level pulse width	t_{TCL1H}	200	—	ns	
CL1 rise time	t_{CL1r}	—	30	ns	
CL1 fall time	t_{CL1f}	—	30	ns	
Data delay time	t_{DD1}	−20	20	ns	
Data setup time	t_{LDS}	15	—	ns	
Data hold time	t_{LDH}	15	—	ns	
CL1 setup time	t_{TSCL1}	500	—	ns	
CL1 hold time	t_{THCL1}	200	—	ns	
CL3 delay time	t_{DCL3}	50	—	ns	
M delay time	t_{DM}	—	300	ns	
FLM hold time	t_{TFH}	200	—	ns	
LDOTCK cycle time	t_{WLDOT}	33	—	ns	

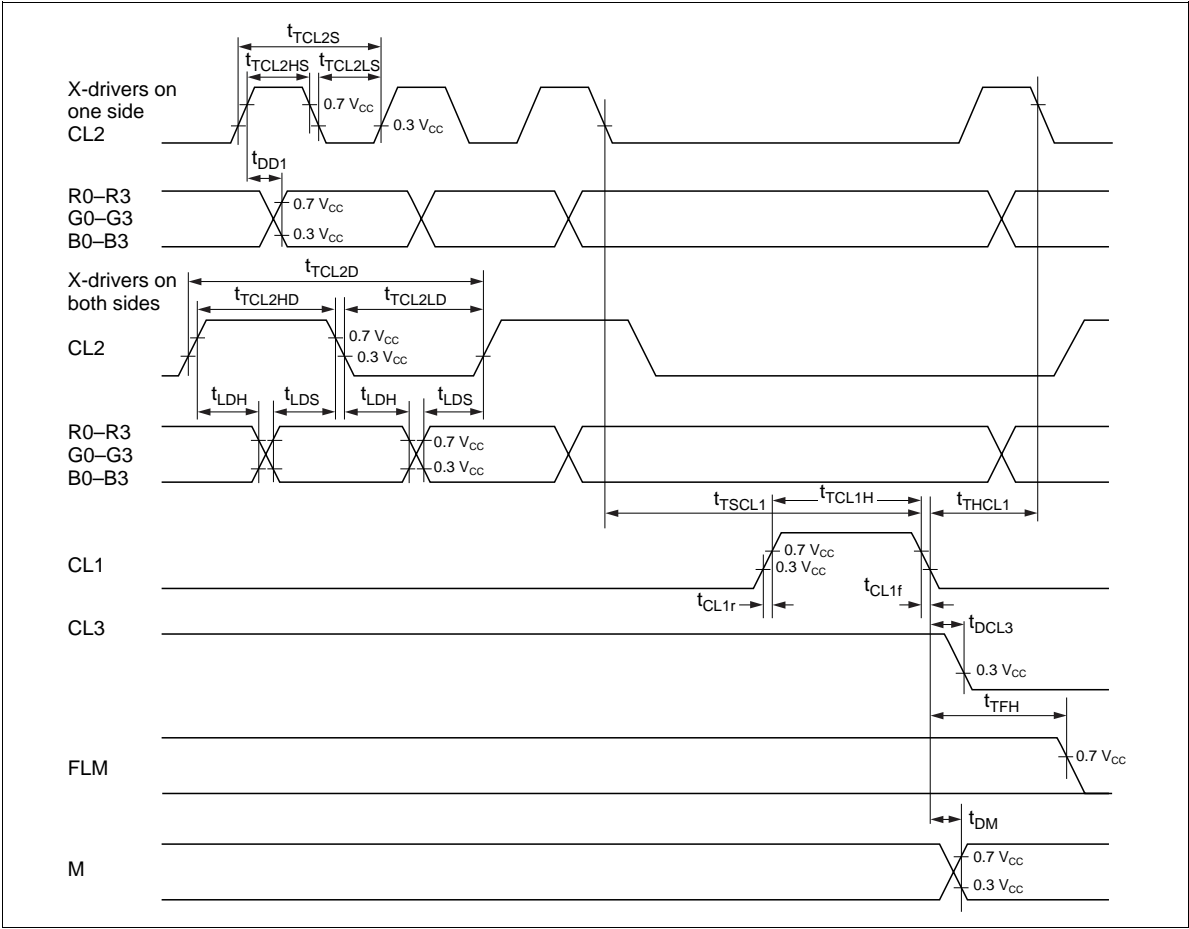


Figure 38 TFT-Type LCD Driver Interface

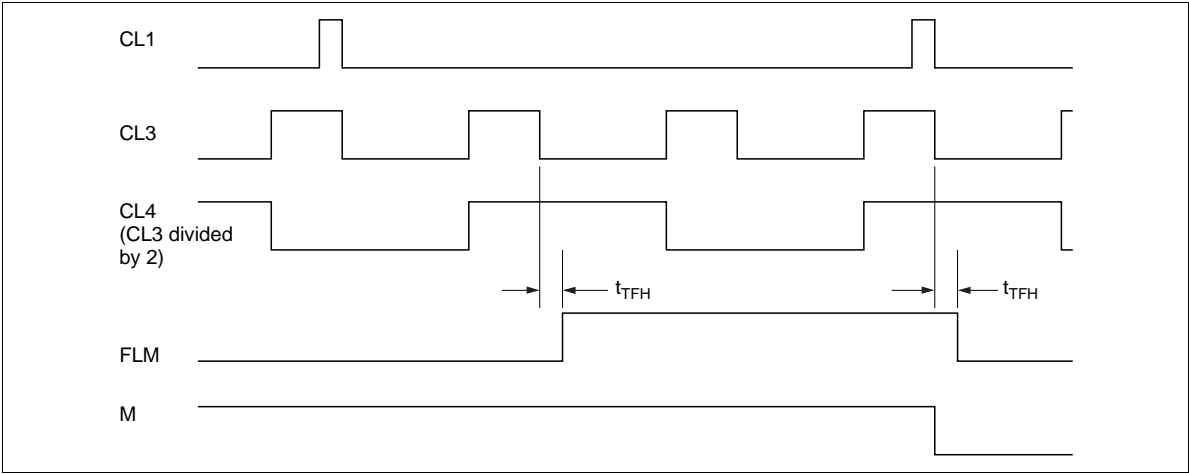


Figure 39 CL1, CL3, CL4, FLM, and M in Horizontal Stripe Modes (Expanded Detail of Figure 38)

Register Programming

MPU Interface

Item	Symbol	Min	Max	Unit	Remark
$\overline{\text{RD}}$ high-level pulse width	t_{WRDH}	190	—	ns	Figure 40
$\overline{\text{RD}}$ low-level pulse width	t_{WRDL}	190	—	ns	
$\overline{\text{WR}}$ high-level pulse width	t_{WWRH}	190	—	ns	
$\overline{\text{WR}}$ low-level pulse width	t_{WWRL}	190	—	ns	
$\overline{\text{CS}}$, RS setup time	t_{AS}	0	—	ns	
$\overline{\text{CS}}$, RS hold time	t_{AH}	0	—	ns	
D0–D3 setup time	t_{DSW}	100	—	ns	
D0–D3 hold time	t_{DHW}	0	—	ns	
D0–D3 output delay time	t_{DDR}	—	150	ns	
D0–D3 output hold time	t_{DHR}	10	—	ns	

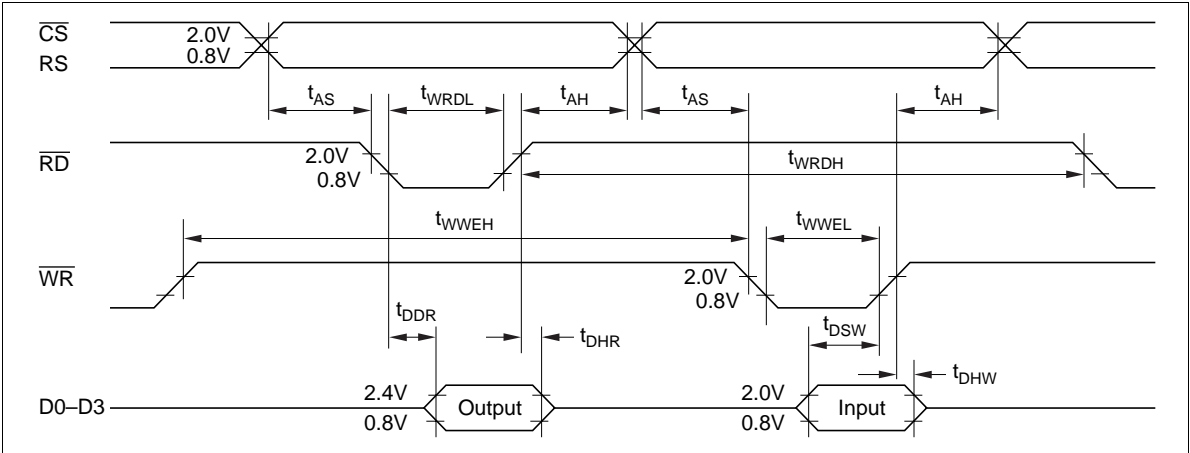


Figure 40 MPU Interface

ROM Interface

Item	Symbol	Min	Max	Unit	Remark
A signal cycle time	t_{CYCA}	528	—	ns	Figure 41
A signal rise time	t_{Ar}	—	100	ns	
A signal fall time	t_{Af}	—	100	ns	
D signal ROM data setup time	t_{DSWD}	120	—	ns	
D signal ROM data hold time	t_{DHWD}	0	—	ns	

Note: $t_{CYCA} = 16 t_{CYCD}$ (t_{CYCD} : DOTCLK cycle time)

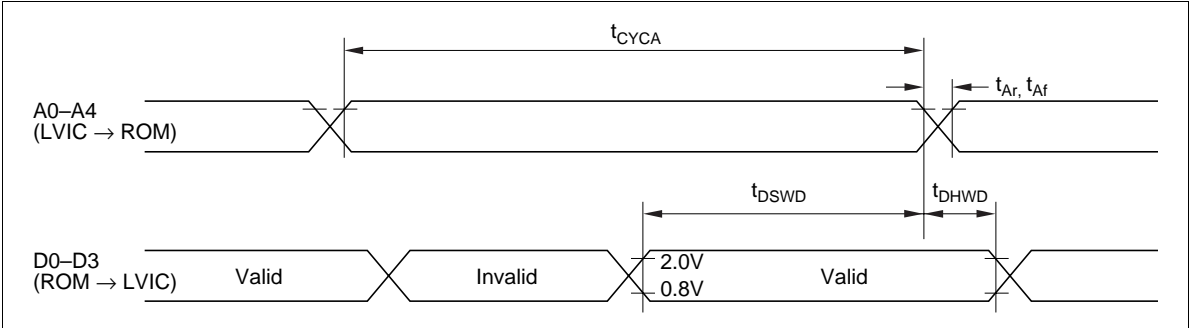


Figure 41 ROM Interface

PLL Interface

Item	Symbol	Min	Max	Unit	Remark
$\overline{\text{CU}}$ fall delay time	t_{Uf}	—	80	ns	Figure 42
$\overline{\text{CU}}$ rise delay time	t_{Ur}	—	80	ns	
$\overline{\text{CD}}$ fall delay time	t_{Df}	—	80	ns	
$\overline{\text{CD}}$ rise delay time	t_{Dr}	—	80	ns	

Reset Input

Item	Symbol	Min	Max	Unit	Remark
RES input pulse width	t_{RES}	1	—	μs	Figure 43

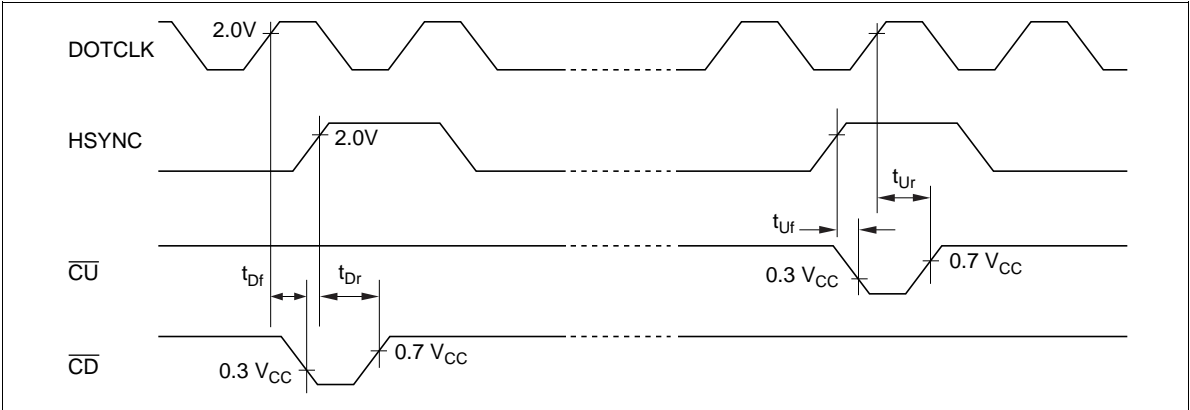


Figure 42 PLL Interface

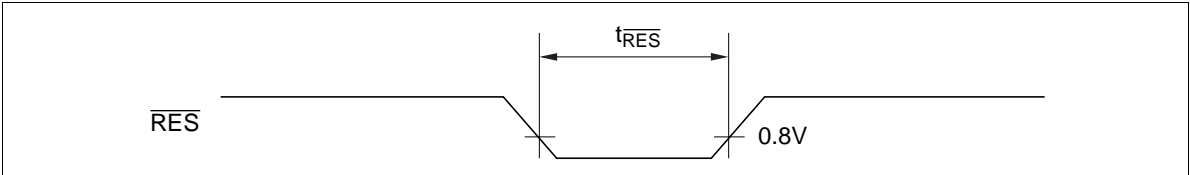


Figure 43 Reset Input

Load Circuits

TTL Load

Pin	RL	R	CL	Remarks
MA0–MA15, MWE, MCS0, MCS1, RD0–RD7, GD0–GD7, BD0–BD7	2.4 kΩ	11 kΩ	40 pF	t _r , t _f : Not specified
A0/RD/XDOT, A1/YL0–A3/YL2, A4/RS/ADJ	2.4 kΩ	11 kΩ	40 pF	t _r , t _f : Specified

Capacitive Load

Pin	C	Remarks
CL1, CL2	40 pF	t _r , t _f : Specified
R0–R3, G0–G3, B0–B3 FLM CU, CD, M, CL3, CL4	40 pF	t _r , t _f : Not specified

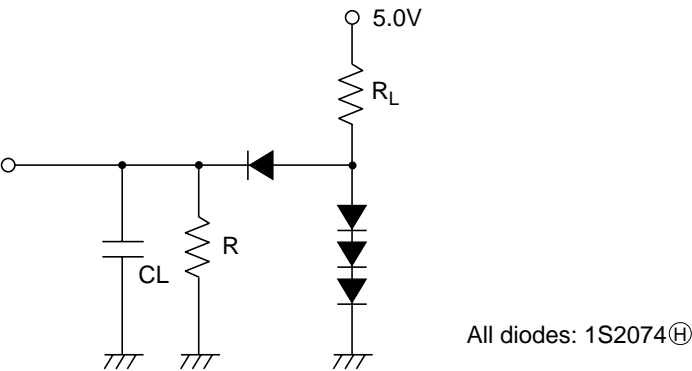


Figure 44 TTL Load Circuit

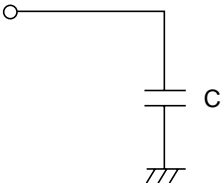


Figure 45 Capacitive Load Circuit

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