16-bit Color LED Driver with PWM Control

Description

The SN3726 is comprised of constant-current drivers designed for color LEDs. The output current value can be set using an external resistor. The output current value can be adjusted from 5mA to 60mA through the external resistor.

As a result, all outputs will have virtually the same current levels.

This driver incorporates 16-bit constant t-current outputs, a 16-bit shift register, a 16-bit latch and a 16-bit AND-gate circuit.

These drivers have been designed using the CMOS process.

Features

- Output current capability and number of outputs: 60 mA × 16 outputs
- Constant current range: 5 to 60 mA
- Application output voltage: ⩾0.4 V
- For anode-common LEDs
- Power supply voltage range V_{DD} = 2.7 to 5.5V
- Serial and parallel data transfer rate: 20 MHz (max, cascade connection)
- Operating temperature range Topr = −40 to 85°C
- Package: QFN-24
- Current accuracy (All output ON)

Output voltage	Current Accuracy		Output Current
	Between Bits	Between ICs	
⩾0.4V	±4%	±12%	5 to 60 mA

Application

- Cellular phones
- MP3/MP4/CD/minidiskplayers
- Toys

Block Diagram

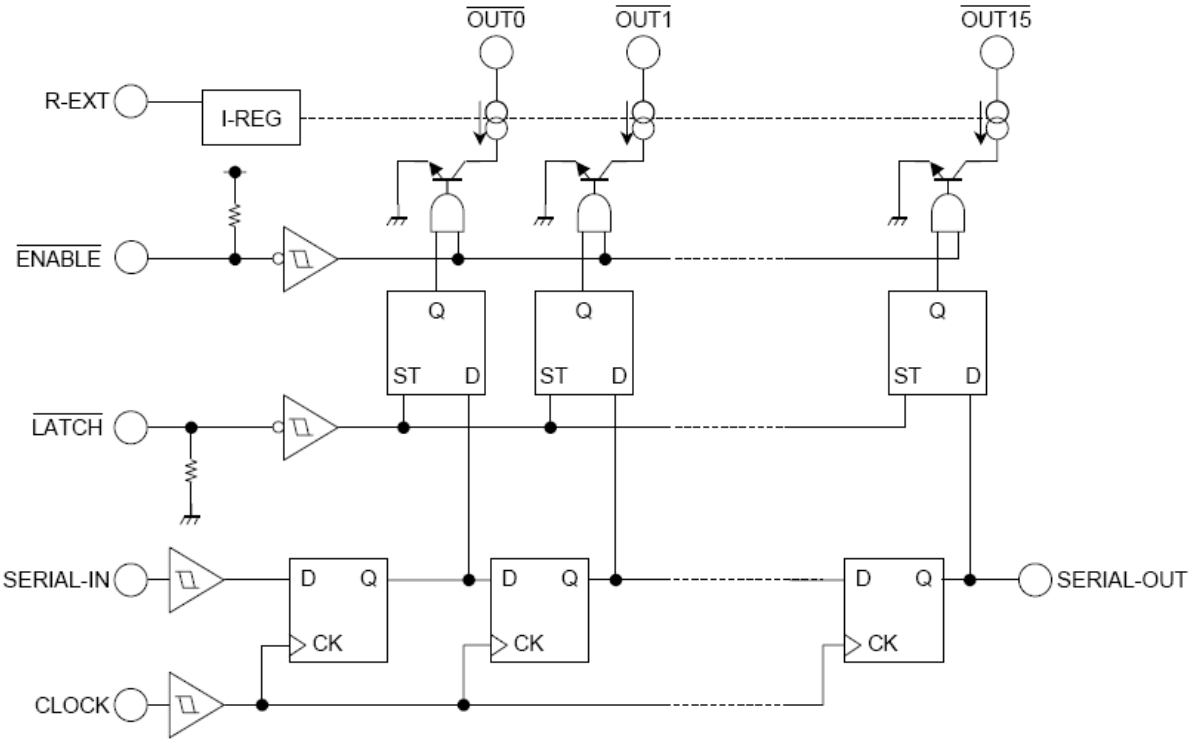


Figure 1

Typical Application Circuit

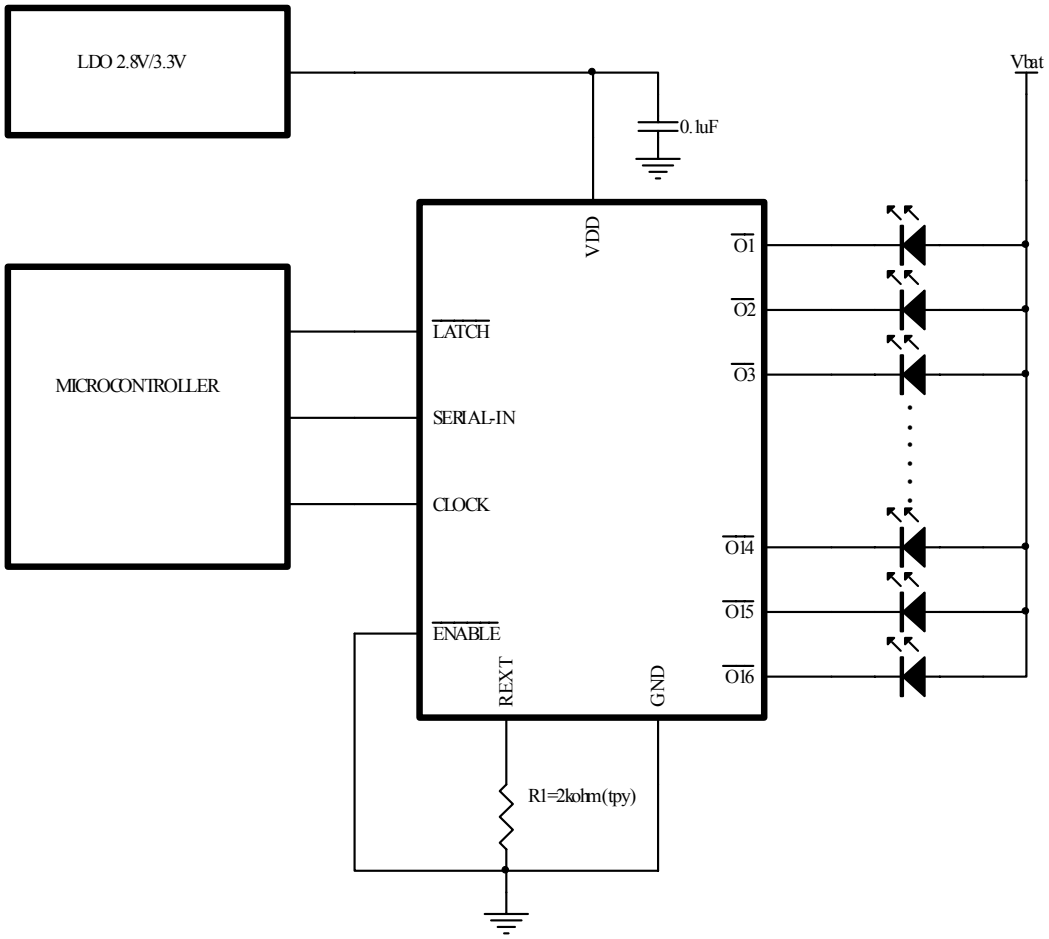
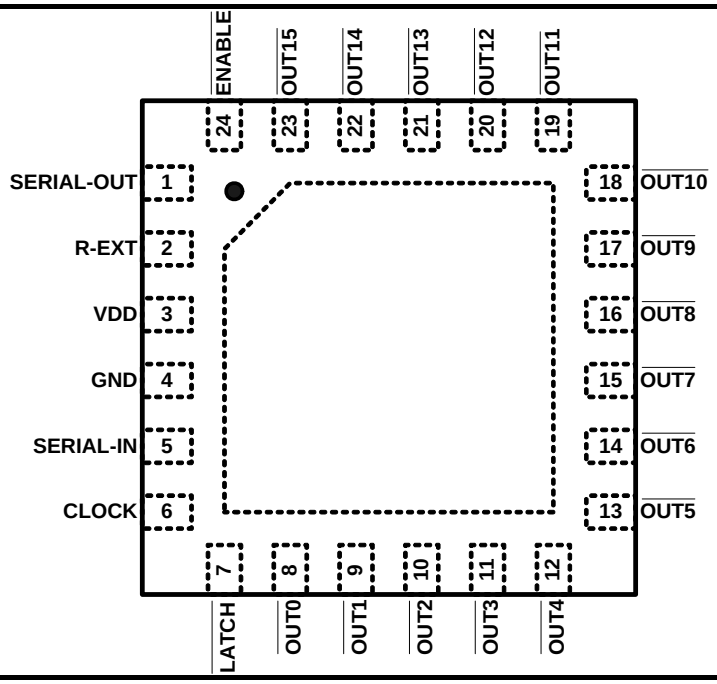


Figure 2. Typical Application Figure

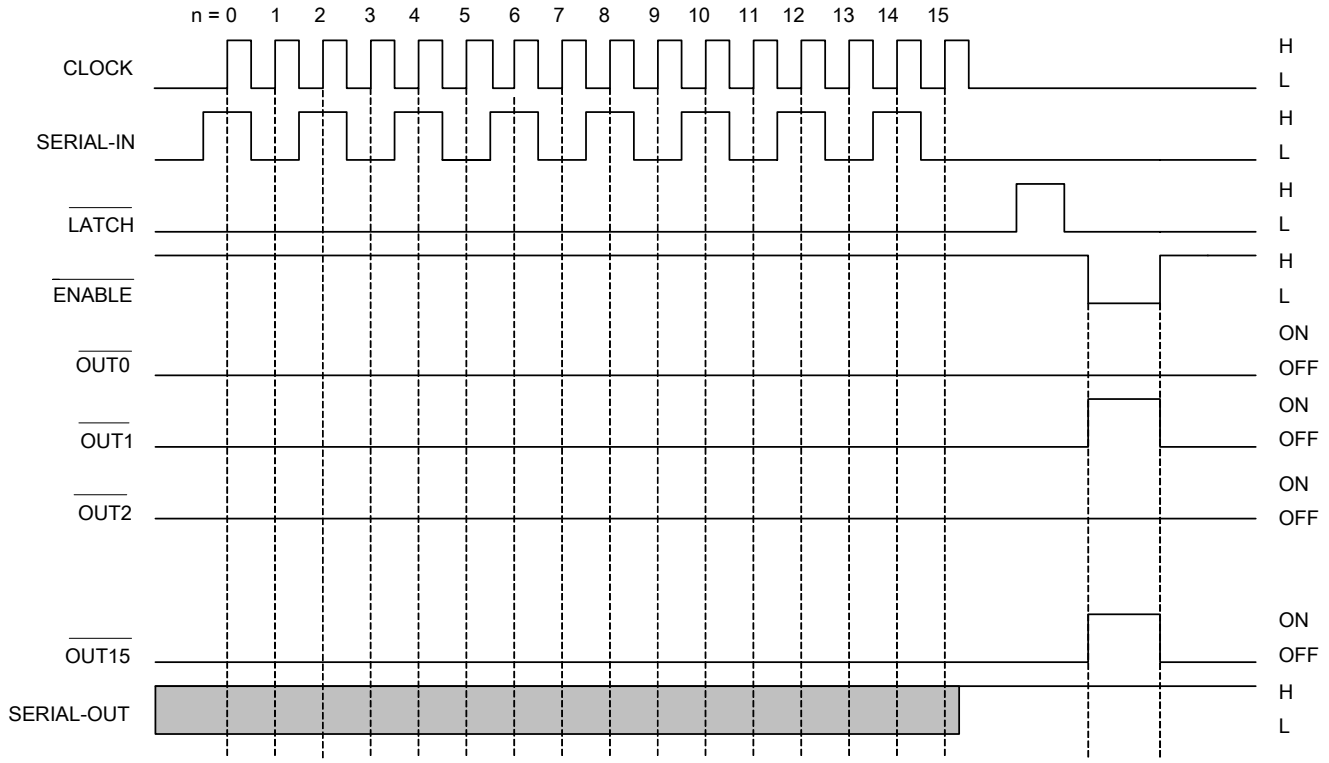
Pin Configurations

Package	Pin Configurations
QFN-24	

Pin Description

Pin	Pin No.	I/O	Description
SERIAL-OUT	1	O	Output terminal for serial data input on SERIAL-IN terminal
R-EXT	2	I	Input terminal used to connect an external resistor. This regulated the output current.
V_{DD}	3	I	Supply voltage terminal.
GND	4		GND terminal for control logic
SERIAL-IN	5	I	Input terminal for serial data for data shift register
CLOCK	6	I	Input terminal for clock for data shift on rising edge
$\overline{\text{LATCH}}$	7	I	Input terminal for data strobe When the $\overline{\text{LATCH}}$ input is driven High, data is not latched. When it is pulled Low ， data is latched.
$\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$	8 to 23	O	Constant-current output terminals
$\overline{\text{ENABLE}}$	24	I	Input terminal for output enable. All outputs ($\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High .And are turned on, when the terminal is driven Low.

Timing Diagram



Warning: Latch circuit is leveled-latch circuit. Be careful because it is not triggered-latch circuit.

Note : The latches circuit holds data by pulling the $\overline{LATCH}$ terminal Low. And, when $\overline{LATCH}$ terminal is a High level, latch circuit doesn't hold data, and it passes from the input to the output. When $\overline{ENABLE}$ terminal is a Low level, output terminal $\overline{OUT0}$ to $\overline{OUT15}$ respond to the data, and on and off does. And, when $\overline{ENABLE}$ terminal is a High level, it offs with the output terminal regardless of the data.

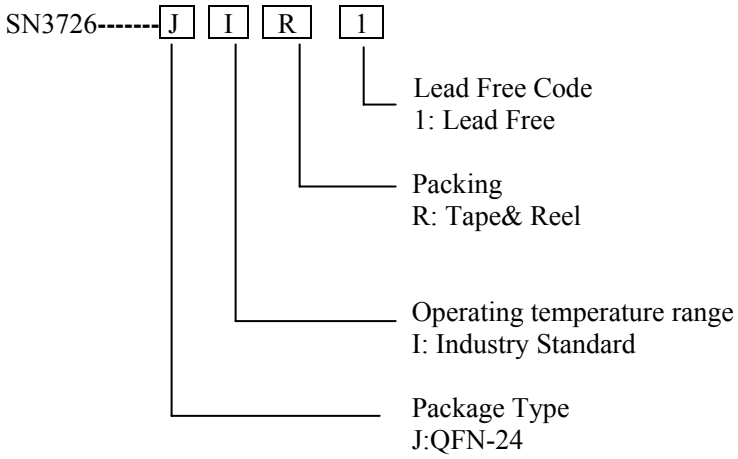
Truth Table

CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL-IN	$\overline{\text{OUT0}}$ …$\overline{\text{OUT7}}$ … $\overline{\text{OUT15}}$	SERIAL-OUT
↑	H	L	Dn	Dn …Dn-7 …Dn-15	Dn-15
↑	L	L	Dn+1	No change	Dn-14
↑	H	L	Dn+2	Dn+2 …Dn-5 …Dn-13	Dn-13
↓	X	L	Dn+3	Dn+2 …Dn-5 …Dn-13	Dn-13
↓	X	H	Dn+3	OFF	Dn-13

Note : $\overline{OUT0}$ to $\overline{OUT15}$ =On when Dn = H; $\overline{OUT0}$ to $\overline{OUT15}$ =Off when Dn = L. In order to ensure that the level of the power supply voltage is correct, an external resistor must be connected between R-EXT and GND.

Ordering Information

Order Number	Package Type	Operating Temperature range
SN3726JIR1	QFN-24	-40 °C to 85°C



Absolute Maximum Ratings

- Supply voltage , V_{DD}---------- 6V
- Input voltage, V_{IN}---------- -0.2V to V_{DD}+0.2V
- Operating temperature range，Topr---- -40°C to 85°C
- Storage temperature range, T_{stg} ------ –55°C to 150°C

Recommended Operating Conditions

(Topr =40°C to 85°C unless otherwise specified)

Characteristics	Symbol	Conditions	Min	Typ.	Max	Unit
Supply voltage	V_{DD}	—	2.7	—	5.5	V
Output voltage	V_{OUT}	—	—	0.7	4	V
Output current	I_{OUT}	Each DC 1 circuit	5	—	60	mA/ch
	I_{OH}	SERIAL-OUT	—	—	-1	mA
	I_{OL}	SERIAL-OUT	—	—	1	
Input voltage	V_{IH}	—	0.7 *V_{DD}	—	V_{DD}+0.15	V
	V_{IL}		-0.15	—	0.3*V_{DD}	
Clock frequency	f_{CLK}	Cascade connected	—	—	20	MHZ
$\overline{\text{LATCH}}$ purse width	t_{wLAT}		50	—	—	ns
CLOCK pulse width	t_{wCLK}	—	25	—	—	ns
$\overline{\text{ENABLE}}$ pulse width (note)	t_{wENA}	Upper I_{OUT}=20mA	2000	—	—	ns
		Lower I_{OUT}=20mA	3000	—	—	
Set-up time for CLOCK terminal	t_{SETUP1}	—	10	—	—	ns
Hold time for CLOCK terminal	t_{HOLD}		10	—	—	ns
Set-up time for $\overline{\text{LATCH}}$ terminal	t_{SETUP2}		50	—	—	ns

Note : When the pulse of the Low level is inputted to the $\overline{ENABLE}$ terminal held in the High level.

Electrical Characteristics *(Topr =25°C, VDD=2.7V to 5.5 V unless otherwise specified)*

Characteristics	Symbol	Conditions		Min	Typ.	Max	Unit
Supply voltage	V_{DD}	Normal operation		2.7	—	5.5	V
Output current	I_{OUT1}	V_{OUT}=0.4V, V_{DD}=3.3V	R_{EXT}=1KΩ	17.2	18.7	20.2	mA
	I_{OUT2}	V_{OUT}=0.4V, V_{DD}=5V	R_{EXT}=1KΩ	17.5	18.9	20.4	mA
Output current error between bits	$\triangle I_{OUT1}$	V_{OUT}≥0.4V, All outputs ON	R_{EXT}=1KΩ	—	±3	±4	%
Output leakage current input voltage	I_{OZ}	V_{OUT}=5.0V		—	—	1	uA
Input voltage	V_{IN}	—		$0.7V_{DD}$	—	V_{DD}	V
		—		GND	—	$0.3V_{DD}$	V
SOUT terminal voltage	V_{OL}	I_{OL}=1.0mA,V_{DD}=3.3V		—	—	0.3	V
		I_{OL}=1.0mA,V_{DD}=5V		—	—	0.3	V
	V_{OH}	I_{OH}=-1.0mA,V_{DD}=3.3V		3	—	—	V
		I_{OH}=-1.0mA,V_{DD}=5V		4.7	—	—	V
Output current supply voltage regulation	%/V_{DD}	When V_{DD} is changed 2.7V to 5.5V		—	-1	-5	%
Pull-up resistor	$R_{(Up)}$	$\overline{ENABLE}$ terminal		115	230	460	kΩ
Pull-down resistor	$R_{(Down)}$	$\overline{LATCH}$ terminal					
Supply current	$I_{DD(OFF)1}$	VOUT=5V	R_{EXT}=OPEN	—	0.18	0.25	mA
	$I_{DD(OFF)2}$	VOUT=5V, All outputs OFF	R_{EXT}=1KΩ	2	3.5	3.8	mA
	$I_{DD(ON)1}$	VOUT=0.7V, All outputs ON	R_{EXT}=1KΩ	—	3.5	4	mA

Switching Characteristics *(Topr= 25°C unless otherwise specifed)*

Characteristics	Symbol	Conditions	Min	Typ.	Max	Unit
Propagation delay	t_{pLH1}	CLK- $\overline{OUTn}$, $\overline{LATCH}$ = "H", $\overline{ENABLE}$ = "L"	—	80	200	ns
	t_{pLH2}	$\overline{LATCH}$ –$\overline{OUTn}$,$\overline{ENABLE}$ = "L"	—	80	200	
	t_{pLH3}	$\overline{ENABLE}$ -$\overline{OUTn}$, $\overline{LATCH}$ = "H"	—	130	250	
	t_{pLH}	CLK-SERIAL OUT	3	5	—	
	t_{pHL1}	CLK- $\overline{OUTn}$, $\overline{LATCH}$ ="H", $\overline{ENABLE}$="L"	—	160	250	
	t_{pHL2}	$\overline{LATCH}$ -$\overline{OUTn}$, $\overline{ENABLE}$= "L"	—	160	250	
	t_{pHL3}	$\overline{ENABLE}$ -$\overline{OUTn}$, $\overline{LATCH}$ ="H"	—	200	350	
	t_{pLH}	CLK-SERIAL OUT	4	6	—	
Output rise time	t_{or}	10~90% of voltage waveform	30	150	200	ns
Output fall time	t_{of}	90~10% of voltage waveform	150	200	250	ns
Maximum CLOCK rise time	t_r	When not on PCB （Note)	—	—	5	us
Maximum CLOCK fall time	t_f		—	—	5	us

Conditions: (Refer to test circuit.)

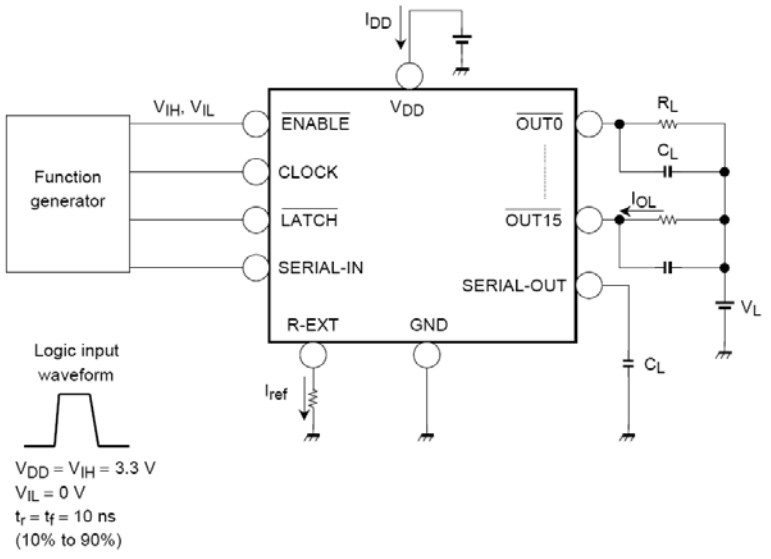
Topr = 25°C, V_{DD}=V_{IH} =3.3 V and 5 V, V_{OUT} = 0.7 V, V_{IL} =0 V, R_{EXT} =1000Ω,V_L =3.0 V, R_L=60Ω, C_L=10.5 pF

Note:

1、 If the device is connected in a cascade and tr/tf for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

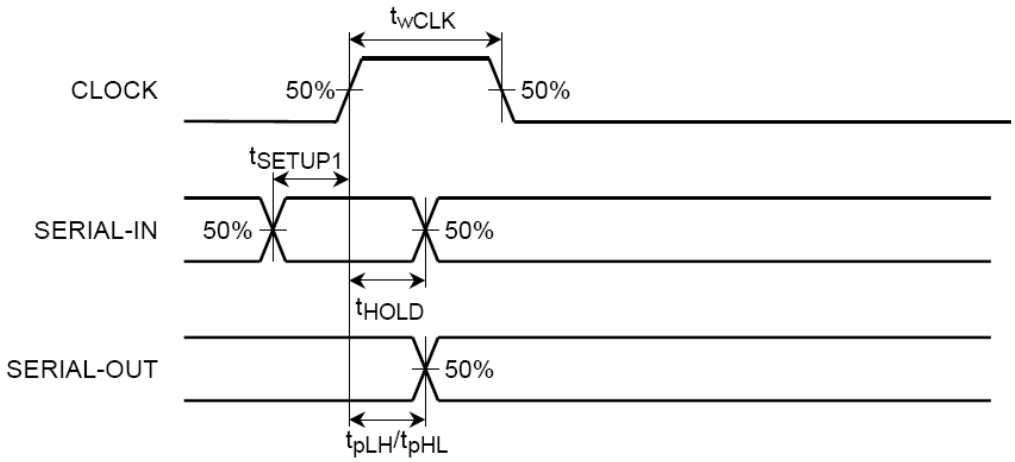
2、 Delay between outputs. The SN3726 has graduated delay circuits between outputs. The fixed delay time is 5ns (typical), OUT1 has 5ns delay, OUT2 has 10 ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on. The delay works during switch on and switch off of each output channel. LEDs that have not turned on before $\overline{ENABLE}$ is low will still turn on and off at the determined delayed time regardless of the state of $\overline{ENABLE}$. Therefore, every LED will be illuminated for the amount of time $\overline{ENABLE}$ is pulled high.

Test Circuit

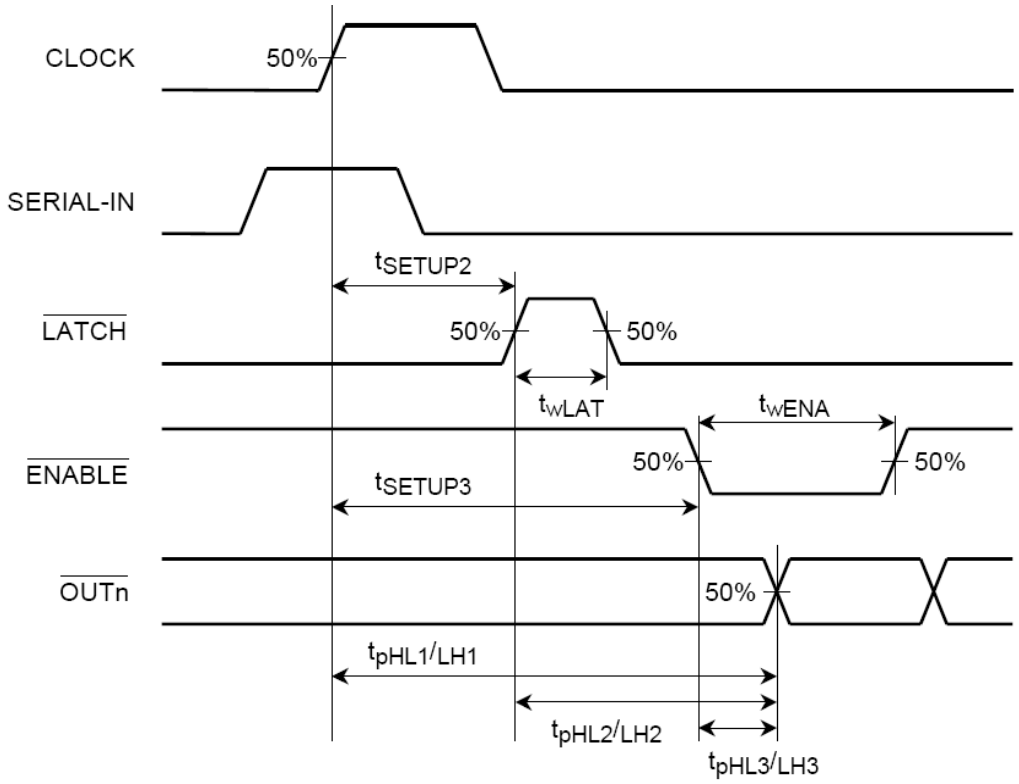


Timing Waveforms

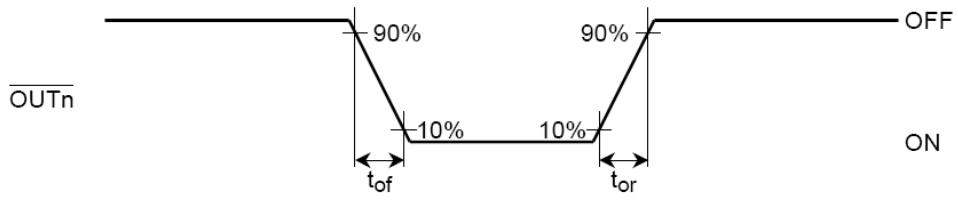
1. CLOCK,SERIAL-IN,SERIAL-OUT



2. CLOCK, SERIAL-IN, $\overline{\text{LATCH}}$, $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$



3. $\overline{\text{OUTn}}$

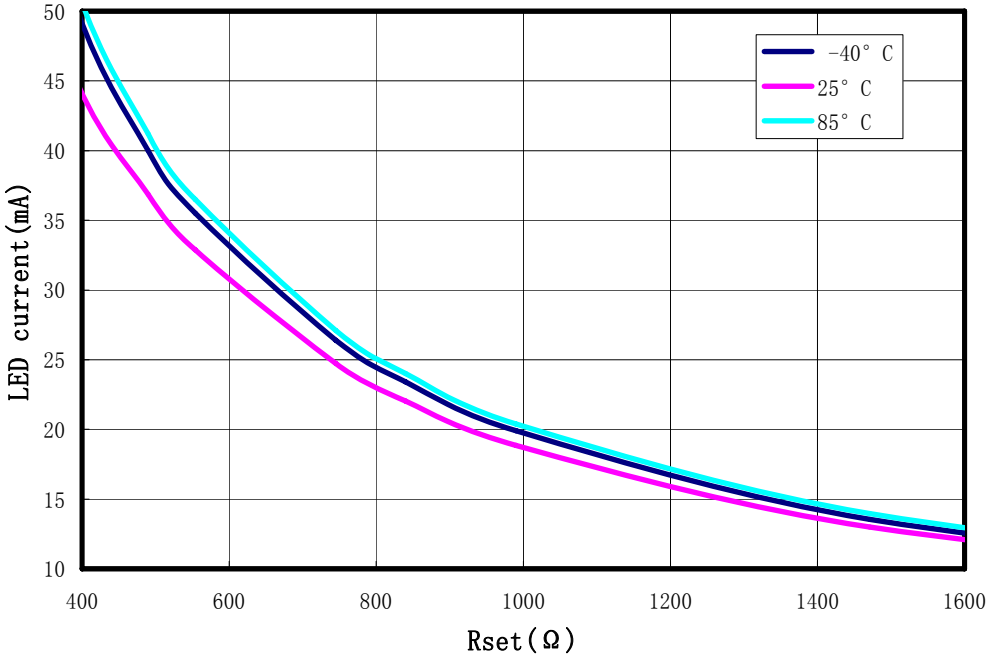


Typical Operating Characteristics

Adjusting output current

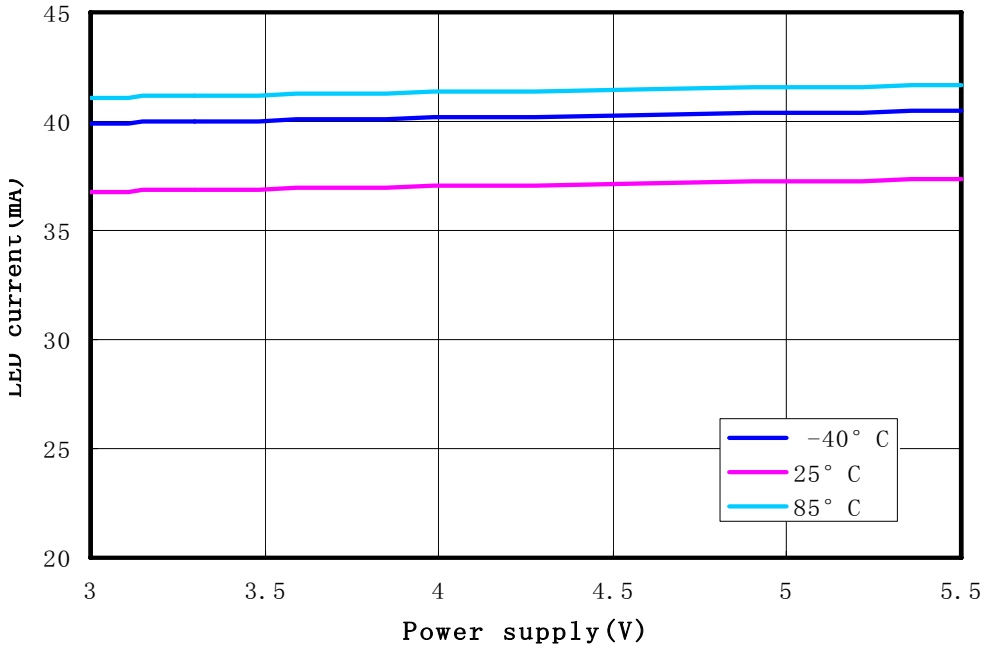
The output current of each channel is set by an external resistor R_{ext}, the relationship between I_{out} and R_{ext} is: $I_{out} = (V_{R\text{-}ext}/R_{ext})*52$,the $V_{R\text{-}ext}$ is 0.36V in the SN3726,so we can count the I_{out} as : $I_{out} = 0.36*52/R_{ext}$.

As show in the figure below:



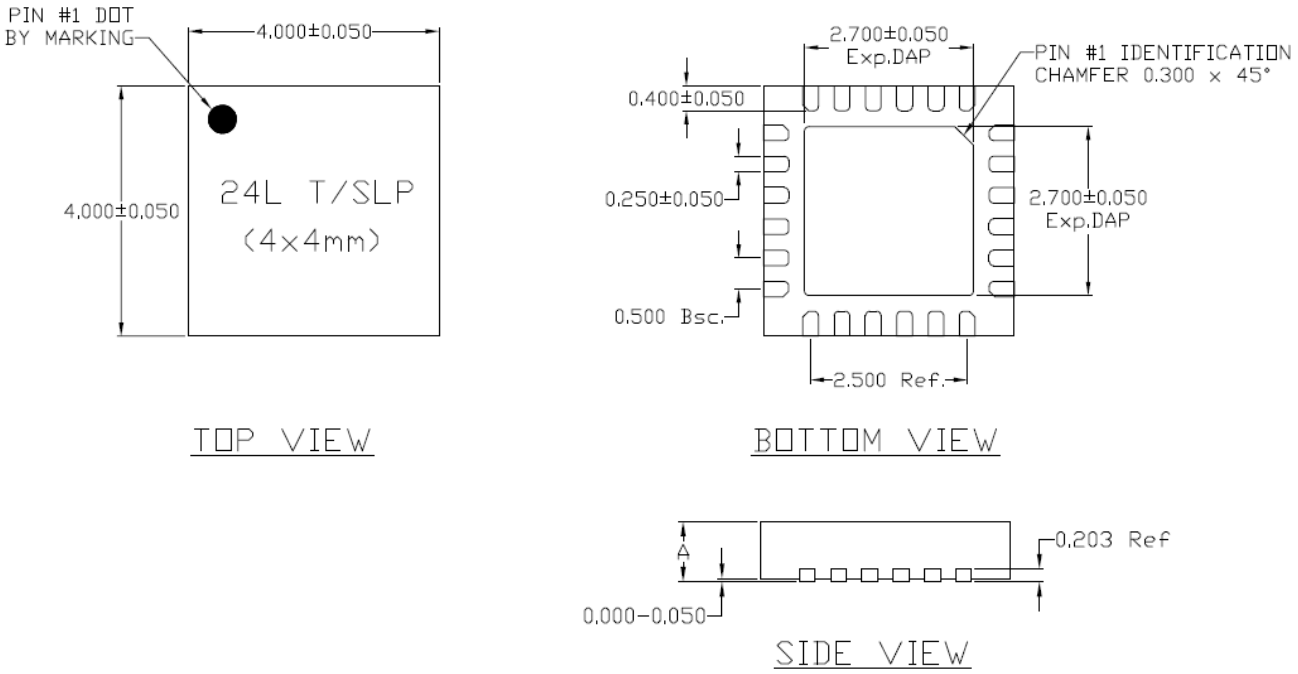
Constant current

As the figure shown below, the current characteristic of output stage is flat. The output current can be kept constant regardless of the variations of LED forward voltages (V_F).this performs as a perfection of load regulation.



Package Information

QFN-24



Symbol	Dimension (mm)		
	MIN	NOM	MAX
A	0.70	0.75	0.80

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