PHKD13N03LT

Dual N-channel TrenchMOS logic level FET

Rev. 03 — 27 April 2010 **Product data sheet**

1. Product profile

1.1 General description

Dual logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- DC-to-DC convertors
- Lithium-ion battery applications
- Notebook computers
- Portable equipment

1.4 Quick reference data

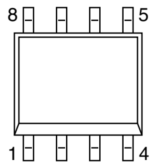
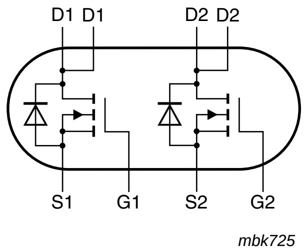
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C		-	-	30	V
I_D	drain current	$T_{sp} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 3	[1]	-	-	10.4	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; see Figure 2		-	-	3.57	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 8$ A; $T_j = 25$ °C; see Figure 9; see Figure 10		-	17	20	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 5$ V; $I_D = 5$ A; $V_{DS} = 15$ V; $T_j = 25$ °C; see Figure 11		-	3.9	-	nC

[1] Single device conducting.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 SOT96-1 (SO8)	
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHKD13N03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

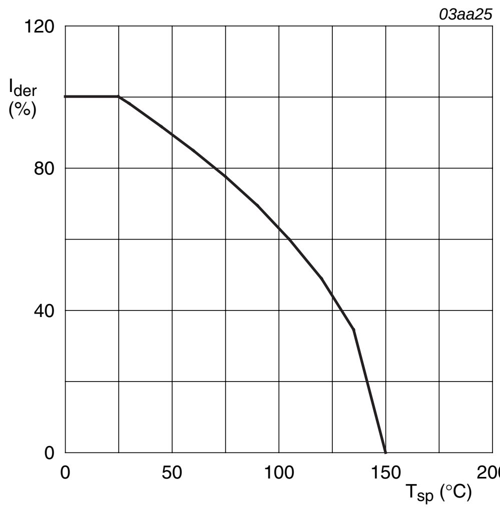
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

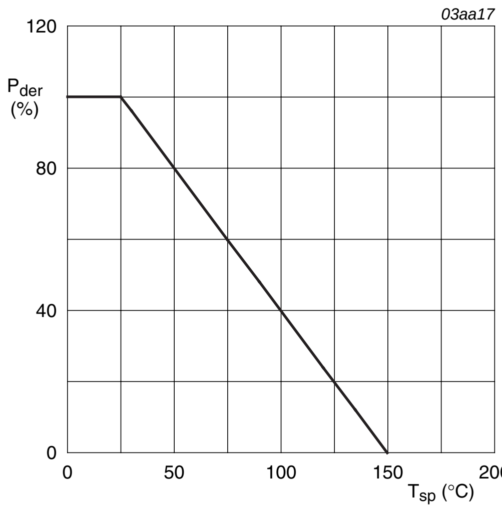
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C		-	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; $R_{GS} = 20$ kΩ		-	-	30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$T_{sp} = 100$ °C; $V_{GS} = 10$ V; see Figure 1	[1]	-	-	6.6	A
		$T_{sp} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 3	[1]	-	-	10.4	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; $t_p \leq 10$ µs; pulsed; see Figure 3	[1]	-	-	42	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; see Figure 2		-	-	3.57	W
T_{stg}	storage temperature			-55	-	150	°C
T_j	junction temperature			-55	-	150	°C
Source-drain diode							
I_S	source current	$T_{sp} = 25$ °C	[1]	-	-	3.2	A
I_{SM}	peak source current	$T_{sp} = 25$ °C; $t_p \leq 10$ µs; pulsed	[1]	-	-	42	A

[1] Single device conducting.



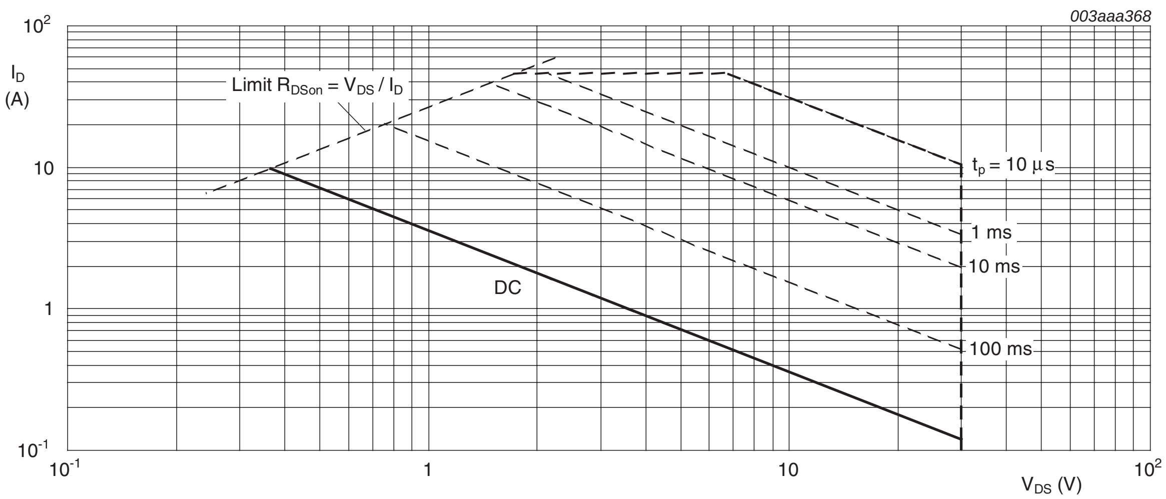
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$$T_{sp} = 25°C;\ I_{DM} \text{ is single pulse}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	35	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	70	-	K/W

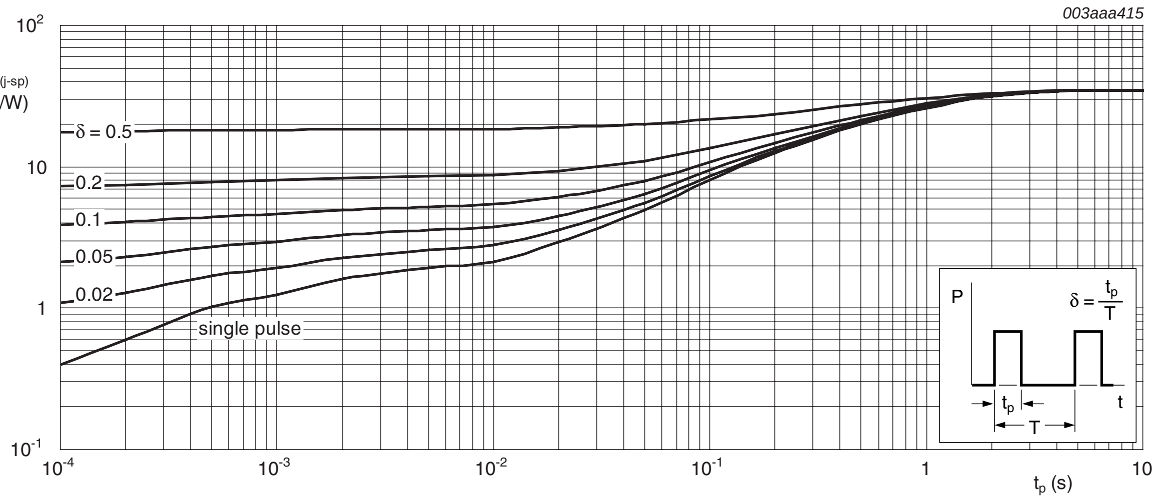
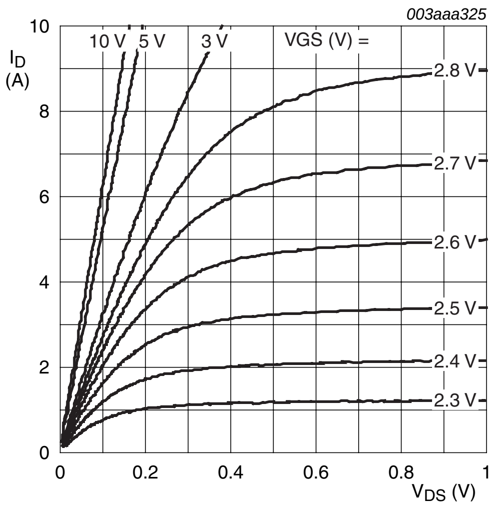


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

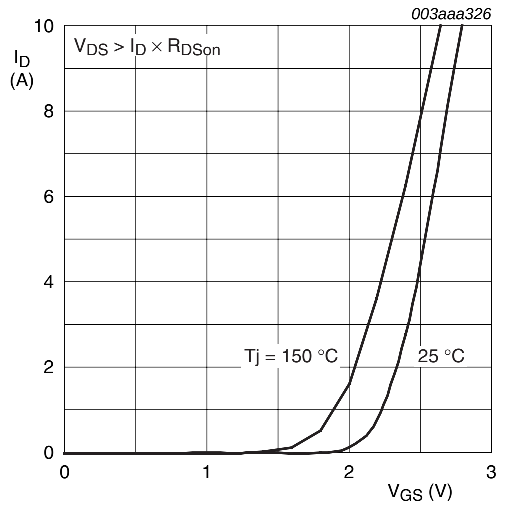
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	27	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 8	-	-	2.2	V
		I_D = 250 µA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 8	0.5	-	-	V
		I_D = 250 µA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 8	1	1.5	2	V
I_{DSS}	drain leakage current	V_{DS} = 24 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 24 V; V_{GS} = 0 V; T_j = 100 °C	-	-	5	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 8 A; T_j = 150 °C; see Figure 9; see Figure 10	-	-	34	mΩ
		V_{GS} = 4.5 V; I_D = 7 A; T_j = 25 °C; see Figure 9	-	21	26	mΩ
		V_{GS} = 10 V; I_D = 8 A; T_j = 25 °C; see Figure 9; see Figure 10	-	17	20	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 15 V; V_{GS} = 5 V; T_j = 25 °C; see Figure 11	-	10.7	-	nC
Q_{GS}	gate-source charge		-	2.7	-	nC
Q_{GD}	gate-drain charge		-	3.9	-	nC
C_{iss}	input capacitance	V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 12	-	752	-	pF
C_{oss}	output capacitance		-	200	-	pF
C_{rss}	reverse transfer capacitance		-	130	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 10 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C; I_D = 1.5 A	-	6	-	ns
t_r	rise time		-	7	-	ns
$t_{d(off)}$	turn-off delay time		-	23	-	ns
t_f	fall time		-	11	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 7 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 13	-	0.86	1.1	V
t_{rr}	reverse recovery time	I_S = 7 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C	-	25	-	ns
Q_r	recovered charge		-	5	-	nC



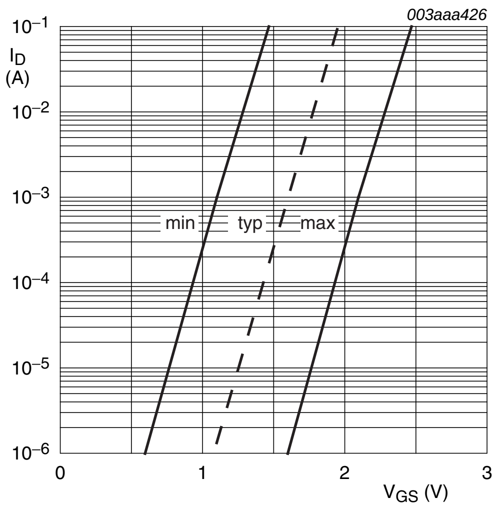
$T_j = 25\,°C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



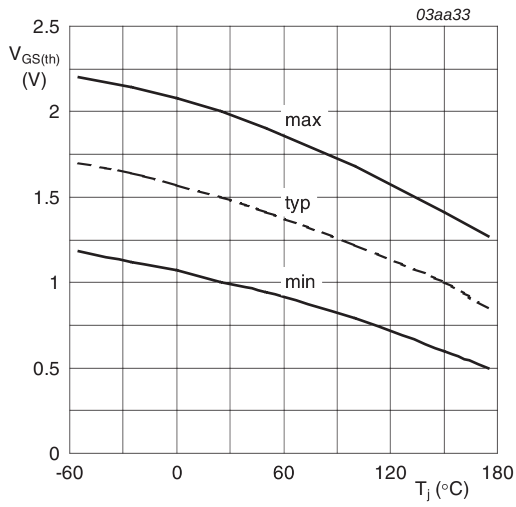
$V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



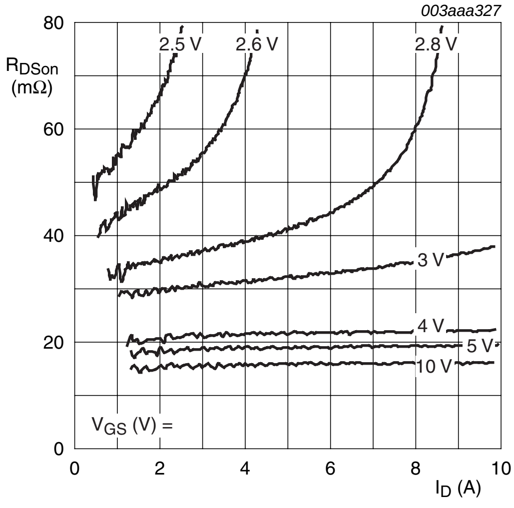
$T_j = 25\,°C; V_{DS} = 5\,V$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



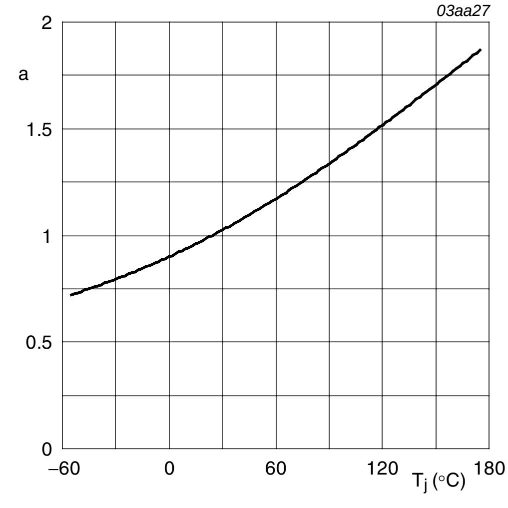
$I_D = 1\,mA; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



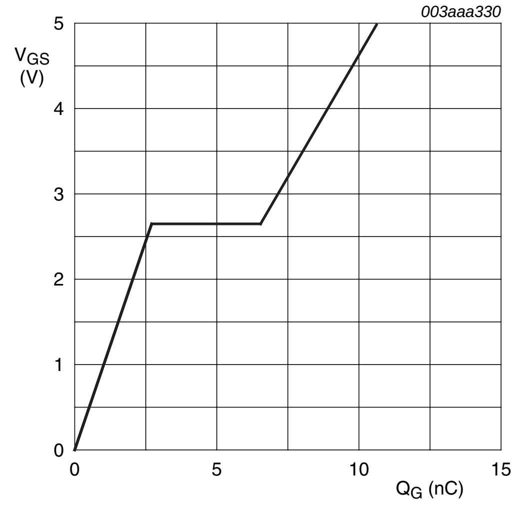
$T_j = 25\,°C$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



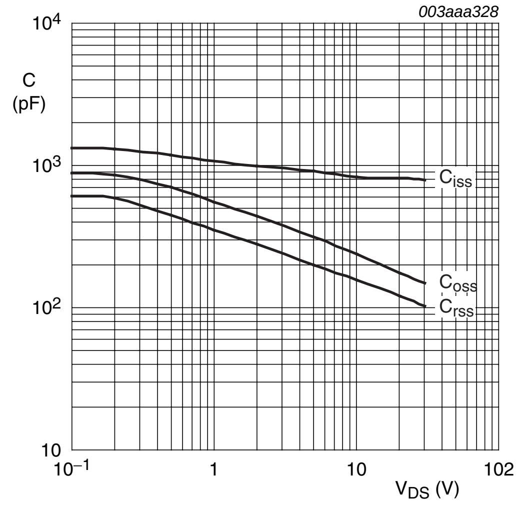
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



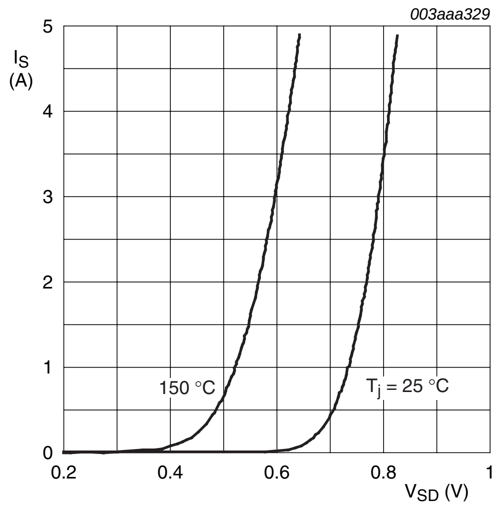
$I_D = 8\,A; V_{DD} = 15\,V$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\,V; f = 1\,MHz$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

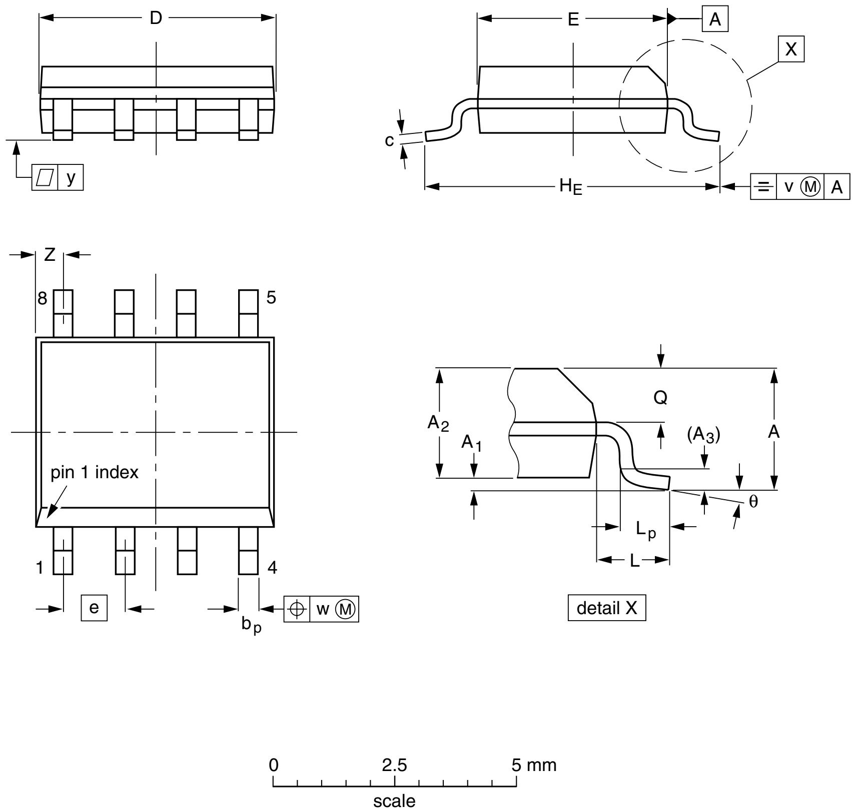


$$V_{GS} = 0\,V$$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHKD13N03LT_3	20100427	Product data sheet	-	PHKD13N03LT_2
Modifications:	• Various changes to content.			
PHKD13N03LT_2	20090306	Product data sheet	-	PHKD13N03LT-01
PHKD13N03LT-01 (9397 750 11612)	20030623	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 27 April 2010

Document identifier: PHKD13N03LT