PIC18F458 → PIC18F4580 Migration

DEVICE MIGRATIONS

The PIC18F4580 is an extended architecture based on the PIC18F458 family, but offers many new features. This document is intended to describe the functional differences, configuration differences and the electrical specification differences that are present when migrating from one device to the next.

Table 1 summarizes the features that may have migration impact on the software code developed for PIC18F458. Table 2 lists the new and modified features of PIC18F4580 that should not have any migration impact. Table 3 and Table 4 summarize the differences in SFRs and configuration memory, respectively. Table 5 summarizes the differences in specific DC characteristics.

The descriptions in the tables explain the differences in brief. The user should refer to the most current version of the device data sheet for the PIC18F458 family (DS41159) and the PIC18F4580 family (DS39637) for detailed explanations. In addition, it is always good design practice to review the latest errata for a device for recent changes.

Note:	This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

Note:	The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

Note:	Throughout this document, “PIC18F4580” refers to the entire PIC18F2480/2580/4480/4580 family of microcontrollers. “PIC18F458” refers to the entire PIC18F248/258/448/458 family of microcontrollers.

TABLE 1: PIC18F458 → PIC18F4580 FEATURES AFFECTING SOFTWARE

Item	Module	Comments
1	Analog-to-Digital Converter (ADC)	1. The PIC18F4580 ADC supports both auto-acquisition and more analog channels. The PIC18F4580 is defined to maintain 100% pinout compatibility with the PIC18F458 by mapping the extra analog inputs with the existing PORTB<4:0> inputs. PORTB<4:0> can be configured either as analog or digital on POR by a configuration bit (CONFIG3H<1>). These changes may require software modifications and, in rare cases, hardware changes to an application's design. 2. Bit allocations for the ADCON0 and ADCON1 registers in the PIC18F4580 are different from PIC18F458. Also, the PCFG3:PCFG0 bits in ADCON1, while in the same positions, do not share equivalent port configurations in both device families. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 19.0 "10-Bit Analog-to-Digital Converter (A/D) Module"** and the PIC18F458 data sheet (DS41159), **Section 20.0 "Compatible 10-Bit Analog-to-Digital Converter (A/D) Module"**.
2	Boot Block	PIC18F4580 has a selectable boot block size of either 2 Kbytes or 4 Kbytes (00h to 7FFh or 00h to FFFh) as compared to 512 bytes (00h to 1FFh) in the PIC18F458. Boot block size is selected by configuration bits in the CONFIG4L register. This change may have an impact on software migration where the table read and write instructions are used and any one of the code protection features (code-protect, write-protect and read-protect) is used. This change may also effect boot loader firmware. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 24.0 "Special Features of the CPU"** and the PIC18F458 data sheet (DS41159), **Section 24.0 "Special Features of the CPU"**.
3	MSSP	For the MSSP module implemented in the PIC18F4580 to receive data in I^2C™ Master mode, the module must be in an Idle state before the RCEN bit is set. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 17.4.11 "I^2C Master Mode Reception"**.

TABLE 2: PIC18F458 → PIC18F4580 NEW FEATURES

Item	Module	Comments
1	Core	1. In addition to the standard 75 instructions of the PIC18F458 instruction set, PIC18F4580 also provides an optional extension to the core CPU functionality. The added features include 8 additional instructions. The additional instruction set is designed to optimize applications written in C; the user may likely never use these instructions directly in assembler. 2. An additional addressing mode, Indexed Literal Offset, is available when the extended instruction set is enabled. The use of Indexed Literal Offset Addressing mode effectively changes how the first 96 locations of the Access RAM (00 to 5Fh) are mapped. Also, the execution of some instructions in the PIC18F458 instruction set are changed when the extended instruction set is enabled. When using the Microchip C compiler, refer to the latest "*MPLAB® C18 C Compiler User's Guide"* (DS51288) for information on the C compiler operation in Extended mode. 3. The additional features of the extended instructional set are disabled by default. To enable them, the user must set the XINST configuration bit. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 5.5 "Program Memory and the Extended Instruction Set"**.
2	Power-Managed Modes	1. PIC18F4580 devices offer a total of seven operating modes for more efficient power management. These modes provide a variety of options for selective power conservation in applications where resources may be limited (i.e., battery-powered devices). 2. Two operating modes (SEC_RUN and RC_RUN) allow the device to be clocked from either the Timer1 oscillator or from the internal oscillator block (see below). 3. Three Idle modes (PRI_IDLE, SEC_IDLE and RC_IDLE) allow the controller CPU to be selectively powered down while the peripherals continue to operate. 4. PIC18F4580 devices also offer a Sleep mode, similar to the PIC18F458, but that consumes less current. Most of these features are controlled by new bits in the OSCCON register. Users need to make certain that bits that are unimplemented in the PIC18F458 OSCCON register are not modified. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 3.0 "Power-Managed Modes"**.
3	Multi-Frequency Internal Oscillator Block	The PIC18F4580 includes an internal oscillator block. The main output (INTOSC) is an 8 MHz clock source which can be used to directly drive the device clock. It also drives a postscaler which can provide a range of clock frequencies from 31 kHz to 8 MHz. The internal oscillator block can also provide clock frequencies up to 32 MHz when used with the internal PLL. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 2.6 "Internal Oscillator Block"**.
4	Interrupts	PIC18F4580 supports an additional interrupt, the oscillator fail interrupt, for indicating the failure of the primary clock source. Bit <7> is implemented in the PIR2, PIE2 and IPR2 registers for this purpose. These bits are unimplemented in PIC18F458. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 24.4.3 "FSCM Interrupts in Power-Managed Modes"**.

TABLE 2: PIC18F458 → PIC18F4580 NEW FEATURES (CONTINUED)

Item	Module	Comments
5	ECAN	This is a new module that replaces the CAN module on the PIC18F458. It maintains full backward compatibility with the original CAN module, while providing several new features. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 23.0 "ECAN Module"** and the PIC18F458 data sheet (DS41159), **Section 19.0 "CAN Module"**.
6	EUSART	The USART module in the PIC18F4580 is implemented as an Enhanced USART (EUSART). This module implements additional features, including: • automatic baud rate detection and calibration • automatic wake-up on Sync Break reception and 12-bit Break character transmit, ideally suited for use in Local Interconnect Network bus (LIN bus) systems • a Baud Rate Generator (BRG) that can be configured for 8-bit or 16-bit operation and that supports the EUSART in both Synchronous and Asynchronous modes No code modification is required. Make sure not to modify TXSTA<3> which is unimplemented in the PIC18F458. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 18.0 "Enhanced Universal Synchronous Receiver Transmitter (EUSART)"**.
7	Timer1	1. T1CON<6> (T1RUN) is a new bit in PIC18F4580. This read-only bit indicates whether the device clock is derived from the Timer1 oscillator or not. No code modification is required. 2. The Timer1 oscillator can operate at two levels of power consumption, controlled by the LPT1OSC configuration bit (CONFIG3H<2>). When set, the oscillator operates in Low-Power mode. The bit is clear by default which is compatible with the PIC18F458 device's operation. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 12.0 "Timer1 Module"**.
8	Two-Speed Start-up	The Two-Speed Start-up feature in PIC18F4580 helps to minimize the latency period from oscillator start-up to code execution by allowing the microcontroller to use the internal oscillator as a clock source until the primary clock is available. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 24.3 "Two-Speed Start-up"**.
9	Fail-Safe Clock Monitor	The Fail-Safe Clock Monitor allows the microcontroller to continue operation in the event of an external oscillator failure by automatically switching the device clock to the internal oscillator block. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 24.4 "Fail-Safe Clock Monitor"**.
10	WDT	The nominal WDT period in PIC18F4580 is 4 ms (compared to a typical period of 18 ms from the PIC18F458). This is multiplied by a 16-bit postscaler, the output of which is selected by a 16:1 multiplexor, controlled by bits in Configuration Register 2H. Available periods range from 4 ms to 131.072 seconds (2.18 minutes). For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 24.2 "Watchdog Timer (WDT)"**.

TABLE 2: PIC18F458 → PIC18F4580 NEW FEATURES (CONTINUED)

Item	Module	Comments
11	HLVD	The LVD module is improved as an HLVD module on the PIC18F4580. This module adds the ability to detect excursions above a preset voltage level and generate an interrupt. No code modification is required if HLVDCON<7> is not modified. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 22.0 "High/Low-Voltage Detect (HLVD)"**.
12	PORTE/$\overline{\text{MCLR}}$	The fourth pin of PORTE ($\overline{\text{MCLR}}$/VPP/RE3) is an input-only pin. Its operation is controlled by the MCLRE configuration bit. No code modification is required. The user may select the "$\overline{\text{MCLR}}$ enabled, RE3 disabled" option in the configuration. For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 10.5 "PORTE, TRISE and LATE Registers"**.
13	Enhanced ICD 2	The PIC18F4580 provides enhanced ICD features, including three Breakpoints and Break on GPR address and data match.

TABLE 3: PIC18F458 → PIC18F4580 SFR DIFFERENCES

Address	SFRs	Differences From PIC18F458	Comment
(Multiple)	(Multiple)	Many new registers implemented for the ECAN module in Banks 13, 14 and 15 of the data memory space	Refer to **Section 5.0 "Memory Organization"** and **Section 23.0 "ECAN Module"** of the PIC18F4580 data sheet (DS39637) for a complete list. Also refer to Microchip application note *AN916, "Comparing CAN and ECAN Modules"* (DS00916).
F9Bh	OSCTUNE	Implemented**(1)**	Control bits for internal oscillator block and low-power modes.
FA0h, FA1h, FA2h	PIE2/PIR2/IPR2	Implements bit 7 in PIE2, PIR2 and IPR2**(2)**	Oscillator Fail Interrupt bits (OSCFIE, OSCFIF and OSCFIP).
FACh	TXSTA	Implements bit 3**(2)**	Send Break character bit (SENDB).
FB0h	SPBRGH	Implemented**(1)**	SPBRGH holds the higher byte of the baud rate value in 16-bit mode.
FB8h	BAUDCON	Implemented**(1)**	Baud Rate Generator Control register.
FC0h	ADCON2	Implemented**(1)**	Controls acquisition time selection.
FC1h	ADCON1	Changes in bit allocations**(3)**	For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 19.0 "10-Bit Analog-to-Digital Converter (A/D) Module"**.
FC2h	ADCON0	Changes in bit allocations**(3)**	For more information, refer to the PIC18F4580 data sheet (DS39637), **Section 19.0 "10-Bit Analog-to-Digital Converter (A/D) Module"**.
FCDh	T1CON	Implements bit 6**(2)**	Flag bit indicates whether the device is running from Timer1 oscillator or not (T1RUN).
FD0h	RCON	Implements bit 6**(2)**	This bit is for the software control of BOR. It is available only if BOR is disabled in hardware.
FD2h	HLVDCON	Implements bit 7, register name changes from LVDCON to HLVDCON**(2)**	Bit adds functionality for high-voltage excursion (VDIRMAG).
FD3h	OSCCON	Implements 7 new bits, alters function of existing SCS bit**(2)**	Adds bits to control internal oscillator, Idle mode and clock source selection. Adds flag bits to indicate status of clock sources.

Note 1: Implemented in PIC18F4580 but not implemented in PIC18F458. However, power-up default conditions of these new registers do not have any impact on migration.

2: On power-up default, these extra bits implemented in PIC18F4580 do not have any migration impact.

3: This change may have a migration impact.

TABLE 4: PIC18F458 → PIC18F4580 CONFIGURATION REGISTER DETAILS

Address	Configuration Register	PIC18F458	PIC18F4580
300001h	CONFIG1H	CONFIG1H<2:0>: Oscillator selection bits (FOSC2:FOSC0) CONFIG1H<5>: Clock switch enable bit (OSCSEN)	Implements 3 new bits: CONFIG1H<3:0>: Oscillator selection bits add two more oscillator choices (FOSC3).(1) CONFIG1H<6>: Enables Fail-Safe Clock Monitor (FCMEN).(1) CONFIG1H<7>: Selects the Two-Speed Start-up feature (IESO).(1)
300002h	CONFIG2L	CONFIG2L<1>: Enables or disables BOR. Also implements CONFIG2L<3:2> (BORV1:BORV0) and CONFIG2L<0> (PWRTEN).	CONFIG2L<2:1>: Adds software-controlled BOR options (BOREN1:BOREN0); other bits unchanged.
300003h	CONFIG2H	CONFIG2H<3:1>: WDT postscaler, up to 1:128. Also implements CONFIG2H<0> (WDTEN).	CONFIG2H<4:1>: WDT postscaler, up to 1:32768 (WDTPS3:WDTPS0); CONFIG2H<0> unchanged.
300005h	CONFIG3H	Unimplemented	Adds 3 new bits: CONFIG3H<7>: RE3 port pin can be used as MCLR or as an input port (MCLRE). CONFIG3H<2>: Timer1 can be operated on low or high-power oscillator. By default, high-power oscillator is enabled which is compatible with PIC18F458 (LPT1OSC).(1) CONFIG3H<1>: Selects the configuration of PORTB<4:0> pins on POR. By default, these pins are configured as analog on POR. For compatibility with PIC18F458, the user needs to configure PORTB<4:0> as digital on POR (PBADEN).
300006h	CONFIG4L	Implements CONFIG4L<7> (DEBUG), CONFIG4L<2> (LVP) and CONFIG4L<0> (STVREN).	Adds 2 new bits: CONFIG4L<6>: Enables instruction set extension (XINST).(1) CONFIG4L<4>: Selects boot block size (BBSIZ).(1) Other bits unchanged.
300008h	CONFIG5L	CONFIG5L<0>: Enables code-protect for 000200h-001FFFh.	CONFIG5L<0>: Enables code-protect for 000800h -001FFFh.
300009h	CONFIG5H	CONFIG5H <6>: Enables code-protect for 000000h-0001FFh (boot block).	CONFIG5H<6>: Enables code-protect for 000000h-0007FFh (boot block).
30000Ah	CONFIG6L	CONFIG6L<0>: Enables write-protect for 000200h-001FFFh.	CONFIG6L<0>: Enables write-protect for 000800h-001FFFh.
30000Bh	CONFIG6H	CONFIG6H<6>: Enables write-protect for 000000h-0001FFh (boot block).	CONFIG6H<6>: Enables write-protect for 000000h-0007FFh (boot block).
30000Ch	CONFIG7L	CONFIG7L<0>: Enables table read protection for 000200h-001FFFh (read executed from other blocks).	CONFIG7L<0>: Enables table read protection for 000800h-001FFFh (read executed from other blocks).
30000Dh	CONFIG7H	CONFIG7H<6>: Enables table read protection for 000000h-0001FFh (boot block).	CONFIG7H<6>: Enables table read protection from 000000h-0007FFh (boot block).

Note 1: These configuration bits have a default unprogrammed state of '0'; all other bits default to '1'. This may have an impact on migration.

TABLE 5: PIC18F458 → PIC18F4580 DC CHARACTERISTICS DIFFERENCES

Parameter No.	Parameter	PIC18LF458			PIC18LF4580			Units
		Min.	Typical	Max.	Min.	Typical	Max.	
D005	**BOR**							
	11	1.98	—	2.14	1.96	2.06	2.16	V
	10	2.67	—	2.89	2.64	2.78	2.92	V
	01	4.16	—	4.5	4.11	4.33	4.55	V
	00	4.45	—	4.83	4.41	4.64	4.87	V

Parameter No.	Parameter	PIC18F458			PIC18F4580			Units
		Min.	Typical	Max.	Min.	Typical	Max.	
D005	**BOR**							
	11	NA	—	NA	NA	—	NA	V
	10	NA	—	NA	NA	—	NA	V
	01	4.16	—	4.5	4.11	4.33	4.55	V
	00	4.45	—	4.83	4.41	4.64	4.87	V
D010, D013, D014, D020, D022 and D025	**Supply Current, Power-Down Current and Module Differential Currents**	Because of their architectural differences, the PIC18F458 and PIC18F4580 report these specifications in completely different manners and cannot be directly compared. The PIC18F4580 provides much greater detail to describe DC current consumption in various power-managed modes and at various ambient temperatures. See **Section 27.1 "DC Characteristics"** of the PIC18F458 data sheet (DS41159) and **Section 27.2 "DC Characteristics: Power-Down and Supply Current"** of the PIC18F4580 data sheet (DS39637) for detailed information.						
D420	**HLVD-LVD**							
	LVV = 0000	—	—	—	2.12	2.17	2.22	V
	LVV = 0001	1.98	2.06	2.14	2.18	2.23	2.28	V
	LVV = 0010	2.18	2.27	2.36	2.31	2.36	2.42	V
	LVV = 0011	2.37	2.47	2.57	2.38	2.44	2.49	V
	LVV = 0100	2.48	2.58	2.68	2.54	2.60	2.66	V
	LVV = 0101	2.67	2.78	2.89	2.72	2.79	2.85	V
	LVV = 0110	2.77	2.89	3.01	2.82	2.89	2.95	V
	LVV = 0111	2.98	3.10	3.22	3.05	3.12	3.19	V
	LVV = 1000	3.27	3.41	3.55	3.31	3.39	3.47	V
	LVV = 1001	3.47	3.61	3.75	3.46	3.55	3.63	V
	LVV = 1010	3.57	3.72	3.87	3.63	3.71	3.80	V
	LVV = 1011	3.76	3.92	4.08	3.81	3.90	3.99	V
	LVV = 1100	3.96	4.13	4.30	4.01	4.11	4.20	V
	LVV = 1101	4.16	4.33	4.50	4.23	4.33	4.43	V
	LVV = 1110	4.45	4.64	4.83	4.48	4.59	4.69	V

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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