SLLS098C - MAY 1980 - REVISED FEBRUARY 2004

<ul> <li>Meets or Exceeds Requirements of ANSI TIA/EIA-422-B and ITU</li> </ul>	, ,	OR NS PAC	
Recommendation V.11	٠. ٦	. U	<b>.</b>
3-State, TTL-Compatible Outputs	1A [	1 16	<b>F</b>
Fast Transition Times		<ul><li>2 15</li><li>3 14</li></ul>	] 4A ] 4Y
High-Impedance Inputs	1,2EN		[] 4Z
Single 5-V Supply	2Z [	5 12	] 3,4EN
Power-Up and Power-Down Protection	2Y [	6 11	] 3Z
Tower op and I ower bown I roteotion	2A [	7 10	] 3Y
description/ordering information	GND [	8 9	] 3A

### d

The MC3487 offers four independent differential line drivers designed to meet the specifications of ANSI TIA/EIA-422-B and ITU Recommendation V.11. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a low logic level. Internal circuitry is provided to ensure the high-impedance state at the differential outputs during power-up and power-down transition times, provided the output enable is low.

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-V supply.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	MC3487N	MC3487N
0°C to 70°C	colo D	Tube	MC3487D	MC2407
0°C to 70°C	SOIC - D	Tape and reel	MC3487DR	MC3487
	SOP - NS	Tape and reel	MC3487NSR	MC3487

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE** (each driver)

INDUT	OUTPUT	OUTI	PUTS
INPUT	ENABLE	Υ	Z
Н	Н	Н	L
L	Н	L	Н
Х	L	Z	Z

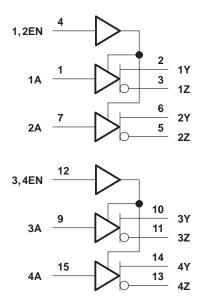
H = TTL high level, L = TTL low level, X = irrelevant, Z = High impedance



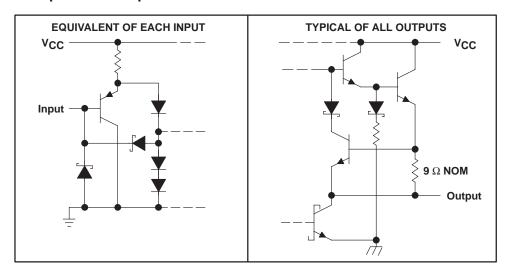
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## logic diagram (positive logic)



# schematics of inputs and outputs



# MC3487 QUADRUPLE DIFFERENTIAL LINE DRIVER

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub> (see Note 1)			8 V
Input voltage, V <sub>I</sub>			5.5 V
Output voltage, VO			7 V
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3)	: D package		73°C/W
	N package		67°C/W
	NS package		64°C/W
Operating virtual junction temperature, T <sub>J</sub>			. 150°C
Storage temperature range, T <sub>stq</sub>		–65°C t	to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential output voltage, VOD, are with respect to the network ground terminal.
  - 2. Maximum power dissipation is a function of  $T_J(max)$ ,  $\bar{\theta}_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
TA	Operating free-air temperature	0		70	°C

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# electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TES1	MIN	MAX	UNIT			
VIK	Input clamp voltage	I <sub>I</sub> = -18 mA				-1.5	V	
Vон	High-level output voltage	V <sub>IL</sub> = 0.8 V,	V <sub>IH</sub> = 2 V,	I <sub>OH</sub> = -20 mA	2.5		V	
VOL	Low-level output voltage	V <sub>IL</sub> = 0.8 V,	V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 48 mA		0.5	V	
IVODI	Differential output voltage	$R_L = 100 \Omega$ ,	See Figure 1		2			
Δ V <sub>OD</sub>	Change in magnitude of differential output voltage <sup>†</sup>	R <sub>L</sub> = 100 Ω,	See Figure 1			±0.4	V	
Voc	Common-mode output voltage <sup>‡</sup>	$R_L = 100 \Omega$ ,	See Figure 1			3	V	
Δ V <sub>OC</sub>	Change in magnitude of common-mode output voltage†	R <sub>L</sub> = 100 Ω,	See Figure 1			±0.4	٧	
	0		V <sub>O</sub> = 6 V			100		
Ю	Output current with power off	ACC = 0	$V_0 = -0.25 \text{ V}$			-100	μΑ	
	High importance state systems arranged	Outrut anables at 0.01/	V <sub>O</sub> = 2.7 V			100		
loz	High-impedance-state output current	Output enables at 0.8 V	V <sub>O</sub> = 0.5 V			-100	μΑ	
II	Input current at maximum input voltage	V <sub>I</sub> = 5.5 V				100	μА	
lіН	High-level input current	V <sub>I</sub> = 2.7 V	V <sub>I</sub> = 2.7 V				μΑ	
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0.5 V				-400	μΑ	
los	Short-circuit output current§	V <sub>I</sub> = 2 V			-40	-140	mA	
laa	Supply ourrent (all drivers)	Outputs disabled				105	m A	
Icc	Supply current (all drivers)	Outputs enabled,	No load			85	mA	

<sup>†</sup>Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

## switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V

	PARAMETER	TES	T CONDITIONS	MIN	MAX	UNIT
<sup>t</sup> PLH	Propagation delay time, low- to high-level output	C <sub>I</sub> = 15 pF,	See Figure 2		20	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	OL = 15 μr,	See Figure 2		20	110
t <sub>sk</sub>	Skew time	$C_L = 15 pF$ ,	See Figure 2		6	ns
t <sub>t</sub> (OD)	Differential-output transition time	C <sub>L</sub> = 15 pF,	See Figure 3		20	ns
<sup>t</sup> PZH	Output enable time to high level	C. F0.5F	Soo Figure 4		30	
tPZL	Output enable time to low level	C <sub>L</sub> = 50 pF,	See Figure 4		30	ns
<sup>t</sup> PHZ	Output disable time from high level	$C_{1} = 50 \text{ pF},$	See Figure 4		25	20
<sup>t</sup> PLZ	Output disable time from low level	CL = 50 pr,	See Figure 4		30	ns



<sup>‡</sup> In ANSI Standard TIA/EIA-422-B, V<sub>OC</sub>, which is the average of the two output voltages with respect to ground, is called output offset voltage, V<sub>OS</sub>.

<sup>§</sup> Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

### PARAMETER MEASUREMENT INFORMATION

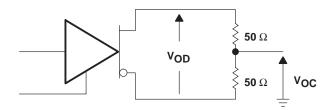
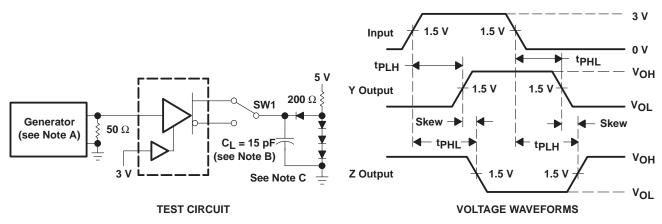


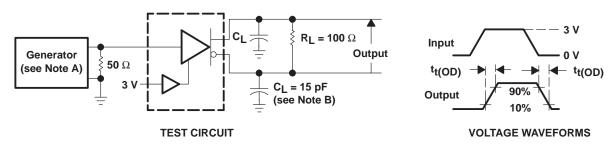
Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $t_f \le 5$  ns,  $t_f \le 5$  ns, PRR  $\le 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .

- B. CL includes probe and stray capacitance.
- C. All diodes are 1N916 or 1N3064.

Figure 2. Test Circuit and Voltage Waveforms

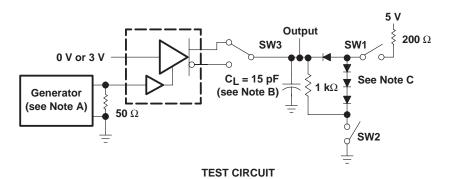


NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $t_f \le 5$  ns,  $t_f \le 5$  ns, PRR  $\le 1$  MHz, duty cycle = 50%,  $Z_{\Omega} = 50 \ \Omega$ .

B. C<sub>L</sub> includes probe and stray capacitance.

Figure 3. Test Circuit and Voltage Waveforms

### PARAMETER MEASUREMENT INFORMATION



Output Output Enable Input 3 V Enable Input 1.5 V <sup>t</sup>PHZ SW1 Closed SW2 Open SW1 Closed 1.5 V SW2 Closed Output Output VOL <sup>t</sup>PZH → tPLZ ۷он Output SW1 Closed Output SW1 Open SW2 Closed **SW2 Closed** 

#### **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $t_T \le 5$  ns,  $t_T \le 5$  ns,  $t_T \le 5$  ns, PRR  $\le 1$  MHz, duty cycle = 50%,  $t_T \le 5$  ns,  $t_$ 

- B. C<sub>L</sub> includes probe and stray capacitance.
- C. All diodes are 1N916 or 1N3064.

Figure 4. Driver Test Circuit and Voltage Waveforms







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#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
MC3487D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
MC3487N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC3487NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC3487NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC3487NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>&</sup>lt;sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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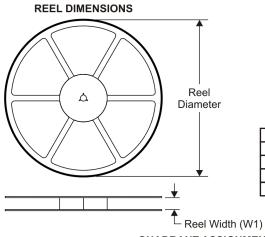
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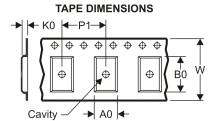
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# PACKAGE MATERIALS INFORMATION

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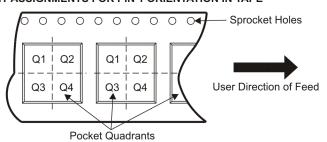
### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC3487DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MC3487NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC3487DR	SOIC	D	16	2500	346.0	346.0	33.0
MC3487NSR	SO	NS	16	2000	346.0	346.0	33.0

### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDS0-G16)

### PLASTIC SMALL OUTLINE

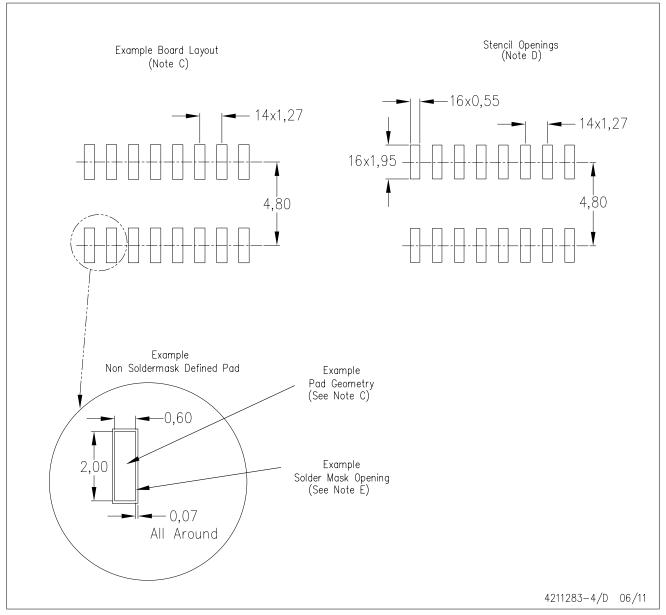


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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