

## Highly Integrated Current Mode PWM Controller with Latch

### TURES

- ◆ Latch Plug-off Protection with External Triggering
- ◆ Built-in Soft Start Function
- ◆ Very Low Startup Current
- ◆ Frequency Reduction and Burst Mode Control for Energy Saving
- ◆ Built-in Frequency Shuffling
- ◆ Programmable Switching Frequency
- ◆ Built-in Synchronous Slope Compensation
- ◆ Cycle-by-Cycle Current Limiting
- ◆ All Pins Floating Protection
- ◆ High Voltage CMOS Process with Excellent ESD Protection
- ◆ Current Mode Control
- ◆ Built-in Leading Edge Blanking (LEB)
- ◆ Constant Power Limiting
- ◆ Audio Noise Free Operation
- ◆ VDD OVP & Clamp
- ◆ VDD Under Voltage Lockout (UVLO)

### APPLICATIONS

Offline AC/DC Flyback Converter for

- ◆ AC/DC Power Adaptors
- ◆ Open-frame SMPS
- ◆ Print Power, Scanners, and Motor Drivers

### GENERAL DESCRIPTION

SF1560 is a high performance, highly integrated current mode PWM controller for medium to large offline flyback converter applications.

In SF1560, the PWM switching is internally trimmed to tight range. To improve EMI performance, the IC integrates frequency shuffling function to reduce conduction EMI emission of a power supply. The IC also integrates Constant Power Limiting block to achieve constant output power limit from 90VAC to 264VAC.

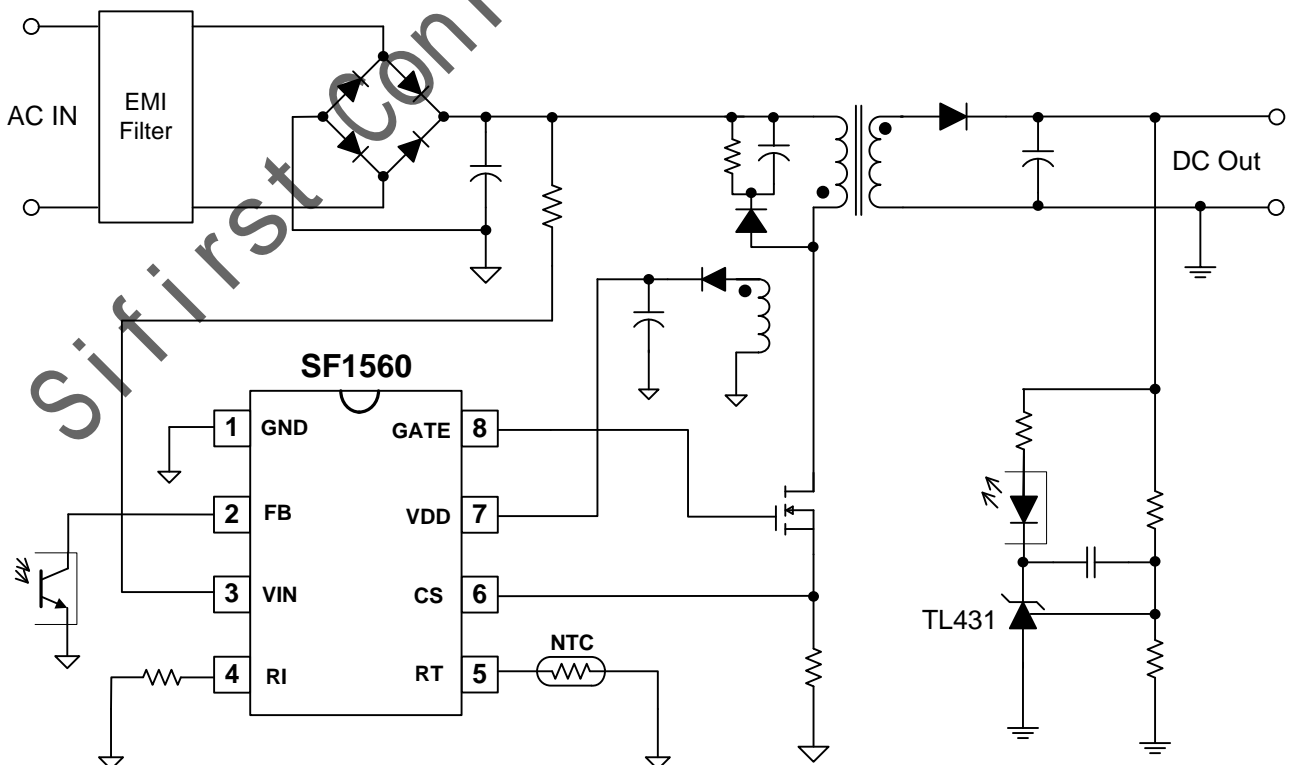
Under light load conditions, a green mode function can continuously decrease the switching frequency. Under zero-load conditions, the power supply enters into burst mode and provides excellent efficiency without audio noise generated. This green mode function enables power supplies to meet international power conservation requirements.

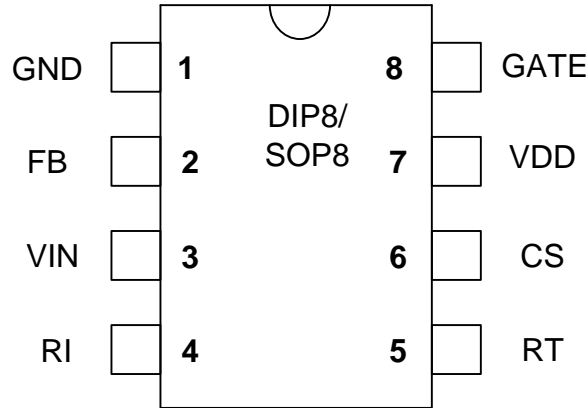
SF1560 integrates functions and protections of Under Voltage Lockout (UVLO), VDD Over Voltage Protection (OVP), Soft Start, External Programmable Over Temperature Protection (OTP), Cycle-by-cycle Current Limiting (OCP), Over Load Protection (OLP), All Pins Floating Protection, RI Pin Short-to-GND Protection, GATE Clamping, VDD Clamping, Leading Edge Blanking (LEB).

In SF1560, the OTP and VDD OVP is latch plug-off protection. The other protection functions are auto-recovery mode protection.

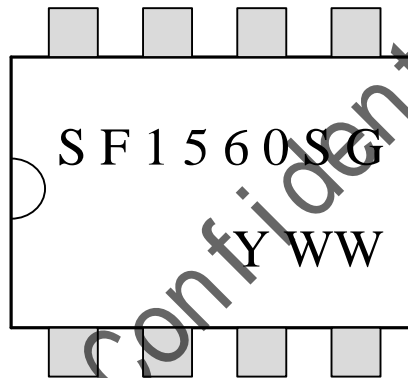
SF1560 is available in SOP-8 and DIP-8 packages.

### TYPICAL APPLICATION

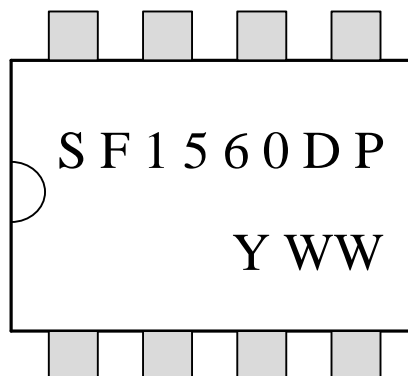


**Pin Configuration**

**Ordering Information**

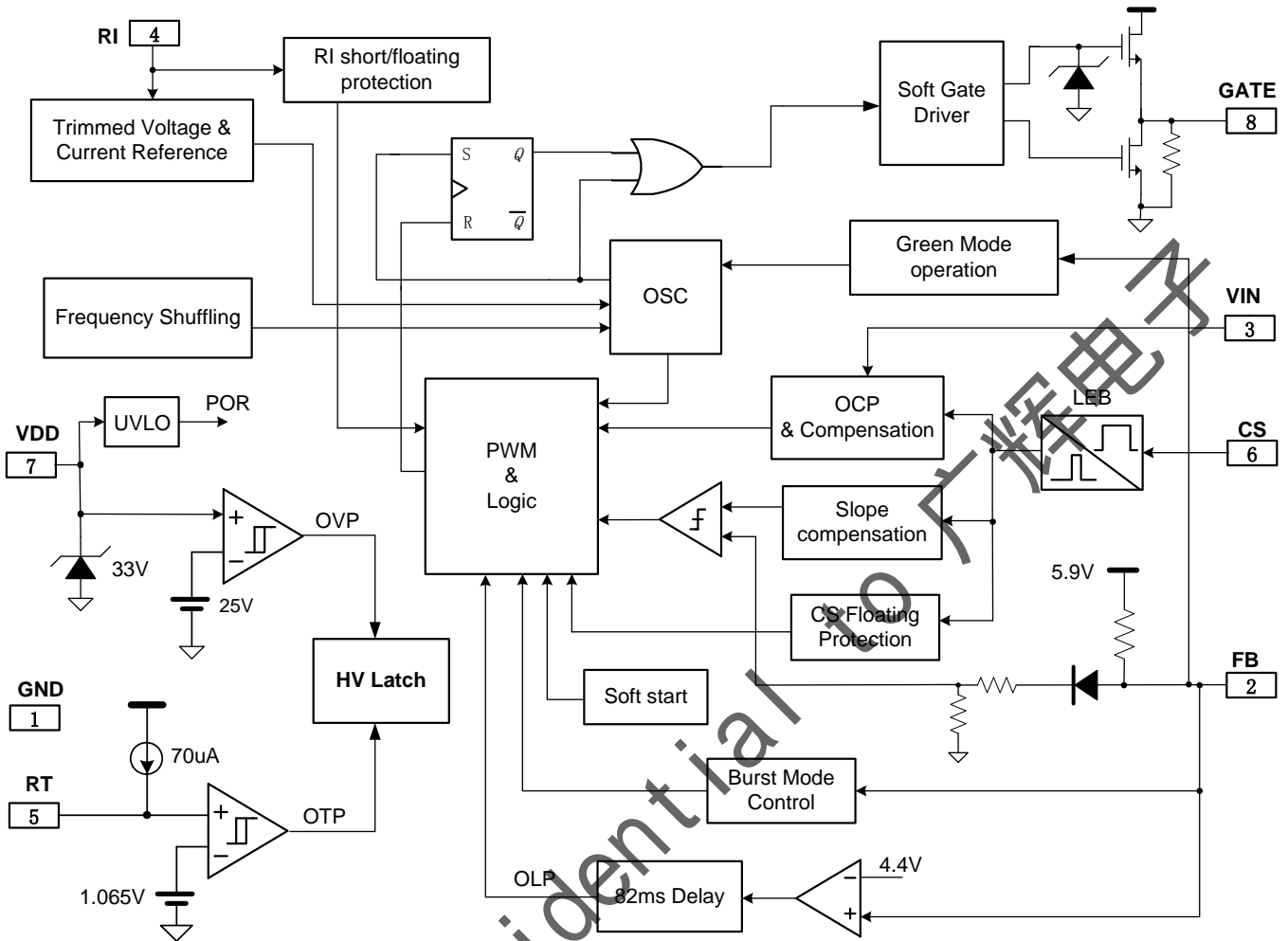
| Part Number | Top Mark | Package |       | Tape & Reel |
|-------------|----------|---------|-------|-------------|
| SF1560SG    | SF1560SG | SOP8    | Green |             |
| SF1560SGT   | SF1560SG | SOP8    | Green | Yes         |
| SF1560DP    | SF1560DP | DIP8    | RoHS  |             |

**Marking Information**


YWW: Year&amp;Week code



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**Block Diagram**

**Pin Description**

| Pin Num | Pin Name | I/O | Description   |
|---------|----------|-----|---|
| 1       | GND      | P   | IC ground pin.  |
| 2       | FB       | I   | Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is generated by this pin voltage and the current sense signal at Pin 6. |
| 3       | VIN      | I   | This pin is connected to the rectified line input via a large value resistor. The function of the pin is for startup and line voltage sensing.  |
| 4       | RI       | I   | Set the switching frequency by connecting a resistor between RI and GND. This pin has floating/short-to-GND protection.   |
| 5       | RT       | I   | This pin is for over temperature protection by connecting an external NTC resistor to ground. Once the pin voltage drops below a fixed limit of 1.065V, PWM output will be disabled.    |
| 6       | CS       | I   | Current sense input pin.  |
| 7       | VDD      | P   | IC power supply pin.  |
| 6       | GATE     | O   | Totem-pole gate driver output to drive the external MOSFET.   |

**Absolute Maximum Ratings** (Note 1)

| Parameter                              | Value      | Unit |
|--|------------|------|
| VDD/VIN DC Supply Voltage              | 33         | V    |
| VDD DC Clamp Current                   | 10         | mA   |
| GATE pin                               | 20         | V    |
| FB, RI, RT, CS voltage range           | -0.3 to 7  | V    |
| Package Thermal Resistance (DIP-8)     | 90         | °C/W |
| Package Thermal Resistance (SOP-8)     | 150        | °C/W |
| Maximum Junction Temperature           | 150        | °C   |
| Operating Temperature Range            | -40 to 85  | °C   |
| Storage Temperature Range              | -65 to 150 | °C   |
| Lead Temperature (Soldering, 10sec.)   | 260        | °C   |
| ESD Capability, HBM (Human Body Model) | 3          | kV   |
| ESD Capability, MM (Machine Model)     | 250        | V    |

**Recommended Operation Conditions** (Note 2)

| Parameter                     | Value     | Unit |
|-------------------------------|-----------|------|
| Supply Voltage, VDD           | 11 to 23  | V    |
| Operating Frequency           | 50 to 130 | kHz  |
| Operating Ambient Temperature | -40 to 85 | °C   |

**ELECTRICAL CHARACTERISTICS**

 (T<sub>A</sub> = 25°C, RI=24K ohm, VDD=18V, if not otherwise noted)

| Symbol                                      | Parameter                                | Test Conditions                      | Min  | Typ  | Max  | Unit |
|---|--|--------------------------------------|------|------|------|------|
| <b>Supply Voltage Section (VDD Pin)</b>     |  |                                      |      |      |      |      |
| I_Startup                                   | VDD Start up Current                     | VDD =15V, Measure current into VDD   |      | 5    | 20   | uA   |
| I_VDD_Op                                    | Operation Current                        | V <sub>FB</sub> =3V, GATE=1nF        |      | 2.5  | 3.5  | mA   |
| UVLO(ON)                                    | VDD Under Voltage Lockout Exit (Startup) |                                      | 15.5 | 16.5 | 17.5 | V    |
| UVLO(OFF)                                   | VDD Under Voltage Lockout Enter          |                                      | 9.5  | 10.5 | 11.5 | V    |
| VDD_OVP_ON                                  | VDD Over Voltage Protection trigger      |                                      | 23.5 | 25   | 26.5 | V    |
| VDD_OVP_Hys                                 | VDD OVP Hysteresis                       |                                      |      | 2    |      | V    |
| V <sub>DD</sub> _Clamp                      | VDD Zener Clamp Voltage                  | I(V <sub>DD</sub> ) = 5mA            |      | 33   |      | V    |
| T_Softstart                                 | System Soft Start Time                   |                                      |      | 3    |      | mSec |
| <b>Feedback Input Section (FB Pin)</b>      |  |                                      |      |      |      |      |
| A <sub>VCS</sub>                            | PWM Input Gain                           | $\Delta V_{FB} / \Delta V_{CS}$      |      | 2.8  |      | V/V  |
| V <sub>FB</sub> _Open                       | FB Open Voltage                          |                                      |      | 5.9  |      | V    |
| I <sub>FB</sub> _Short                      | FB short circuit current                 | Short FB pin to GND, measure current |      | 1.2  |      | mA   |
| V <sub>FB</sub> _min_duty                   | FB under voltage gate clock is off.      |                                      |      | 1.0  |      | V    |
| V <sub>TH</sub> _PL                         | Power Limiting FB Threshold Voltage      |                                      |      | 4.4  |      | V    |
| T <sub>D</sub> _PL                          | Power limiting Debounce Time             | Note 3                               |      | 82   |      | mSec |
| Z <sub>FB</sub> _IN                         | Input Impedance                          |                                      |      | 5    |      | Kohm |
| <b>Current Sense Input Section (CS Pin)</b> |  |                                      |      |      |      |      |
| T_blanking                                  | SENSE Input Leading Edge Blanking Time   |                                      |      | 250  |      | nSec |
| V <sub>th</sub> _OC_max                     | Internal current limiting threshold      | I(VIN)=0                             | 0.85 | 0.9  | 0.95 | V    |
| T <sub>D</sub> _OC                          | Over Current                             | GATE=1nF                             |      | 120  |      | nSec |

|   |                                 |                                     |       |       |       |      |
|---|---------------------------------|-------------------------------------|-------|-------|-------|------|
|   | Detection and Control Delay     |                                     |       |       |       |      |
| <b>Oscillator Section (RI Pin)</b>          |                                 |                                     |       |       |       |      |
| F <sub>osc</sub>                            | Normal Oscillation Frequency    |                                     | 60    | 65    | 70    | KHZ  |
| ΔF(shuffle)/F <sub>osc</sub>                | Frequency shuffling range       | Note 4                              | -4    |       | 4     | %    |
| Δf_Temp                                     | Frequency Temperature Stability | -40°C to 125°C (Note 4)             |       | 5     |       | %    |
| Δf_VDD                                      | Frequency Voltage Stability     | VDD = 12-23V (Note 4)               |       | 5     |       | %    |
| Duty_max                                    | Maximum Duty cycle              |                                     | 75    | 80    | 85    | %    |
| RI_range                                    | Operating RI Range              |                                     | 12    | 24    | 60    | Kohm |
| V_RI_open                                   | RI open voltage                 |                                     |       | 2.0   |       | V    |
| F_BM  | Burst Mode Base Frequency       |                                     |       | 22    |       | KHz  |
| <b>Over Temperature Protection (RT Pin)</b> |                                 |                                     |       |       |       |      |
| I_RT  | Output Current of RT Pin        |                                     |       | 70    |       | uA   |
| V <sub>TH_OTP</sub>                         | OTP Threshold Voltage           |                                     | 1.015 | 1.065 | 1.115 | V    |
| V <sub>TH_OTP_OFF</sub>                     | OTP Release Voltage             |                                     |       | 1.165 |       | V    |
| V <sub>TH_OTP_Hys</sub>                     | OTP Hysteresis                  |                                     |       | 0.1   |       | V    |
| V_RT_Open                                   | RT Pin Open Voltage             |                                     |       | 4.6   |       | V    |
| <b>Latch Protection</b>                     |                                 |                                     |       |       |       |      |
| V <sub>Latch_release</sub>                  | VDD Latch Release Voltage       |                                     | 5.5   | 6     | 6.5   | V    |
| I <sub>vdd(latch)</sub>                     | VDD Current when latch off      | VDD= V <sub>Latch_release</sub> +1V |       | 40    |       | uA   |
| <b>Gate Drive Output (GATE Pin)</b>         |                                 |                                     |       |       |       |      |
| VOL   | Output Low Level                | I <sub>o</sub> = 20 mA (sink)       |       |       | 0.3   | V    |
| VOH   | Output High Level               | I <sub>o</sub> = 20 mA (source)     | 11    |       |       | V    |
| Gate_Clamp                                  | Output Clamp Voltage Level      | VDD=24V                             |       | 18    |       | V    |
| T <sub>r</sub>                              | Output Rising Time              | GATE = 1nF                          |       | 120   |       | nSec |
| T <sub>f</sub>                              | Output Falling Time             | GATE = 1nF                          |       | 50    |       | nSec |

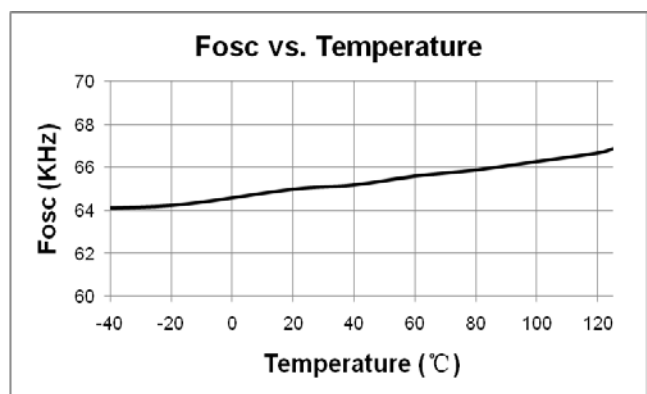
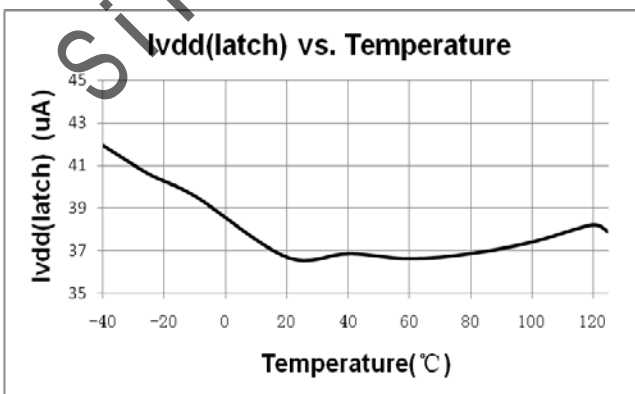
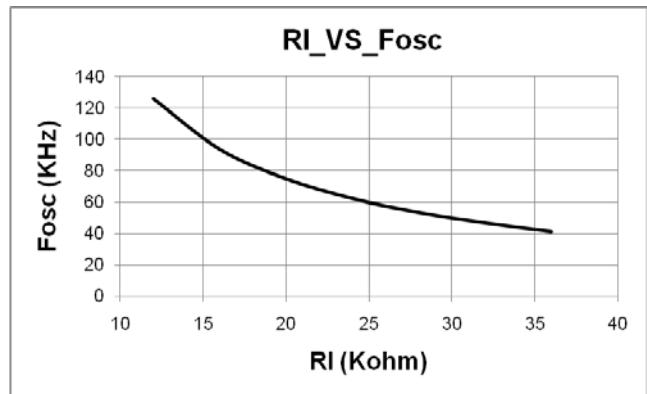
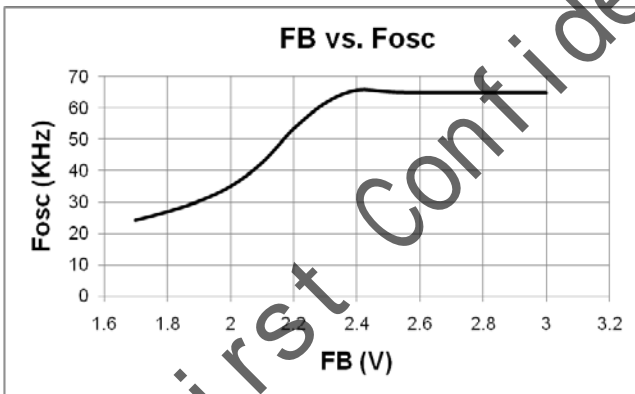
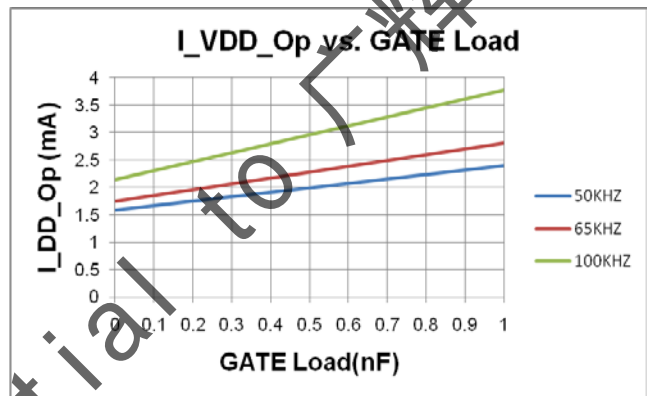
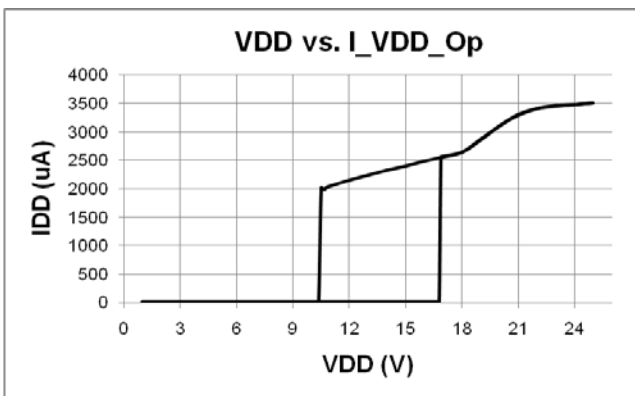
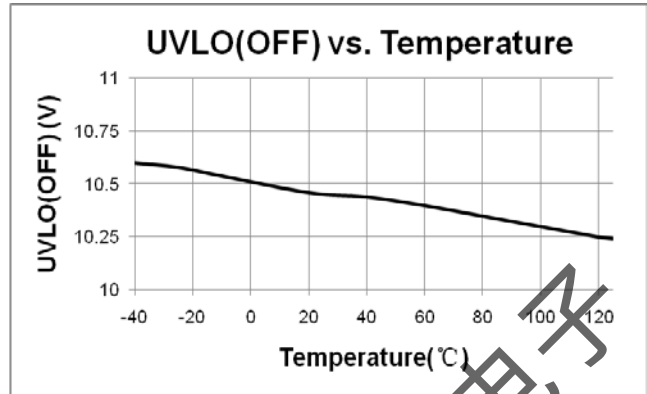
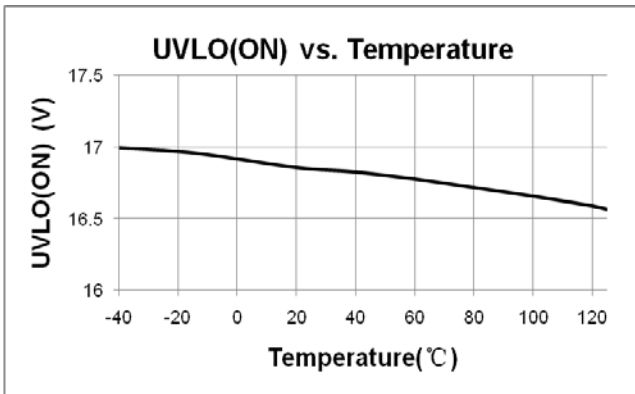
**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

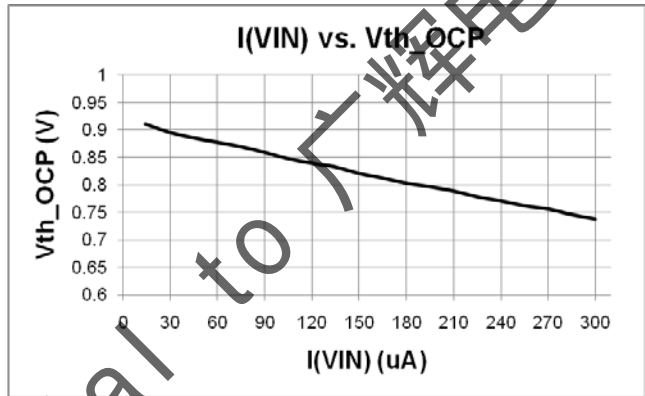
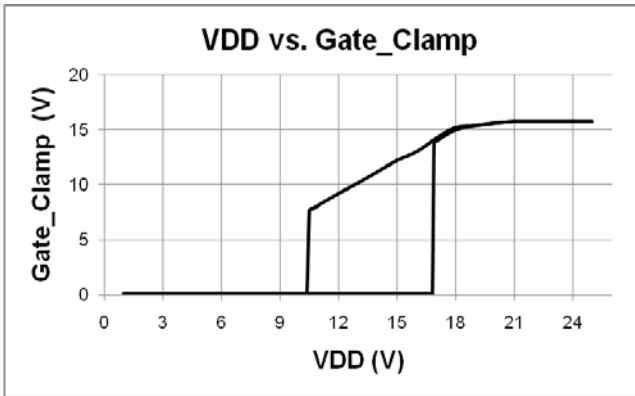
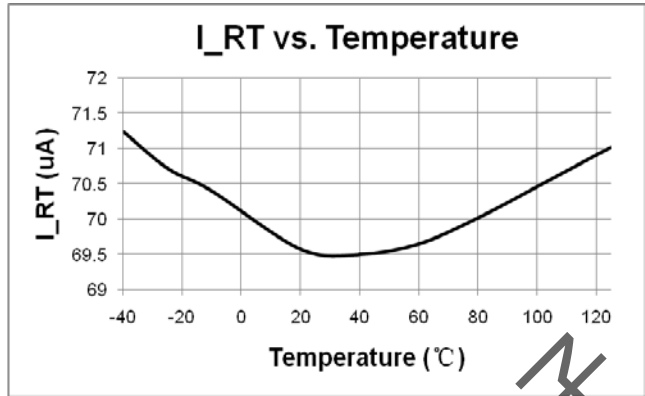
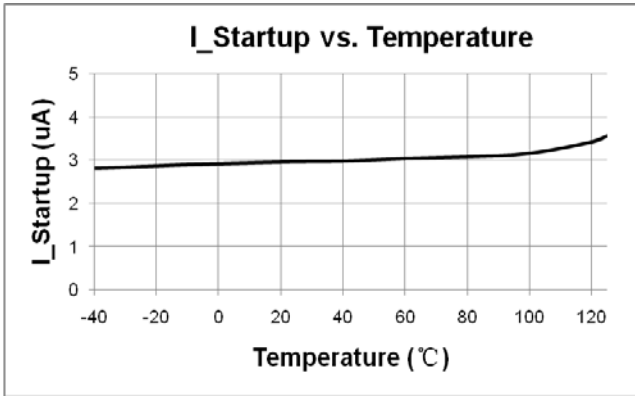
**Note 2.** The device is not guaranteed to function outside its operating conditions.

**Note 3.** The OLP debounce time is proportional to the period of switching cycle.

**Note 4.** Guaranteed by design.

CHARACTERIZATION PLOTS





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## OPERATION DESCRIPTION

SF1560 is a high performance, highly integrated current mode PWM controller for medium to large offline flyback converter applications. The built-in advanced energy saving with high level protection features improves the SMPS reliability and performance without increasing the system cost.

### ◆ Low Startup Current & Operating Current

The typical startup current of SF1560 is only about 5uA so that a high resistance startup resistor can be used to minimize power loss. For an AC/DC adapter with universal input range, a 2M Ohm, 1/8W startup resistor can be used to provide a fast startup and yet low power dissipation design solution.

The operating current in SF1560 is as small as 2.3mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

### ◆ Soft Start

SF1560 features an internal 3ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

### ◆ Oscillator with Frequency Shuffling

Connecting a resistor from RI pin to GND according to the equation below to program the normal switching frequency:

$$F_{\text{osc}}(\text{KHz}) = \frac{1560}{\text{RI}(\text{K}\Omega)}$$

It can typically operate between 50kHz to 130kHz. To improve system EMI performance, SF1560 operates the system with  $\pm 4\%$  frequency shuffling around setting frequency.

### ◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver. Thus, external RC filter with a small time constant is enough for current sensing.

### ◆ Frequency Reduction for Green Mode Operation

When the loading is light, the IC will automatically reduce the PWM switching frequency to achieve high efficiency. In the whole frequency reduction process, there is no audio noise generated.

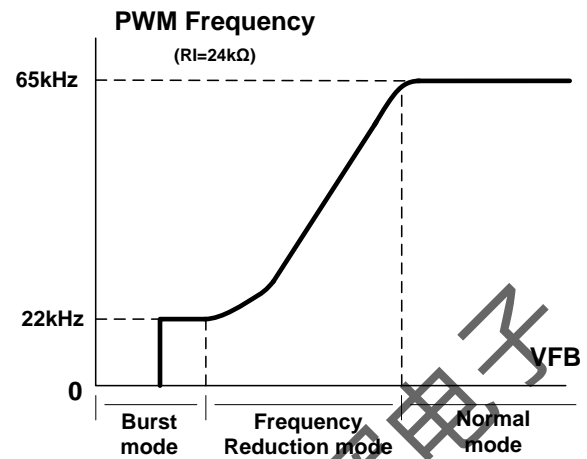


Fig.1

### ◆ Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below  $V_{\text{skip}}$ , SF1560 will stop switching and output voltage starts to drop, which causes the VFB to rise. Once VFB rises above  $V_{\text{skip}}$ , switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

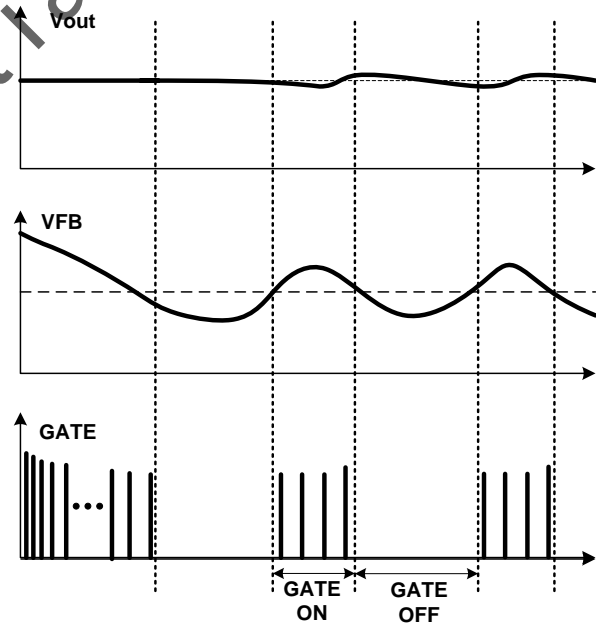


Fig.2

### ◆ Synchronous Slope Compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. In SF1560, the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.



### ◆ Constant Power Limiting

In flyback converter applications, the GATE drive delay can cause system OPP (Over Power Point) to change according to the AC line input voltage. In SF1560, a OPP compensation block is integrated to achieve constant max. output power capability over universal AC input range. Since the pin VIN is connected to the rectified input line voltage through the startup resistor, the current flowed into the VIN pin indicates the line voltage. Using the information of VIN pin current, the IC adjusts the cycle-by-cycle OCP threshold according to the following equation:

$$V_{TH\_OCP}(V) = 0.9 - 0.0278 \times RI \times I(VIN)$$

In this way, the system OPP variation can be compensated automatically.

### ◆ Over Temperature Protection with Latch Shutdown

By connecting a NTC resistor in series with a regular resistor between RT and GND, the over temperature protection (OTP) can be realized. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current  $I_{RT}$  flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP comparator is triggered and shut down the PWM signal when the sensed input voltage is lower than the comparator threshold voltage. OTP is a **latched shutdown** mode.

### ◆ VDD OVP(Over Voltage Protection) with Latch Shutdown

VDD OVP (Over Voltage Protection) is implemented in SF1560 and it is a protection of **latch shutdown** mode.

### ◆ RT Pin Used as Latch Shutdown Input Control

RT pin can also be used as a control input to implement system latch shutdown function. By externally forcing a level on pin RT less than 1.065V(typical), SF1560 can be permanently latched off. To resume normal operation, VDD voltage should go below 6V(typical), which implies to unplug the SMPS from the mains.

### ◆ Auto Recovery Mode Protection

As shown in Fig.3, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered from the auxiliary winding. When VDD falls to UVLO(off) (typical 10.5V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.3. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

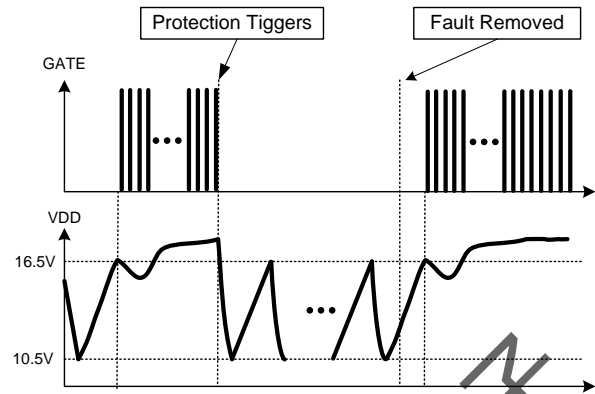


Fig.3

### ◆ Over Load Protection (OLP) / Over Current Protection (OCP) / Over Power Protection (OPP) / Open Loop Protection (OLP)

When OLP/OCP/OPP/Open Loop occurs, a fault is detected. If this fault is present for more than 82ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above, as shown in Fig.4. The 82ms delay time is to prevent the false trigger from the power-on and turn-off transient.

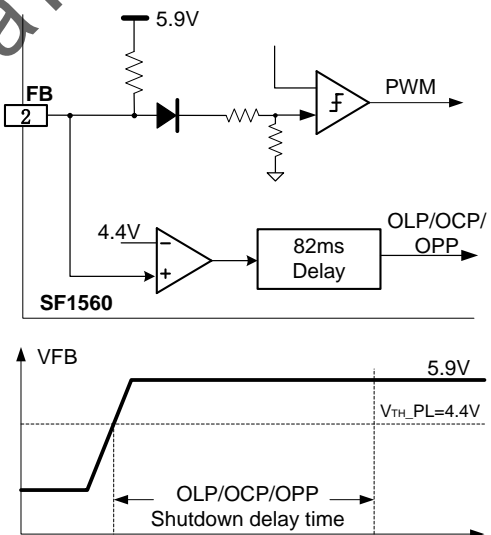


Fig.4

### ◆ All Pins Floating Protection and RI Pin Short-to-GND Protection

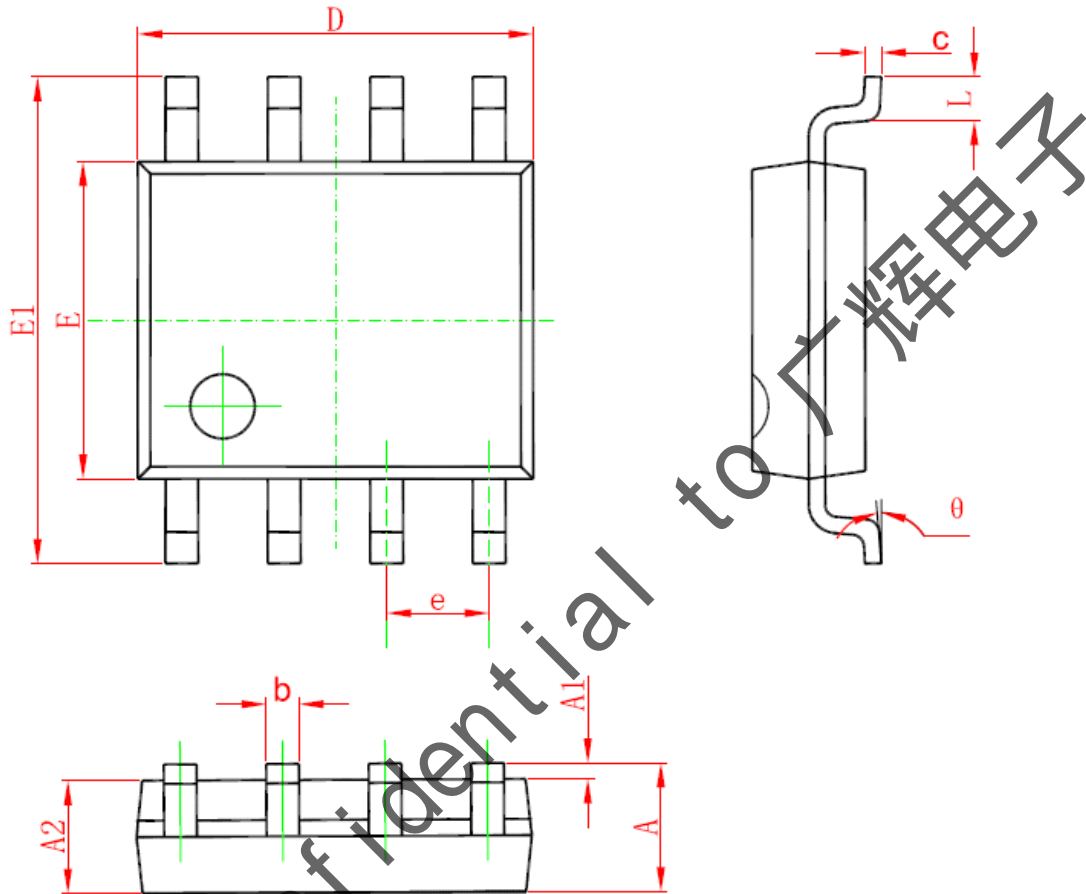
In SF1560, if pin floating situation or RI pin short-to-GND occurs, the protection is triggered immediately and the system will experience the process of auto-recovery mode protection.

### ◆ Soft Gate Drive

SF1560 has a fast totem-pole gate driver with 800mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 17.5V clamp is added for MOSFET gate protection at higher than expected VDD input. A soft driving waveform is implemented to minimize EMI.

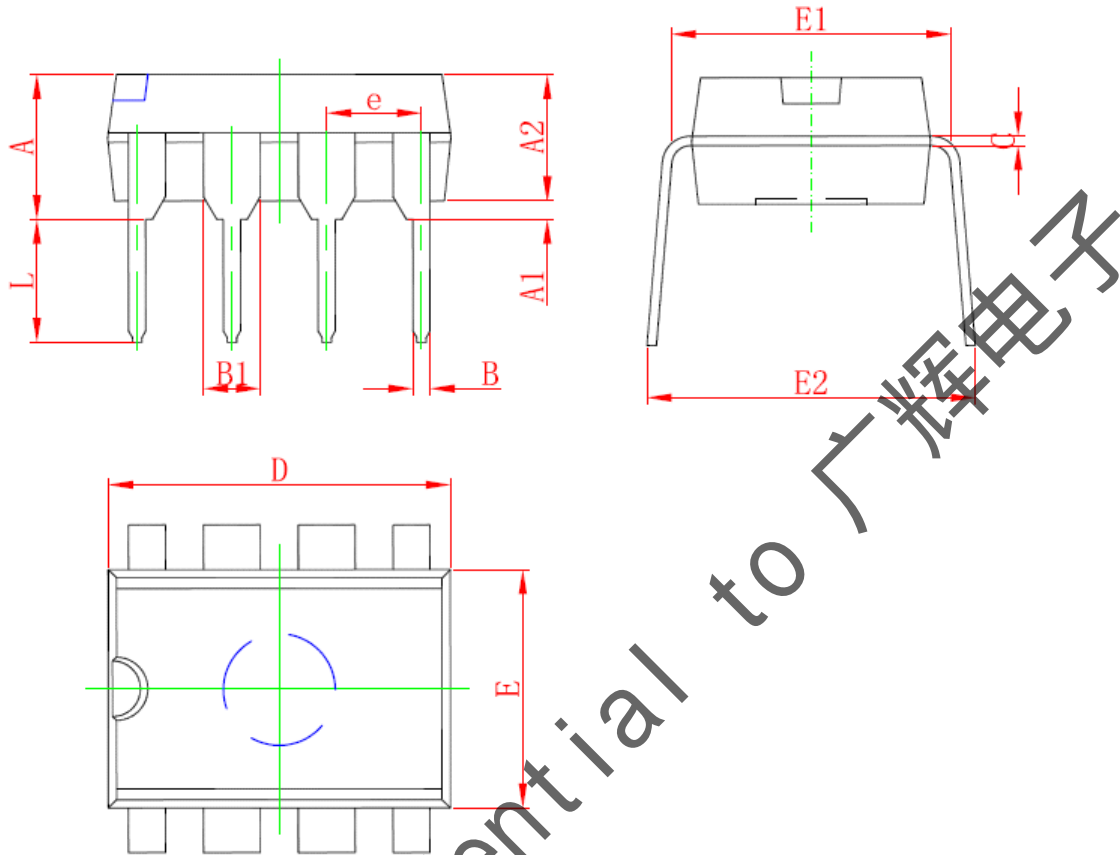
PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



| Symbol | Dimensions In Millimeters |       | Dimensions In Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min                       | Max   | Min                  | Max   |
| A      | 1.350                     | 1.750 | 0.053                | 0.069 |
| A1     | 0.050                     | 0.250 | 0.002                | 0.010 |
| A2     | 1.250                     | 1.650 | 0.049                | 0.065 |
| b      | 0.310                     | 0.510 | 0.012                | 0.020 |
| c      | 0.170                     | 0.250 | 0.006                | 0.010 |
| D      | 4.700                     | 5.150 | 0.185                | 0.203 |
| E      | 3.800                     | 4.000 | 0.150                | 0.157 |
| E1     | 5.800                     | 6.200 | 0.228                | 0.244 |
| e      | 1.270 (BSC)               |       | 0.05 (BSC)           |       |
| L      | 0.400                     | 1.270 | 0.016                | 0.050 |
| θ      | 0°                        | 8°    | 0°                   | 8°    |

DIP8 PACKAGE OUTLINE DIMENSIONS



| Symbol | Dimensions In Millimeters |       | Dimensions In Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min                       | Max   | Min                  | Max   |
| A      | 3.710                     | 4.310 | 0.146                | 0.170 |
| A1     | 0.510                     |       | 0.020                |       |
| A2     | 3.200                     | 3.600 | 0.126                | 0.142 |
| B      | 0.380                     | 0.570 | 0.015                | 0.022 |
| B1     | 1.524 (BSC)               |       | 0.06 (BSC)           |       |
| C      | 0.204                     | 0.360 | 0.008                | 0.014 |
| D      | 9.000                     | 9.400 | 0.354                | 0.370 |
| E      | 6.200                     | 6.600 | 0.244                | 0.260 |
| E1     | 7.320                     | 7.920 | 0.288                | 0.312 |
| e      | 2.540 (BSC)               |       | 0.100 (BSC)          |       |
| L      | 3.000                     | 3.600 | 0.118                | 0.142 |
| E2     | 8.400                     | 9.000 | 0.331                | 0.354 |

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