

4 Line ESD Protection Diode Array

UESD54B SC70-5 / SC88A / SOT353

General Description

The UESD54B of TVS diode array is designed to protect sensitive electronics from damage or latch-up due to ESD, for use in applications where board space is at a premium. It is unidirectional device and may be used on lines where the signal polarities are above ground, each device will protect up to four lines.

TVS diodes are solid-state devices feature large cross-sectional area junctions for conducting high transient currents, specifically for transient suppression. It offers desirable characteristics for board level protection including fast response time, low operating, low clamping voltage, and no device degradation.

The UESD54B may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

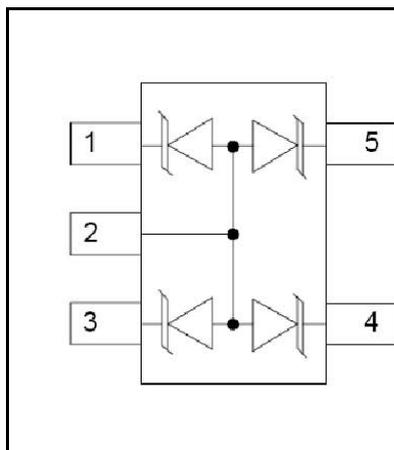
Applications

Cellular Handsets & Accessories
 Cordless Phones
 Personal Digital Assistants (PDA's)
 Notebooks & Handhelds
 Portable Instrumentation
 Digital Cameras
 Peripherals
 MP3 Players

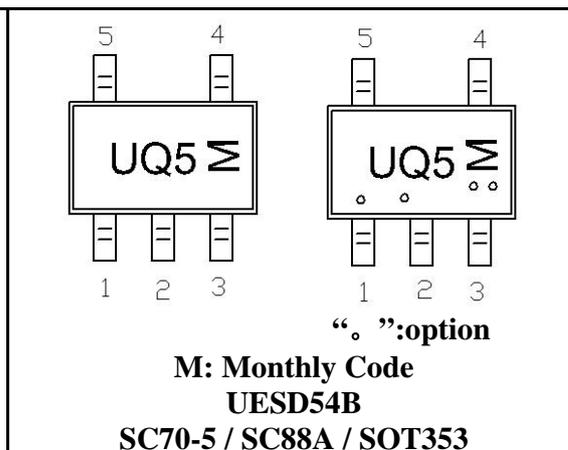
Features

Transient protection for data & power lines to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
 Protect four I/O lines
 Ultra-small SC70-5 / SC88A / SOT353
 Working Voltages: 5V
 Low Leakage current
 Low operating and clamping voltage
 Solid-state silicon avalanche technology

Pin Configurations



Top View



Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UESD54B	5.0V	SC70-5 / SC88A / SOT353	4	UQ5	3000/7 inch Reel

Absolute Maximum Ratings

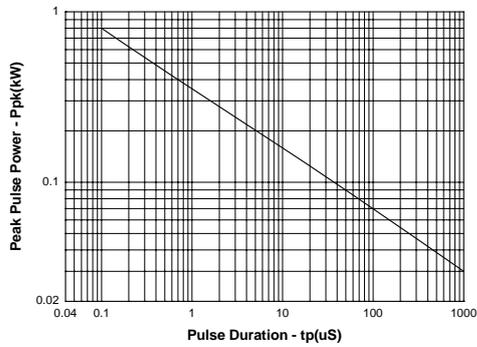
RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20 \mu s$) @ $T_A \leq 25^\circ C$	P_{PK}	140	Watts
Peak Pulse Current ($t_p = 8/20 \mu s$)	I_{PP}	11	A
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	325	$^\circ C/W$
Lead Soldering Temperature	T_L	260(10 sec.)	$^\circ C$
Operating Temperature	T_J	-55 to +125	$^\circ C$
Storage Temperature	T_{STG}	-55 to +125	$^\circ C$
Maximum Junction Temperature	T_{JMAX}	150	$^\circ C$

Electrical Characteristics

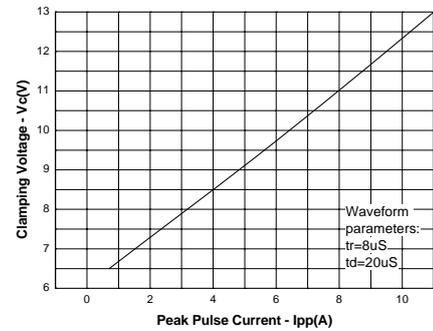
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	6	6.8	7.2	V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T=25^\circ C$			0.1	μA
Clamping Voltage	V_C	$I_{PP} = 5A, t_p = 8/20\mu S$			9.1	V
		$I_{PP} = 11A, t_p = 8/20\mu S$			13	
Junction Capacitance	C_J	Pin 1, 3, 4, 5 to 2 $V_R = 0V, f = 1MHz$		40	50	pF
Junction Capacitance	C_J	Pin 1, 3, 4, 5 to 2 $V_R = 2.5V, f = 1MHz$		30	40	pF

Typical Operating Characteristics

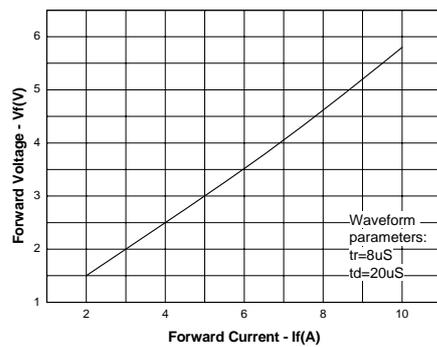
Non-Repetitive Peak Pulse Power vs. Pulse Time



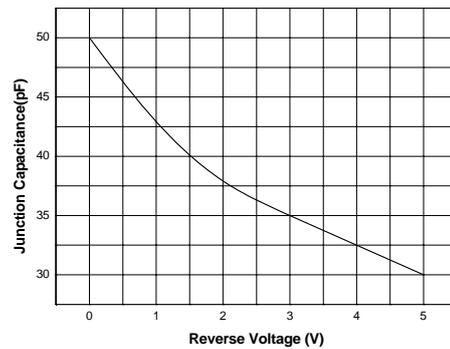
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage



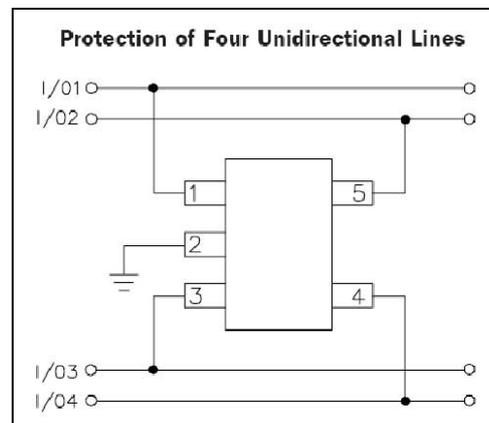
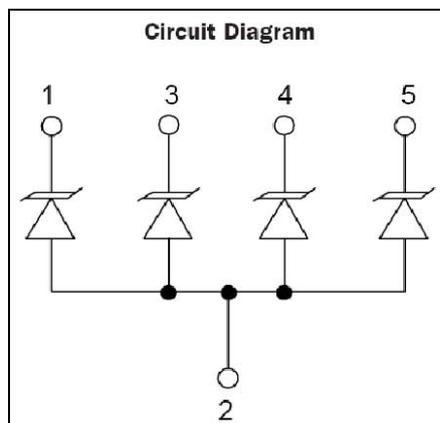
Applications Information

UESD54B ESD protection diode array is designed to protect quad data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode band should be placed towards the line that is to be protected.

Device Connection for Protection of Quad Data Lines

The Quad TVS Diode Array is designed to protect up to four unidirectional data lines. The device is connected as follows:

Unidirectional protection of four I/O lines is achieved by connecting pins 1, 3, 4 and 5 to the data lines. Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.



Circuit Board Layout Recommendations for Suppression of ESD

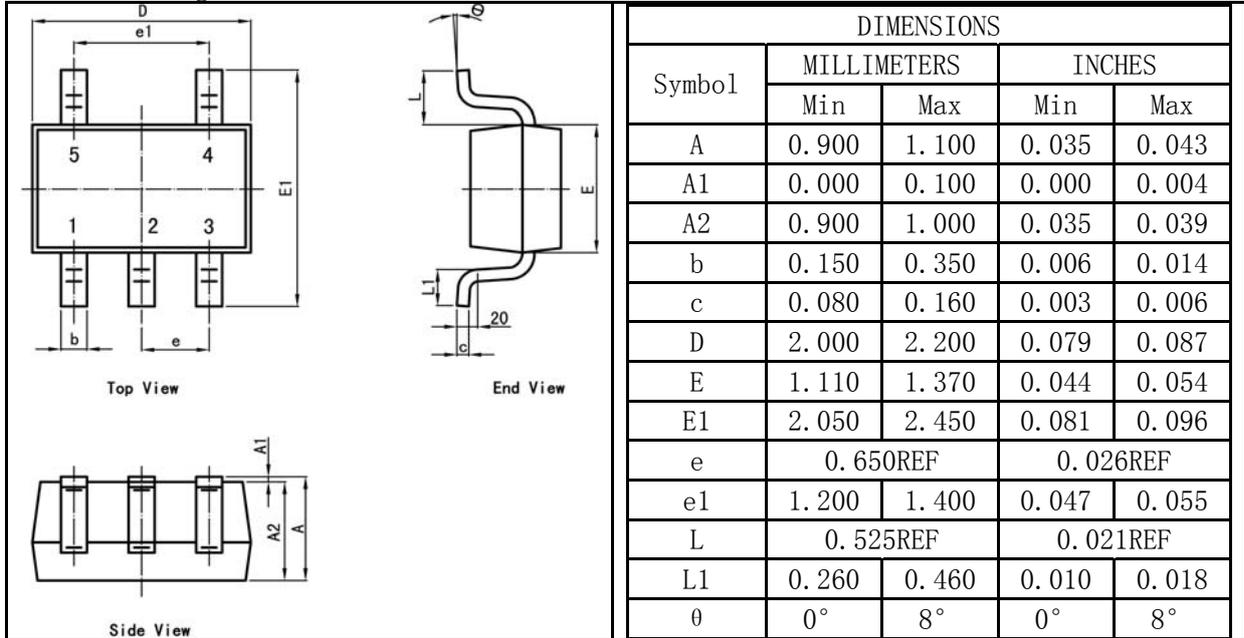
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
- Keep parallel signal paths to a minimum.
- Avoid running protection conductors in parallel with unprotected conductor.
- Minimize all printed-circuit board conductive loops including power and ground loops.
- Avoid using shared transient return paths to a common ground point.

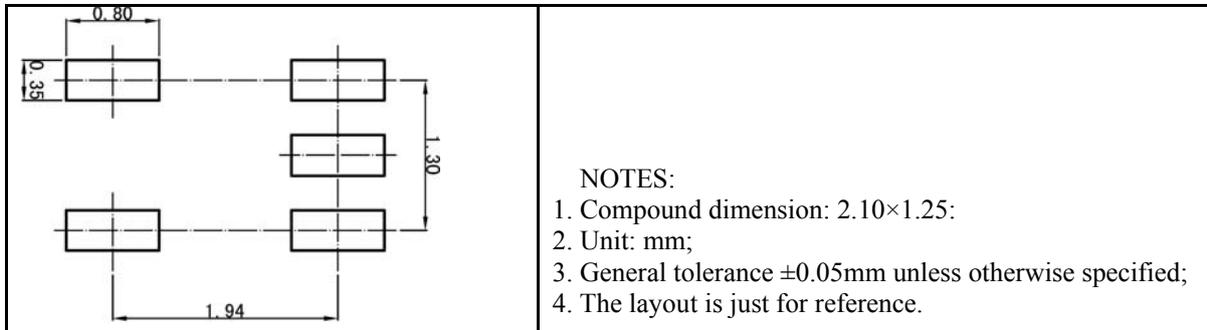
Package Information

UESD54B SC70-5 / SC88A / SOT353

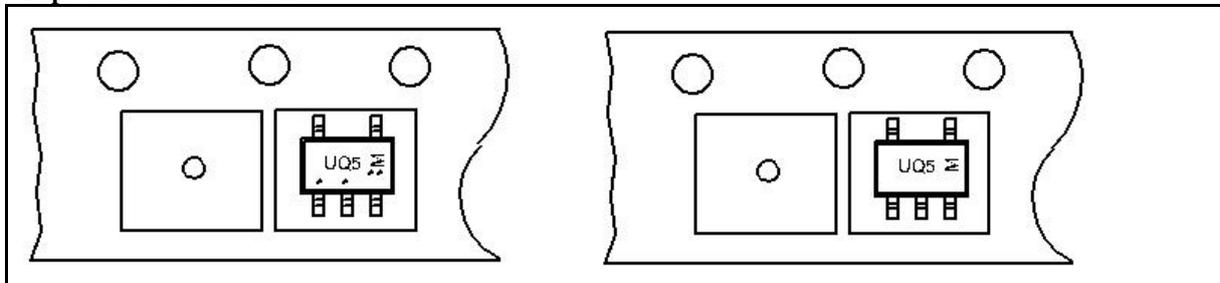
Outline Drawing



Land Pattern



Tape and Reel Orientation



IMPORTANT NOTICE

The information in this document has been carefully reviewed and is believed to be accurate. Nonetheless, this document is subject to change without notice. Union assumes no responsibility for any inaccuracies that may be contained in this document, and makes no commitment to update or to keep current the contained information, or to notify a person or organization of any update. Union reserves the right to make changes, at any time, in order to improve reliability, function or design and to attempt to supply the best product possible.

Union Semiconductor, Inc
Add: 7F, No. 5, Bibo Road, Shanghai 201203
Tel: 021-51097928
Fax: 021-51026018
Website: www.union-ic.com