Tri Axis Gyroscope & Accelerometer

Preliminary Technical Data

ADIS16350

FEATURES

Tri-axis gyroscope
- **±320 degrees/second measurement range**
- **14-bit resolution**

Tri-axis accelerometer
- **±10g measurement range**
- **14-bit resolution**

350Hz Bandwidth
Factory calibrated sensitivity and bias
Digitally controlled bias calibration
Digitally controlled sample rate
Digitally controlled filtering
Programmable condition monitoring, alarms
Auxiliary digital I/O
Digitally activated self-test
Programmable power management
Embedded Temperature Sensor
SPI®-compatible serial interface
Auxiliary 12-bit ADC input and DAC output
Single-supply operation: +4.75V to +5.25 V
2000 *g* powered shock survivability

APPLICATIONS

Guidance and control
Platform control and stabilization
Motion control and analysis
Inertial Measurement Units
General Navigation
Image stabilization
Robotics

GENERAL DESCRIPTION

The ADIS16350 ***i***Sensor™ provides complete tri axis inertial sensing (both angular and linear motion) in a compact module fully ready for system integration. With Analog Devices' iMEMS™ sensor technology at its core, the ADIS16350 includes embedded processing for sensor calibration and tuning. An SPI interface allows for simple system interface and programming.

The SPI port provides access to the following embedded sensors: X, Y, and Z axis angular rate; X, Y, and Z axis linear acceleration; Internal Temperature; Power Supply; and an Auxiliary analog input. The inertial sensors are precision aligned across axes, and are calibrated for offset and sensitivity.

System interfacing is simplified with the following additional programmable features:

- In-system Bias Auto Calibration
- Digital Filtering and Sample Rate
- Self Test
- Power Management
- Condition Monitoring
- Auxiliary Digital I/O

The ultra compact module measures 22.7 mm × 23.2 mm × 22.9 mm, plus mounting extensions.

FUNCTIONAL BLOCK DIAGRAM

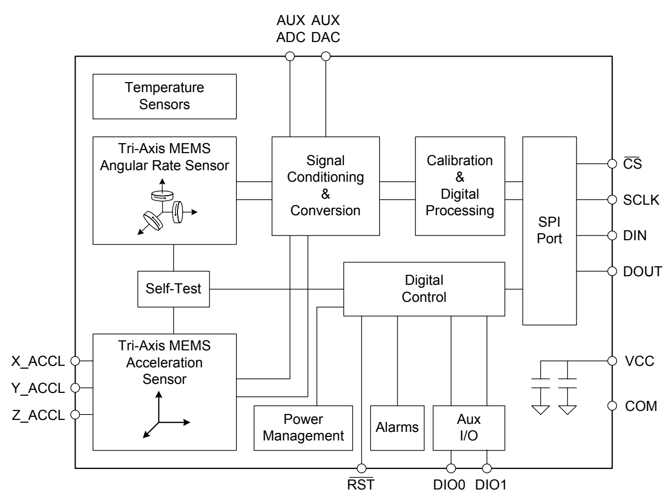

Figure 1.

Rev. PrB

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

10/06—Revision PrA: Initial Version

01/07—Revision PrB

SPECIFICATIONS

T_A = −40ºC to +85°C, V_{CC} = 5.0 V, Angular Rate = 0°/s, Dynamic Range 320°/sec, ±1g, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
GYRO SENSITIVITY	Each axis				
Dynamic Range	Full-scale range over specifications range	±320			°/s
Initial	25°C, Dynamic range = ±320°/sec	0.07233	0.07326	0.07400	°/s/LSB
	25°C, Dynamic range = ±160°/sec		0.03663		°/s/LSB
	25°C, Dynamic range = ±80°/sec		0.01832		°/s/LSB
Sensitivity Drift over Temp	-20°C to 75°C		±250		ppm/ºC
Axis Non-orthogonality	25°C, difference from 90 degrees ideal		±0.02		degree
Axis Misalignment	25°C, relative to base-plate & guide pins		±0.1		degree
Non-Linearity	Best fit straight line		±0.1		% of FS
Voltage Sensitivity	Vcc = +4.75 to +5.25V		+0.1		%/V
GYRO BIAS					
In Run Bias Stability	25°C, 1 σ		0.016		°/s
Turn on – Turn on Bias Stability	25°C, 1 σ		0.05		°/s
Angular Random Walk	25°C		3.6		°/√hr
Zero Rate Bias Drift over Temp	-20°C to 75°C		±0.06		°/s/°C
g Sensitivity	Any Axis		0.1		°/s/*g*
Voltage Sensitivity	V_{CC} = 4.75 V to 5.25 V		0.2		°/s /V
GYRO NOISE PERFORMANCE					
Output Noise	At 25°C, ±320 º/s Dynamic range, no filtering		TBD		°/s rms
	At 25°C, ±160 º/s Dynamic range, minimum 4 tap filter setting		TBD		°/s rms
	At 25°C, ±80 º/s Dynamic range, minimum 16 tap filter setting		TBD		°/s rms
Rate Noise Density	At 25°C, f= 25Hz, no average		0.05		°/s/√Hz rms
GYRO FREQUENCY RESPONSE					
Sensor Bandwidth			350		Hz
Sensor Resonant Frequency			14		kHz
GYRO SELF-TEST STATE					
Change for positive stimulus	Relative to nominal output	439	721	1092	LSB
Change for negative stimulus	Relative to nominal output	-439	-721	-1092	LSB
ACCELEROMETER SENSITIVITY	Each axis				
Dynamic Range		±10			g
Initial	@25°C	TBD	2.522	TBD	mg/LSB
Sensitivity Drift Over Temperature			TBD		ppm/°C
Axis Non-orthogonality	25°C, difference from 90 degrees ideal		TBD		degree
Axis Misalignment	25°C, relative to base-plate & guide pins		TBD		degree
Nonlinearity	Best Fit Straight Line		±0.2		% of FS
ACCELEROMETER BIAS					
0g Offset	@25°C	TBD		TBD	mg
0g Offset Over Temperature			TBD		mg/°C

Table 2. (Continued)

Parameter	Conditions	Min	Typ	Max	Unit
ACCELEROMETER NOISE PERFORMANCE					
Output Noise	@25°C, no filtering		TBD		LSB rms
Noise Density	@25°C, no filtering		0.072		LSB/√Hz rms
ACCELEROMETER FREQUENCY RESPONSE					
Sensor Bandwidth			350		Hz
Sensor Resonant Frequency			10		kHz
ACCELEROMETER SELF-TEST STATE					
Output Change When Active	@25°C		TBD		LSB
TEMPERATURE SENSOR					
Output at 25°C			0		LSB
Scale Factor			6.88		LSB/°C
ADC INPUT					
Resolution			12		Bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±4		LSB
Gain Error			±2		LSB
Input Range		0		2.5	V
Input Capacitance	During acquisition		20		pF
DAC OUTPUT	5 kΩ/100 pF to GND				
Resolution			12		Bits
Relative Accuracy	For Code 101 to Code 4095		4		LSB
Differential Nonlinearity			1		LSB
Offset Error			±5		mV
Gain Error			±0.5		%
Output Range			0 to 2.5		V
Output Impedance			2		Ω
Output Settling Time			10		µs
LOGIC INPUTS					
Input High Voltage, V_{INH}		2.0			V
Input Low Voltage, V_{INL}				0.8	V
	For −CS signal when used to wake up from SLEEP mode			0.55	V
Logic 1 Input Current, I_{INH}	V_{IH} = 3.3 V		±0.2	±10	µA
Logic 0 Input Current, I_{INL}	V_{IL} = 0 V				
All except $\overline{RST}$			−40	−60	µA
$\overline{RST}$ [1]			−1		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
SLEEP TIMER					
Timeout Period[2]		0.5		128	Sec
FLASH MEMORY					
Endurance[3]		20,000			Cycles
Data Retention[4]	T_J = 55°C	20			Years

[1] The $\overline{RST}$ pin has an internal pull-up.
[2] Guaranteed by design
[3] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[4] Retention lifetime equivalent at junction temperature (T_J) 55°C as per JEDEC Standard 22 Method A117. Retention lifetime decreases with junction temperature.

Table 3. (Continued)

CONVERSION RATE					
Minimum Conversion Time			1.22		ms
Maximum Conversion Time			2.42		Sec
Maximum Throughput Rate			819.2		SPS
Minimum Throughput Rate			0.413		SPS
START-UP TIME[1]					
Initial power up			150		ms
Sleep mode recovery			3		ms
POWER SUPPLY					
Operating Voltage Range V_{CC}		4.75	5.0	5.25	V
Power Supply Current	Normal mode at 25°C		33		mA
	Fast mode at 25°C		57		mA
	Sleep mode at 25°C		750		µA

[1] This is defined as the time from wake-up to the first conversion. This time does not include sensor settling time, which is dependent on the filter settings

TIMING SPECIFICATIONS

T_A = +25°C, VCC = +5.0 V, angular rate = 0°/sec, unless otherwise noted.

Table 4.

Parameter	Description	Min[1]	Typ	Max[1]	Unit
f_{SCLK}	Fast mode, SMPL_TIME ≤ 0x09 (f_S ≥ 164 Hz)	0.01		2.5	MHz
	Normal mode, SMPL_TIME ≥ 0x0A (f_S ≤ 149 Hz)	0.01		1.0	MHz
$t_{DATARATE}$	Chip select period, fast mode, SMPL_TIME ≤ 0x09 (f_S ≥ 164 Hz)	40			µs
	Chip select period, normal mode, SMPL_TIME ≥ 0x0A (f_S ≤ 149 Hz)	100			µs
t_{CS}	Chip select to clock edge	48.8			ns
t_{DAV}	Data output valid after SCLK falling edge[2]			100	ns
t_{DSU}	Data input setup time before SCLK rising edge	24.4			ns
t_{DHD}	Data input hold time after SCLK rising edge	48.8			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge[3]	5			ns

[1] Guaranteed by design, not production tested.
[2] The MSB presents an exception to this parameter. The MSB clocks out on the falling edge of $\overline{CS}$. The rest of the DOUT bits are clocked after the falling edge of SCLK and are governed by this specification.
[3] This parameter may need to be expanded to allow for proper capture of the LSB. After $\overline{CS}$ goes high, the DOUT line goes into a high impedance state.

TIMING DIAGRAMS

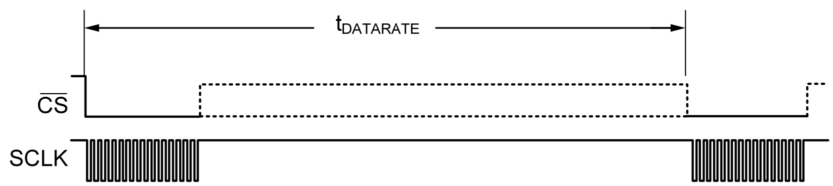

Figure 2. SPI Chip Select Timing

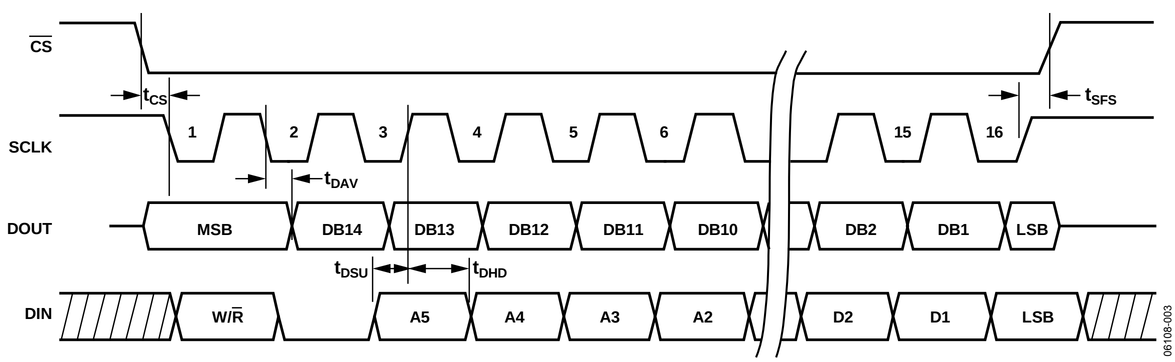

Figure 3. SPI Timing, Utilizing SPI Settings Typically Identified as Phase = 1, Polarity = 1

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Acceleration (Any Axis, Unpowered)	2000 *g*
Acceleration (Any Axis, Powered)	2000 *g*
Vcc to COM	−0.3 V to +6.0 V
Digital Input/Output Voltage to COM	−0.3 V to +5.3 V
Analog Inputs to COM	−0.3 V to VCC + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C[1]

[1] Extended exposure to temperatures outside of the specified temperature range of -40°C to +85°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of -40°C to +85°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
TBD	TBD	TBD	TBD

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

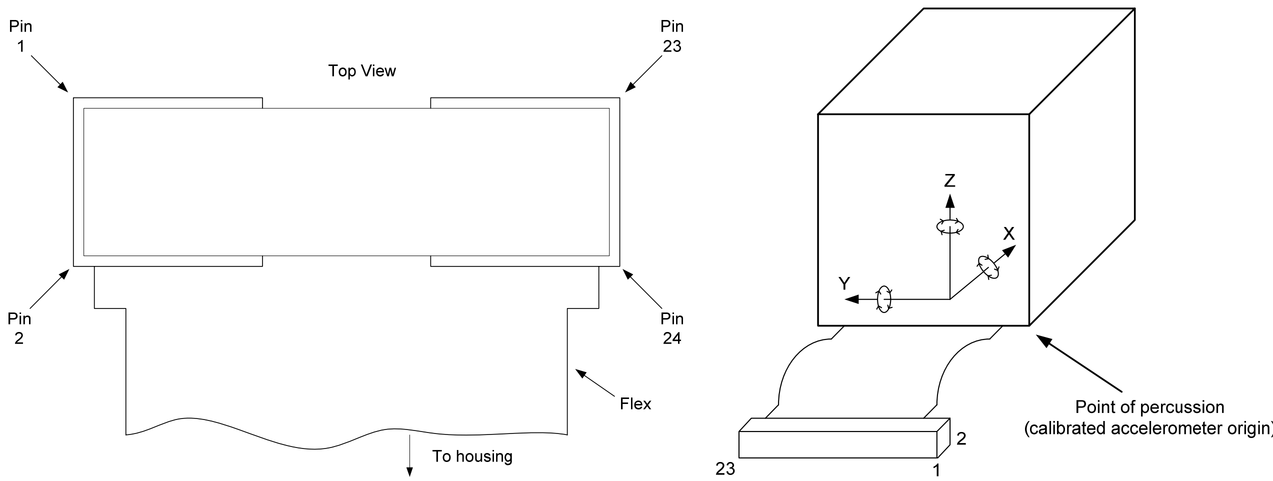

Figure 4. Pin Configuration, Connector Top View

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	DNC	N/A	Do not connect
2	DNC	N/A	Do not connect
3	SCLK	I	SPI, Serial clock
4	DOUT	O	SPI, Data output
5	DIN	I	SPI, Data input
6	~CS	I	SPI, Chip Select
7	DIO0	I/O	Digital I/O
8	~RST	I	Reset
9	DIO1	I/O	Digital I/O
10	VCC	S	Power supply
11	VCC	S	Power supply
12	VCC	S	Power supply
13	GND	S	Power ground
14	GND	S	Power ground
15	GND	S	Power ground
16	DNC	N/A	Do not connect
17	DNC	N/A	Do not connect
18	DNC	N/A	Do not connect
19	DNC	N/A	Do not connect
20	AUX_DAC	O	Auxiliary, 12-bit, DAC Output
21	AUX_ADC	I	Auxiliary, 12-bit, ADC Input
22	Y_ACCL	O	Y-Axis acceleration
23	X_ACCL	O	X-Axis acceleration
24	Z_ACCL	O	Z-Axis acceleration

[1] S = supply, O = output, I = input.

THEORY OF OPERATION

OVERVIEW

The ADIS16350 integrates three orthogonal axes of gyroscope sensors with three orthogonal axes of accelerometer sensors, creating the basic, "Six degrees of freedom" (6DOF) in one single package. The accelerometers are oriented along the axis of rotation for each gyroscope. These six sensing elements are coupled together by an aluminum structure that couples external force and motion. Each sensor's output signal is sampled using an ADC, and then the digital data is fed into a proprietary digital processing circuit. The digital processing circuit applies the correction tables to each sensor's output, manages the I/O function using a simple register structure and serial interface, and provides many other features that simplify system-level designs.

GYROSCOPE SENSOR

The core angular rate sensor (gyroscope) used in the ADIS16350 operates on the principle of a resonator gyro. Two polysilicon sensing structures each contain a dither frame, which is electrostatically driven to resonance. This provides the necessary velocity element to produce a Coriolis force during rotation. At two of the outer extremes of each frame, orthogonal to the dither motion, are movable fingers placed between fixed fingers to form a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed to a series of gain and demodulation stages that produce the electrical rate signal output.

ACCELEROMETER SENSOR

The core acceleration sensor used in the ADIS16350 is a surface micromachined polysilicon structure built on top of the silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against acceleration forces. Deflection of the structure is measured using a differential capacitor that consists of independent fixed plates and central plates attached to the moving mass. An acceleration will deflect the beam and unbalance the differential capacitor, resulting in a differential output that is fed to a series of gain and demodulation stages that produce the electrical rate signal output.

FACTORY CALIBRATION

The ADIS16350 provides a factory-calibration that simplifies the process of integrating it into system level designs. This calibration provides correction for initial sensor bias and sensitivity, power supply variation, axial alignment, and linear acceleration (gyroscopes). An extensive, 3-axis characterization, provides the basis for generating correction tables for each individual sensor.

AUXILIARY ADC FUNCTION

The auxiliary ADC function integrates a standard 12-bit ADC into the ADIS16350 to digitize other system-level analog signals. The output of the ADC can be monitored through the AUX_ADC control register, as defined in Table 9. The ADC is a 12-bit successive approximation converter. The output data is presented in straight binary format with the full-scale range extending from 0 V to 2.5 V.

Figure 5 shows the equivalent circuit of the analog input structure of the ADC. The input capacitor (C1) is typically 4 pF and can be attributed to parasitic package capacitance. The two diodes provide ESD protection for the analog input. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. This causes the diodes to become forward-biased and to start conducting. The diodes can handle 10 mA without causing irreversible damage. The resistor is a lumped component that represents the on resistance of the switches. The value of this resistance is typically 100 Ω. Capacitor C2 represents the ADC sampling capacitor and is typically 16 pF.

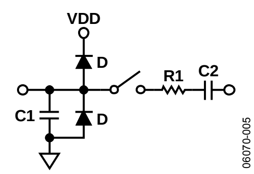

Figure 5. Equivalent Analog Input Circuit
Conversion Phase: Switch Open
Track Phase: Switch Closed

For ac applications, removing high frequency components from the analog input signal is recommended by the use of a low-pass filter on the analog input pin.

In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input must be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. When no input amplifier is used to drive the analog input, the source impedance should be limited to values lower than 1 kΩ.

BASIC OPERATION

The ADIS16350 is designed for simple integration into system designs, requiring only a 5.0 V power supply and a four-wire, industry standard serial peripheral interface (SPI). All outputs and user-programmable functions are handled by a simple register structure. Each register is 16 bits in length and has its own unique bit map. The 16 bits in each register consist of an upper (D8 to D15) byte and a lower (D0 to D7) byte, each of which has its own 6-bit address.

SERIAL PERIPHERAL INTERFACE (SPI)

The ADIS16350 serial peripheral interface (SPI) port includes four signals: chip select ($\overline{CS}$), serial clock (SCLK), data input (DIN), and data output (DOUT). The $\overline{CS}$ line enables the ADIS16350 SPI port and frames each SPI event. When this signal is high, the DOUT lines are in a high impedance state and the signals on DIN and SCLK have no impact on operation. A complete data frame contains 16 clock cycles. Because the SPI port operates in full duplex mode, it supports simultaneous, 16-bit receive (DIN) and transmit (DOUT) functions during the same data frame.

Refer to Table 2, Figure 2, and Figure 3 for detailed timing and operation of the SPI port.

Writing to Registers

Figure 6 displays a typical data frame for writing a command to a control register. In this case, the first bit of the DIN sequence is a 1, followed by a 0, the 6-bit address, and the 8-bit data command. Because each write command covers a single byte of data, two data frames are required when writing the entire 16-bit space of a register.

Reading from Registers

Reading the contents of a register requires a modification to the sequence in Figure 6. In this case, the first two bits in the DIN sequence are 0, followed by the address of the register. Each register has two addresses (upper, lower), but either one can be used to access its entire 16 bits of data. The final 8 bits of the DIN sequence are irrelevant and can be counted as "don't cares" during a read command. During the next data frame, the DOUT sequence contains the register's 16-bit data, as shown in Figure 7. Although a single read command requires two separate data frames, the full duplex mode minimizes this overhead, requiring only one extra data frame when continuously sampling.

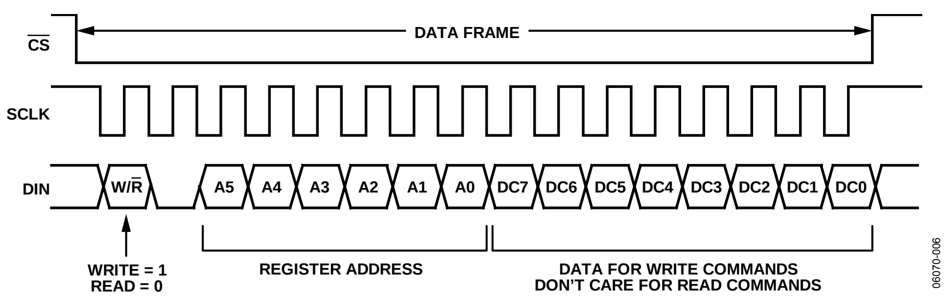

Figure 6. DIN Bit Sequence

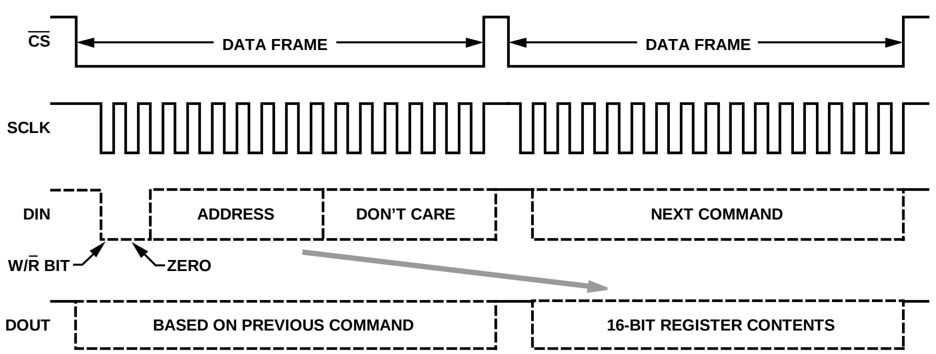

Figure 7. SPI Sequence for Read Commands

DATA OUTPUT REGISTER ACCESS

The ADIS16350 provides access to a full "6 degrees of freedom" (6DOF) set of calibrated motion measurements, power supply measurements, temperature measurements, and an auxiliary 12-bit ADC channel. This output data is continuously updating internally, regardless of user read rates. The following bit map describes the structure of all output data registers in the ADIS16350.

Table 8. Register Bit Map

MSB							LSB
ND	EA	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

The MSB holds the new data (ND) indicator. When the output registers are updated with new data, the ND bit goes to a 1 state. After the output data is read, it returns to a 0 state. The EA bit is used to indicate a system error or an alarm condition that can result from a number of conditions, such as a power supply that is out of the specified operating range. See the Status and Diagnostics section for more details. The output data is either 12 bits or 14 bits in length. For all of the 12-bit output data, the Bit D13 and Bit D12 are assigned "don't care" status.

The output data register map is located in Table 9 and provides all of the necessary details for accessing each register's data. Table 10 displays the output coding for the GYRO_OUT register. Figure 8 provides an example SPI read cycle for this register.

Table 9. Data Output Register Information

Name	Function	Addresses	Data Length (Bits)	Data Format	Scale Factor (per LSB)
SUPPLY_OUT	Power Supply Measurement	0x03, 0x02	12	Binary	1.8315 mV
XGYRO_OUT	X-axis Gyroscope Output Measurement	0x05, 0x04	14	Two's Complement	0.07326 °/sec[1]
YGYRO_OUT	Y-axis Gyroscope Output Measurement	0x07, 0x06	14	Two's Complement	0.07326 °/sec
ZGYRO_OUT	Z-axis Gyroscope Output Measurement	0x09, 0x08	14	Two's Complement	0.07326 °/sec
XACCL_OUT	X-axis Acceleration Output Measurement	0x0B, 0xA	14	Two's Complement	2.522 mg
YACCL_OUT	Y-axis Acceleration Output Measurement	0x0D, 0xC	14	Two's Complement	2.522 mg
ZACCL_OUT	Z-axis Acceleration Output Measurement	0x0F, 0xE	14	Two's Complement	2.522 mg
XTEMP_OUT	X-axis Gyroscope Sensor Temperature Measurement	0x11, 0x10	12	Two's Complement	0.1453 °C
YTEMP_OUT	Y-axis Gyroscope Sensor Temperature Measurement	0x13, 0x12	12	Two's Complement	0.1453 °C
ZTEMP_OUT	Z-axis Gyroscope Sensor Temperature Measurement	0x15, 0x14	12	Two's Complement	0.1453 °C
AUX_ADC	Auxiliary Analog Input Data	0x17, 0x16	12	Binary	0.6105 mV

[1] Assumes that the scaling is set to 320°/sec.

Table 10. Output Coding Example, XGYRO_OUT, YGYRO_OUT, and ZGYRO_OUT[1, 2]

Rate of Rotation					
±320°/sec Range	±160°/sec Range	±80°/sec Range	Binary Output	HEX Output	Decimal
320°/sec	160°/sec	80°/sec	01 0001 0001 0000	0x1110	4368
80°/sec	40°/sec	20°/sec	00 0100 0100 0100	0x0444	1092
40°/sec	20°/sec	10°/sec	00 0010 0010 0010	0x0222	546
0.07326°/sec	0.03663°/sec	0.018315°/sec	00 0000 0000 0001	0x0001	1
0°/sec	0°/sec	0°/sec	00 0000 0000 0000	0x0000	0
−0.07326°/sec	−0.03663°/sec	−0.018315°/sec	11 1111 1111 1111	0x3FFF	−1
−40°/sec	−20°/sec	−10°/sec	11 1101 1101 1110	0x3DDE	−546
−80°/sec	−40°/sec	−20°/sec	11 1011 1011 1100	0x3BBC	−1092
−320°/sec	−160°/sec	−80°/sec	10 1110 1111 0000	0x2EF0	-4368

[1] Two MSBs have been masked off and are not considered in the coding.
[2] Zero offset null performance are assumed.

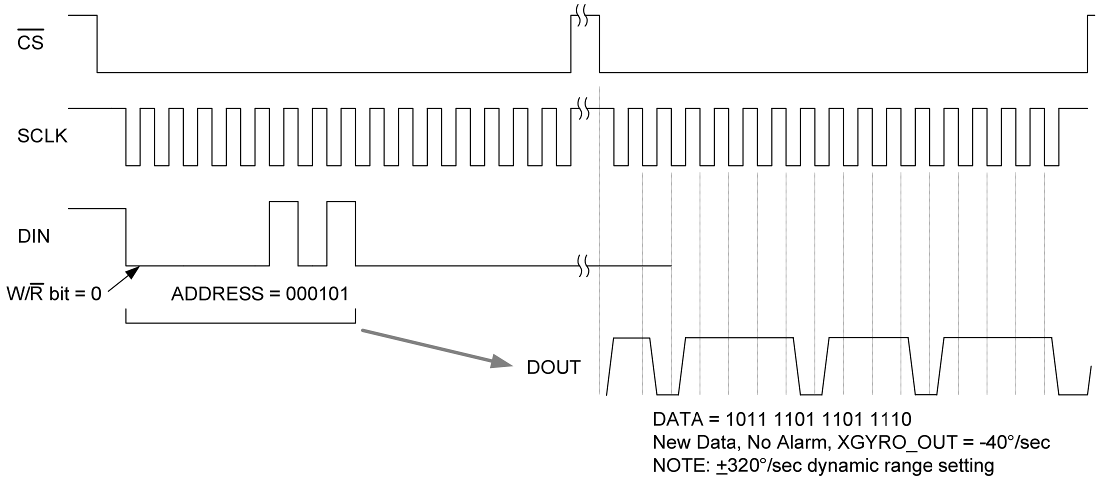

Figure 8. Example Read Cycle

PROGRAMMING AND CONTROL

CONTROL REGISTER OVERVIEW

The ADIS16350 offers many programmable features controlled by writing commands to the appropriate control registers using the SPI. The following sections describe these controls and specify each function and corresponding register configuration. The features available for configuration in this register space are as follows:

- Calibration
- Global commands
- Operational control
  - Sample rate
  - Power management
  - Digital filtering
  - Dynamic range
  - DAC output
  - Digital I/O
- Operational status and diagnostics
  - Self test
  - Status conditions
  - Alarms

CONTROL REGISTER ACCESS

Table 11 displays the control register map for the ADIS16350, including address, volatile status, basic function, and accessibility (read/write). The following sections contain detailed descriptions and configurations for each of these registers.

The ADIS16350 is a flash-based device with the nonvolatile functional registers implemented as flash registers. Take into account the endurance limitation of 20,000 writes when considering the system-level integration of these devices. The nonvolatile column in Table 11 indicates the registers that are recovered on power-up. Use a manual flash update command (using the command register) to store the nonvolatile data registers once they are configured properly. When performing a manual flash update command, make sure that the power supply remains within limits for a minimum of 50 ms after the start of the update. This ensures a successful write of the nonvolatile data.

Table 11. Control Register Mapping

Register Name	Type	Volatility	Address	Bytes	Function	Reference Table
			0x19, 0x018	2	Reserved	
XGYRO_OFF	R/W	Nonvolatile	0x1B, 0x1A	2	X-axis Gyroscope bias offset factor	
YGYRO_OFF	R/W	Nonvolatile	0x1D, 0x1C	2	Y-axis Gyroscope bias offset factor	
ZGYRO_OFF	R/W	Nonvolatile	0x1F, 0x1E	2	Z-axis Gyroscope bias offset factor	
XACCL_OFF	R/W	Nonvolatile	0x21, 0x20	2	X-axis Acceleration bias offset factor	
YACCL_OFF	R/W	Nonvolatile	0x23, 0x22	2	Y-axis Acceleration bias offset factor	
ZACCL_OFF	R/W	Nonvolatile	0x25, 0x24	2	Z-axis Acceleration bias offset factor	
ALM_MAG1	R/W	Nonvolatile	0x27, 0X26	2	Alarm 1 amplitude threshold	
ALM_MAG2	R/W	Nonvolatile	0x29, 0x28	2	Alarm 2 amplitude threshold	
ALM_SMPL1	R/W	Nonvolatile	0x2B, 0x2A	2	Alarm 1 sample period	
ALM_SMPL2	R/W	Nonvolatile	0x2D, 0x2C	2	Alarm 2 sample period	
ALM_CTRL	R/W	Nonvolatile	0x2F, 0x2E	2	Alarm source control register	
AUX_DAC	R/W	Volatile	0x31, 0x30	2	Auxiliary DAC data	
GPIO_CTRL	R/W	Volatile	0x33, 0x32	2	Auxiliary digital I/O control register	
MSC_CTRL	R/W	Nonvolatile[1]	0x35, 0x34	2	Miscellaneous control register	
SMPL_PRD	R/W	Nonvolatile	0x37, 0x36	2	ADC sample period control	
SENS/AVG	R/W	Nonvolatile	0x39, 0x38	2	Defines the dynamic range (sensitivity setting) and the number of taps for the digital filter	
SLP_CNT	R/W	Volatile	0x3B, 0x3A	2	Counter used to determine length of power-down mode	
STATUS	R	Volatile	0x3D, 0x3C	2	System status register	
COMMAND	W	N/A	0x3F, 0x3E	2	System command register	

[1] The contents of the upper byte are nonvolatile; the contents of the lower byte are volatile

CALIBRATION

For applications that require "point of use" calibration, the ADIS16350 provides bias correction registers for all six sensors. Table 12, Table 13, Table 14, and Table 15 provides all of the details required for using these registers to calibrate the ADIS16350's sensors.

Table 12. Gyroscope Bias Correction Registers

Register	Address	Common Parameters
XGYRO_OFF	0x1B, 0x1A	Default Value = 0x0000
YGYRO_OFF	0x1D, 0x1C	Scale = 0.018315°/sec per LSB
ZGYRO_OFF	0x1F, 0x1E	Two's Complement, Read/Write

Table 13. Gyroscope Bias Correction Register Bits

Bit	Description
15:12	Not used
11:0	Data bits

Table 14. Accelerometer Bias Correction Registers

Register	Address	Common Parameters
XACCL_OFF	0x21, 0x20	Default Value = 0x0000
YACCL_OFF	0x23, 0x22	Scale = 2.522 mg per LSB
ZACCL_OFF	0x25, 0x24	Two's Complement, Read/Write

Table 15. Accelerometer Bias Correction Register Bits

Bit	Description
15:12	Not used
11:0	Data bits

Manual Bias Calibration

Since each offset bias register has Read/Write access, the bias of each sensor is adjustable. Write the contents to the appropriate register. For example, in order to adjust for an output drift of 0.18 °/sec, execute the following commands:

- Write 0xF6 to address 0x1A, then 0x0F to address 0x1B

Automatic Bias Null Calibration

The ADIS16350 provides a single-command, automatic bias calibration for all three-gyroscope sensors. The COMMAND register provides this function, which measures all three gyroscope output registers, then loads the three bias correction registers with values that return their outputs to zero (null). A single register write command starts this process:

- Write 0x01 to address 0x3E (See Table 17)

Precision Automatic Bias Null Calibration

The ADIS16350 also provides a single-command function that incorporates the optimal averaging time for generating the appropriate bias correction factor. This command requires approximately 30 seconds. For optimal calibration accuracy, the device should be stable (no motion) for this entire period. In addition, a reset command is required to stop it once it has begun. The following sequence will start this calibration option:

- Write 0x10 to address 0x3E (See Table 17)

Restoring Factory Calibration

The ADIS16350's factory calibration can be restored by returning the contents of each bias correction register to their default value of zero. The following command will accomplish this function for all six sensor signal paths:

- Write 0x02 to address 0x3E (See Table 17)

Linear Acceleration Compensation (Gyroscopes)

The ADIS16350 provides compensation for the gyroscopes' linear acceleration sensitivity. This compensation is controlled by the MSC_CTRL register and can be enabled by the following:

- Write 0x80 to address 0x34 (See Table 29)

Linear Acceleration "Origin" Alignment

The ADIS16350 provide origin alignment for the accelerometers. This compensation is controlled by the MSC_CTRL register and can be enabled by the following:

- Write 0x40 to address 0x34 (See Table 29)

GLOBAL COMMANDS

The ADIS16350 provides global commands for common operations such as calibration, manual FLASH update, auxiliary DAC latch, and software reset. Each of these global commands has a unique control bit assigned to it in the COMMAND register and is initiated by writing a 1 to its assigned bit.

The manual FLASH update writes the contents of each nonvolatile register into FLASH memory for storage. This process takes approximately 50 ms and requires the power supply voltage to be within specification for the duration of the event. It is worth noting that this operation also automatically follows the auto null and factory reset commands.

The DAC latch command loads the contents of AUX_DAC into the DAC latches. Since the AUX_DAC contents must be updated one byte at a time, this command ensures a stable DAC output voltage during updates. Finally, the software reset command sends the ADIS16350 digital processor into a restart sequence, effectively doing the same thing as the $\overline{\text{RST}}$ line.

Table 16. COMMAND Register Definition

Address	Default	Format	Access
0x3F, 0x3E	N/A	N/A	Write only

Table 17. COMMAND Bit Descriptions

Bit	Description
15:8	Not used
7	Software reset command
6:5	Not used
4	Precision Auto null command
3	Manual FLASH update command
2	Auxiliary DAC data latch
1	Factory Calibration Restore command
0	Auto null command

OPERATIONAL CONTROL

Internal Sample Rate

The internal sample rate defines how often data output variables are updated, independent of the rate at which they are read out on the SPI port. The SMPL_PRD register controls the ADIS16350 internal sample rate and has two parts: a selectable time base and a multiplier. The sample period can be calculated using the following equation:

$T_S = T_B \times (N_S + 1)$

Where:

T_S = sample period

T_B = time base

N_S = Multiplier

The default value is the maximum 819.2 samples per second, and the contents of this register are nonvolatile.

Table 18. SMPL_PRD Register Definition

Address	Default	Format	Access
0x37, 0x36	0x0001	N/A	R/W

Table 19. SMPL_PRD Bit Descriptions

Bit	Description
15:8	Not used
7	Time base, 0 = 0.61035 ms, 1 = 18.921 ms
6:0	Multiplier

Here is an example calculation of the sample period for the ADIS16350:

If *SMPL_PRD* = 0x0007, $B7 - B0$ = 00000111

$B7 = 0 \rightarrow T_B = 0.61035$ ms

$B6 \ldots B0 = 000000111 \rightarrow N_S = 7$

$T_S = T_B \times (N_S + 1) = = 0.61035 \text{ ms} \times (7 + 1) = 4.8828\ ms$

$f_S = 1/T_S = 204.8\ SPS$

The sample rate setting has a direct impact on the SPI data rate capability. For SMPL_PRD settings less than, or equal to 0x09 ("FAST MODE"), the SPI SCLK can run at a rate up to 2.5 MHz. For SMPL_PRD settings greater than 0x09 (NORMAL MODE), the SPI SCLK can run at a rate up to 1 MHz.

The sample rate setting also affects the power dissipation. The NORMAL MODE power dissipation is approximately 67% less than the FAST MODE power dissipation. The two different modes of operation offer a system-level trade-off between performance (sample rate, serial transfer rate) and power dissipation.

Power Management

In addition to offering two different performance modes for power optimization, the ADIS16350 offers a programmable shutdown period. Writing the appropriate sleep time to the SLP_CNT register shuts the device down for the specified time. The following example provides an illustration of this relationship:

B7 … B0 = 00000110 = 6 codes => 3 seconds

After completing the sleep period, the ADIS16350 returns to normal operation. If measurements are required before sleep period completion, the ADIS16350 can be awakened by putting the $\overline{CS}$ line in a zero logic state. Otherwise, the $\overline{CS}$ line must be kept high to maintain sleep mode.

Table 20. SLP_CNT Register Definition

Address	Scale[1]	Default	Format	Access
0x3B, 0x3A	0.5sec	0x0000	Binary	R/W

[1] Scale is the weight of each LSB.

Table 21. SLP_CNT Bit Descriptions

Bit	Description
15:8	Not used
7:0	Data bits

Digital Filtering

Each sensor's signal conditioning circuit has an analog bandwidth of approximately 350Hz. The ADIS16350 provides a Bartlett Window FIR filter for additional noise reduction on all of the output data registers. The SENS/AVG register stores the number of taps in this filter in six, "power of two," step sizes (that is, $N=2^M$ = 1, 2, 4, 16, 32, and 64). Filter setup requires one simple step: write the appropriate M factor to the assigned bits in the SENS/AVG register. The bit assignments are listed in Table 23. The following equation offers a frequency response relationship for this filter:

$$H_B(f) = H_A^2(f) \quad \Rightarrow \quad H_A(f) = \frac{\sin(\pi \times N \times f \times t_s)}{N \times \sin(\pi \times f \times t_s)}$$

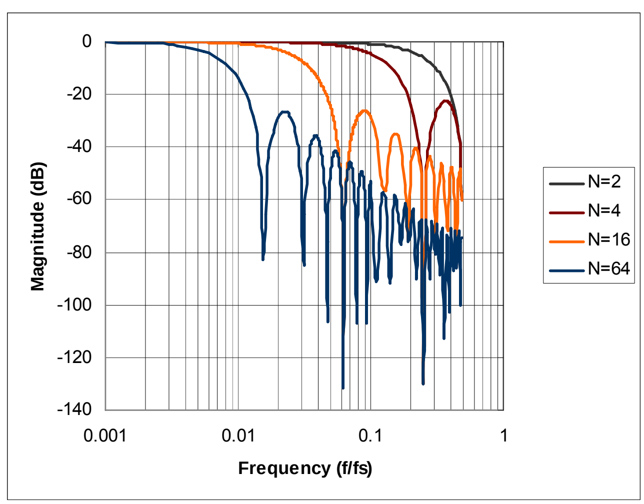

Figure 9. Bartlett Window FIR Frequency Response

Dynamic Range

The ADIS16350 provides three dynamic range settings: ±80°/sec, ±160°/sec, and ±320°/sec. The lower dynamic range settings (80, 160) limit the minimum filter tap sizes in order to maintain the resolution as the measurement range decreases.
The recommended order for programming the SENS/AVG register is (1) upper byte (sensitivity) and then (2) the lower byte (filtering). The contents of the SENS/AVG register are nonvolatile.

Table 22. SENS/AVG Register Definition

Address	Default	Format	Access
0x39, 0x38	0x0402	Binary	R/W

Table 23. SENS/AVG Bit Descriptions

Bit	Value	Description
15:11		Not used
10:8		Sensitivity selection bits
	100	320°/sec (default condition)
	010	160°/sec, filter taps ≥ 4 (Bit 3:0 ≥ 0x02)
	001	80°/sec, filter taps ≥16 (Bit 3:0 ≥ 0x04)
7:3		Not used
2:0		Filter tap setting, M = binary number (number of taps, $N = 2^M$)

Auxiliary DAC

The auxiliary DAC provides a 12-bit level adjustment function. The AUX_DAC register controls the operation of this feature. It offers a rail-to-rail buffered output that has a range of 0 V to 2.5 V. The DAC can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches ground, the linearity begins to degrade (100 LSB beginning point). As the sink current increases, the nonlinear range increases. The DAC output latch function, contained in the COMMAND register, provides continuous operation while writing each byte of this register. The contents of this register are volatile, which means that the desired output level must be set after every reset and power cycle event.

Table 24. AUX_DAC Register Definition

Address	Default	Format	Access
0x31, 0x30	0x0000	Binary	R/W

Table 25. AUX_DAC Bit Descriptions

Bit	Description
15:12	Not used
11:0	Data bits 0x0000 – 0V output, 0x0FFF – 2.5V output

General-Purpose I/O

The ADIS16350 provides two general-purpose pins that enable digital I/O control using the SPI. The GPIO_CTRL control register establishes the configuration of these pins and handles the SPI-to-pin controls. Each pin provides the flexibility of both input (read) and output (write) operations. The contents of this register are volatile. For example, writing a 0x0202 to this register establishes Line 1 as an output and sets its level as a one. Writing 0x0000 to this register establishes both lines as inputs, and their status can be read through Bit 0 and Bit 1 of this register.

The digital I/O lines are also available for data-ready and alarm/error indications. In the event of conflict, the following priority structure governs the digital I/O configuration:

- GPIO_CTRL
- MSC_CTRL
- ALM_CTRL

Table 26. GPIO_CTRL Register Definition

Address	Default	Format	Access
0x33, 0x32	0x0000	N/A	R/W

Table 27. GPIO_CTRL Bit Descriptions

Bit	Description
15:10	Not used
9	General-purpose I/O line 1 polarity 1 = high, 0 = low
8	General-purpose I/O line 0 polarity 1 = high, 0 = low
7:2	Not used
1	General-purpose I/O line 1, data direction control 1 = output, 0 = input
0	General-purpose I/O line 0, data direction control 1 = output, 0 = input

STATUS AND DIAGNOSTICS

The ADIS16350 provides a number of status and diagnostic functions. Table 28 provides a summary of these functions, along with their appropriate control registers.

Table 28. Status and Diagnostic Functions

Function	Register
Data-ready I/O indicator	MSC_CTRL
Self test, mechanical check for MEMS sensor	MSC_CTRL
Status Check for predefined error conditions	STATUS
Flash memory endurance	ENDURANCE
Alarms Configure and check for user-specific conditions	ALM_MAG1/2 ALM_SMPL1/2 ALM_CTRL

Data-Ready I/O Indicator

The data-ready function provides an indication of updated output data. The MSC_CTRL register provides the opportunity to configure either of the general-purpose I/O pins (DIO0 and DIO1) as a data-ready indicator signal.

Table 29. MSC_CTRL Register Definition

Address	Default	Format	Access
0x35, 0x34	0x0000	N/A	R/W

Table 30. MSC_CTRL Bit Descriptions

Bit	Description
15:11	Not used
10	Internal self-test enable: 1 = enabled, 0 = disabled
9	External negative rotation self-test enable 1 = enabled, 0 = disabled
8	External positive rotation self-test enable 1 = enabled, 0 = disabled
7	Linear acceleration compensation for gyroscopes 1 = enabled, 0 = disabled
6	Rotational compensation for accelerometers 1 = enabled, 0 = disabled
5:3	Not used
2	Data-ready enable 1 = enabled, 0 = disabled
1	Data-ready polarity 1 = active high, 0 = active low
0	Data-ready line select 1 = DIO1, 0 = DIO0

Self Test

The MSC_CTRL register also provides a self-test function, which verifies the MEMS sensor's mechanical integrity. There are two different self-test options: (1) internal self-test and (2) external self-test. The internal test provides a simple, two-step process for checking the MEMS sensor: (1) start the process by writing a 1 to Bit 10 in the MSC_CTRL register and (2) check the result by reading Bit 5 of the STATUS register. The entire cycle takes approximately 20ms, during which, the output data is not available. The external self-test is a static condition that can be enabled and disabled. In this test, both positive and negative gyroscope MEMS sensor movements are available. After writing to the appropriate control bit, the GYRO_OUT register reflects the changes after a delay that reflects the sensor signal chain response time. For example, the standard 350 Hz bandwidth reflects an exponential response with a time constant of 0.45 ms. Note that the digital filtering impacts this delay as well. The appropriate bit definitions for self-test are listed in Table 29 and Table 30.

Status Conditions

The STATUS register contains the following error-condition flags: Alarm conditions, self-test status, angular rate over range, SPI communication failure, control register update failure, and power supply out of range. See Table 31 and Table 32 for the appropriate register access and bit assignment for each flag.

The bits assigned for checking power supply range and sensor over range automatically reset to zero when the error condition no longer exists. The remaining error-flag bits in the STATUS register require a read in order to return them to zero. Note that a STATUS register read clears all of the bits to zero.

Table 31. STATUS Register Definition

Address	Default	Format	Access
0x3D, 0x3C	0x0000	N/A	Read only

Table 32. STATUS Bit Descriptions

Bit	Description
15	Z-axis Accelerometer Self Diagnostic Error Flag 1 = failure, 0 = passing
14	Y-axis Accelerometer Self Diagnostic Error Flag 1 = failure, 0 = passing
13	X-axis Accelerometer Self Diagnostic Error Flag 1 = failure, 0 = passing
12	Z-axis Gyroscope Self Diagnostic Error Flag 1 = failure, 0 = passing
11	Y-axis Gyroscope Self Diagnostic Error Flag 1 = failure, 0 = passing
10	X-axis Gyroscope Self Diagnostic Error Flag 1 = failure, 0 = passing
9	Alarm 2 status: 1 = active, 0 = inactive
8	Alarm 1 status 1 = active, 0 = inactive
7:6	Not used
5	Self-test diagnostic error flag 1 = error condition, 0 = normal operation
4	Sensor over range (any of the six) 1 = error condition, 0 = normal operation
3	SPI communications failure 1 = error condition, 0 = normal operation
2	Control register update failed 1 = error condition, 0 = normal operation
1	Power supply in range above 5.25 V 1 = above 5.25 V, 0 = below 5.25V (normal)
0	Power supply below 4.75 V 1 = below 4.75 V, 0 = above 4.75V (normal)

Alarms

The ADIS16350 provides two independent alarm options for event detection. Event detections occur when output register data meets the configured conditions. Configuration options are

- All output data registers are available for monitoring as the source data
- The source data can be filtered or unfiltered
- Comparisons can be static or dynamic (rate of change)
- The threshold levels and times are configurable
- Comparison can be greater than or less than

The ALM_MAG1 register and the ALM_MAG2 register both establish the threshold level for detecting events. They take on the format of the source data and provide a bit for establishing the greater than/less than comparison direction. When making dynamic comparisons, the ALM_SMPL1 register and the ALM_SMPL2 register establish the number of averages taken for the source data as a reference for comparison. In this configuration, each subsequent source data sample is subtracted from the previous one, establishing an instantaneous delta. The ALM_CTRL register controls the source data selection, static/dynamic selection, filtering selection, and digital I/O usage for the alarms.

The rate of change calculation is

N_{DS} = number of samples in ALM_SMPL1/2

$y(n)$ = sampled output data

M_C = magnitude for comparison in ALM_MAG1/2

Y_C = factor to be compared with M_C

$$Y_C = \frac{1}{N_{DS}} \sum_{n=1}^{N_{DS}} y(n+1) - y(n)$$

Rate of change alarm ⇒

Compare Y_C with M_C according to ALM_MAG1/2 MSB (> or < ?)

The contents of ALM_MAG1/2 and ALM_SMPL1/2 are non-volatile.

Table 33. ALM_MAG1 Register Definition

Address	Default	Format	Access
0x27, 0x26	0x0000	N/A	R/W

Table 34. ALM_MAG1 Bit Designations

Bit	Description
15	Comparison polarity: 1 = greater than, 0 = less than
14	Not used
13:0	Data bits: format matches source data format

Table 35. ALM_SMPL1 Register Definition

Address	Default	Format	Access
0x2B, 0x2A	0x0000	Binary	R/W

Table 36. ALM_SMPL1 Bit Designations

Bit	Description
15:8	Not used
7:0	Data bits

Table 37. ALM_MAG2 Register Definition

Address	Default	Format	Access
0x29, 0x28	0x0000	N/A	R/W

Table 38. ALM_MAG2 Bit Designations

Bit	Description
15	Comparison polarity: 1 = greater than, 0 = less than
14	Not used
13:0	Data bits: format matches source data format

Table 39. ALM_SMPL2 Register Definition

Address	Default	Format	Access
0x2D, 0x2C	0x0000	Binary	R/W

Table 40. ALM_SMPL2 Bit Designations

Bit	Description
15:8	Not used
7:0	Data bits

Table 41. ALM_CTRL Register Definition

Address	Default	Format	Access
0x2F, 0x2E	0x0000	N/A	R/W

Table 42. ALM_CTRL Bit Designations

Bit	Value	Description
15:12		Alarm 2 source selection
	0000	Disable
	0001	Power supply output
	0010	X-axis Gyroscope output
	0011	Y-axis Gyroscope output
	0100	Z-axis Gyroscope output
	0101	X-axis Accelerometer output
	0110	Y-axis Accelerometer output
	0111	Z-axis Accelerometer output
	1000	X-axis Gyroscope Temperature Output
	1001	Y-axis Gyroscope Temperature Output
	1010	Z-axis Gyroscope Temperature Output
	1011	Auxiliary ADC Output
11:8		Alarm 1 source selection (same as Alarm 2)
7		Rate of change (ROC) enable for alarm 2 1 = rate of change, 0 = static level
6		Rate of change (ROC) enable for alarm 1 1 = rate of change, 0 = static level
5		Not used
4		Comparison Data Filter Setting 1 = filtered data, 0 = unfiltered data
3		Not used
2		Alarm output enable 1 = enabled, 0 = disabled
1		Alarm output polarity 1 = active high, 0 = active low
0		Alarm output line select 1 = DIO1, 0 = DIO0

OUTLINE DIMENSIONS

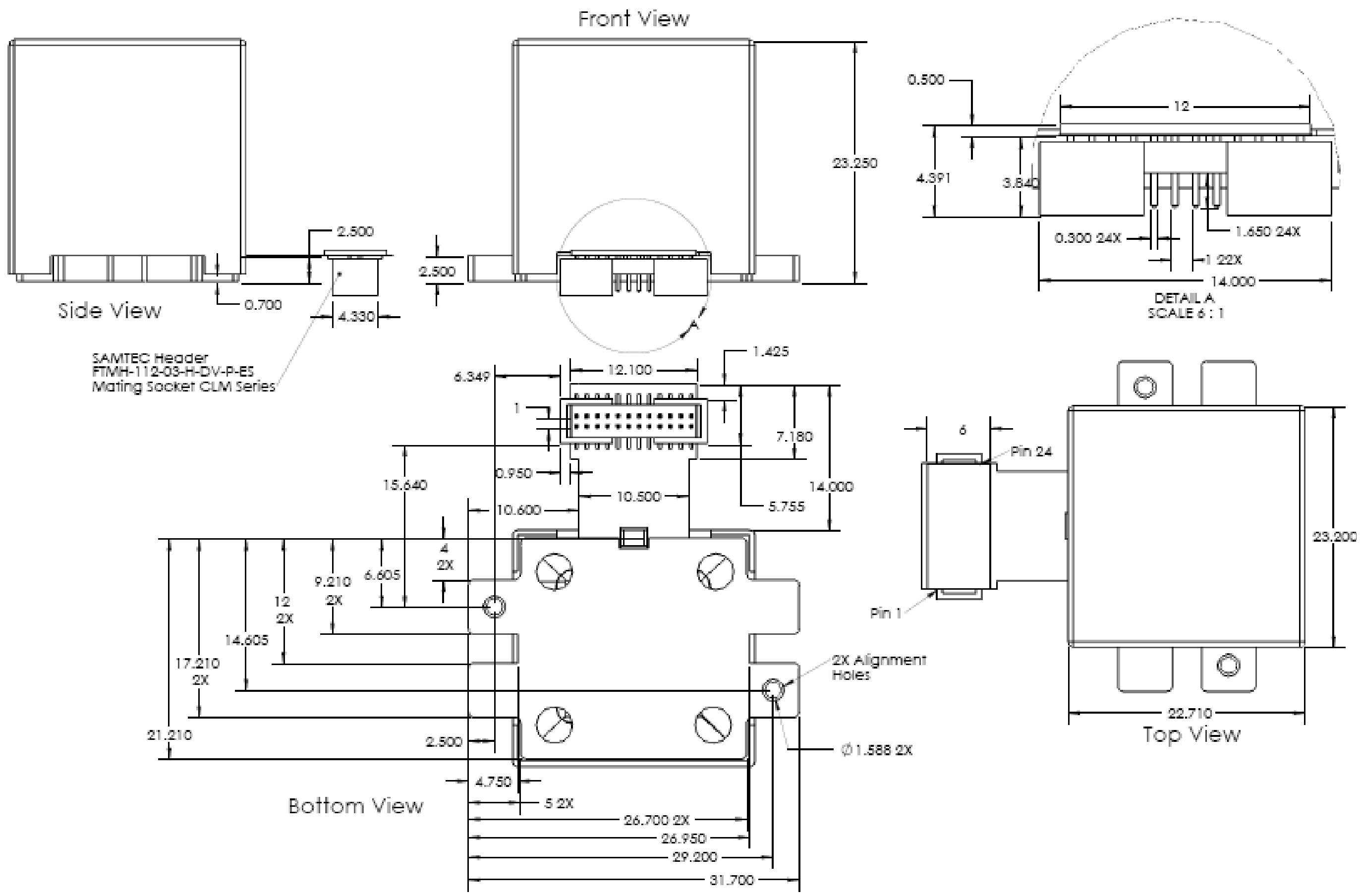

Figure 10.
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADIS16350AML ADIS16350/PCBZ	-40°C to +85°C		

NOTES