

MTD3055VL

N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

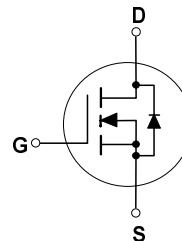
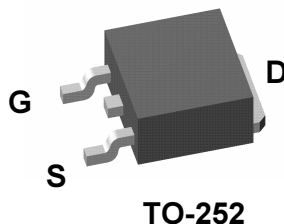
This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- 12 A, 60 V. $R_{DS(ON)} = 0.18 \Omega @ V_{GS} = 5 V$
- Critical DC electrical parameters specified at elevated temperature.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(th)} < 2 V$.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.



Absolute Maximum Ratings $T_c=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DSS}	Drain-Source Voltage	60	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Maximum Drain Current -Continuous (Note 1)	12	A
	$T_C = 100^\circ\text{C}$ (Note 1)	8	
P_D	Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ (Note 1)	48	W
	$T_A = 25^\circ\text{C}$ (Note 1a)	3.9	
	$T_A = 25^\circ\text{C}$ (Note 1b)	1.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to- Case (Note 1)	3.13	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to- Ambient (Note 1a)	71.4	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MTD3055VL	MTD3055VL	13"	16mm	2500

* Die and manufacturing source subject to change without prior notification.

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

DRAIN-SOURCE AVALANCHE RATINGS (Note 2)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25\text{ V}, I_D = 12\text{ A}$			72	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				12	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		54		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			10	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$			100	
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -15\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.5	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-2.6		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 5\text{ V}, I_D = 6\text{ A}$			0.18	Ω
$V_{DS(on)}$	Drain-Source On-Voltage On-Resistance	$V_{GS} = 5\text{ V}, I_D = 12\text{ A}$			2.6	V
		$I_D = 6\text{ A}, T_J = 150^\circ\text{C}$			2.5	
g_{FS}	Forward Transconductance	$V_{DS} = 8\text{ V}, I_D = 6\text{ A}$	5.0			S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$			570	pF
C_{oss}	Output Capacitance				160	pF
C_{riss}	Reverse Transfer Capacitance				40	pF

Switching Characteristics (Note 2)

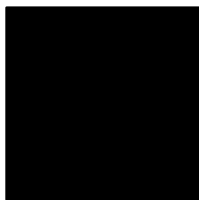
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 12\text{ A}, V_{GS} = 5\text{ V}, R_{GEN} = 9.1\ \Omega$			20	ns
t_r	Turn-On Rise Time				190	ns
$t_{d(off)}$	Turn-Off Delay Time				30	ns
t_f	Turn-Off Fall Time				90	ns
Q_g	Total Gate Charge	$V_{DS} = 48\text{ V}, I_D = 12\text{ A}, V_{GS} = 5\text{ V}$			10	nC
Q_{gs}	Gate-Source Charge			2		nC
Q_{gd}	Gate-Drain Charge			6.1		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current (Note 2)				12	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current (Note 2)				42	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 12\text{ A}$ (Note 2)			1.3	V
t_{rr}	Drain-Source Reverse Recovery Time	$I_F = 12\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		51		nS

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the drain tab. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



■ a) $R_{\theta JA} = 38^\circ\text{C/W}$ when mounted on a 1 in² pad of 2oz copper.

■ b) $R_{\theta JA} = 96^\circ\text{C/W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE _x [™]	FAST _r [™]	OPTOLOGIC [®]	SMART START [™]	VCX [™]
Bottomless [™]	FRFET [™]	OPTOPLANAR [™]	SPM [™]	
CoolFET [™]	GlobalOptoisolator [™]	PACMAN [™]	Stealth [™]	
CROSSVOLT [™]	GTO [™]	POP [™]	SuperSOT [™] -3	
DOME [™]	HiSeC [™]	Power247 [™]	SuperSOT [™] -6	
EcoSPARK [™]	I ² C [™]	PowerTrench [®]	SuperSOT [™] -8	
E ² CMOS [™]	ISOPLANAR [™]	QFET [™]	SyncFET [™]	
EnSigna [™]	LittleFET [™]	QST [™]	TinyLogic [™]	
FACT [™]	MicroFET [™]	QT Optoelectronics [™]	TruTranslation [™]	
FACT Quiet Series [™]	MicroPak [™]	Quiet Series [™]	UHC [™]	
FAST [®]	MICROWIRE [™]	SILENT SWITCHER [®]	UltraFET [®]	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.