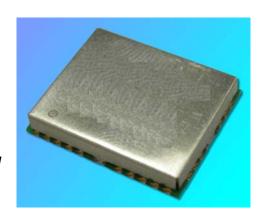


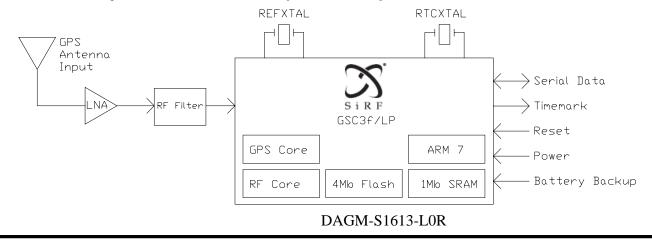
## DAGM-S1613-L0R GPS/AGPS Module

- Multi-ca<sub>I</sub>rier,Multi-standard Cellular handsets.
- W-CDMA,GSM/EDGE,UMTS,PDC CDMA,etc.
- Telematics, Navigation/Security and Gaming/Tracking.



### **FEATURES**

- Supports GPS L1band C/A code
- The GSC3f is SiRF starlll receiver in a single package, The baseband, RF, and Flash are integrated into the 7X10mm.
- High indoor sensitivity of -158dBm achieved utilizing 200,000 effective correlators(both acquisition & tracking)
- Works in both Autonomous mode and Assisted-GPS(MS-Based and MS-assisted) mode
- Fast TTFF of typically 5s when hot and <55s from cold
- Accuracy of 5m outdoors (CEP 95%) and <10m indoors



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# **Specification**

General	GPS L1-band C/A code
Sensitivity	-158dBm(Tracking)
Interface	UART(TX/RX)
Baud rate	9600 bps (Sample)
Protocols	a. SiRF Binary message b. NMEA message
Update Rate	Once per second
Accuracy	5m outdoors (CEP 95%)
Acquisition	Hot start: 3s (typical)
	Cold start: <50s
	Warm start: 5-38s
Operating Voltage	3.0 ~5.0 V
Operating Temperature	-30 ~ +85 °C
Package Size	15.9(L)*13.1(W)*2.0(H) mm



# **Electrical requirements**

### **DC Operating Characteristics for RTC Block (Backup Voltage Ratings)**

Item	Symbol	Min.	Тур.	Max	Units
RTC Supply	D1.5VCC	2.0	3.0	5.0	V
Supply Current	IDDRTC		10		μΑ

### **Absolute Maximum Ratings**

Item	Symbol	Min	Max	Unit
Power Dissipation (Ta=+80C)	PD		400	mW
Supply Voltage, RTC	VDD_RTC	-0.3	2.0	V
Supply Voltage, SRAM	VDD_RTC	-0.3	2.0	V
High Level Input Voltage, GPIO and data bus	VIH	0.7*VDD	0.3+VDD	V
Low Level Input voltage, GPIO and data bus	VIL	-0.3	0.3*VDD	V

#### **Recommended Operating Conditions**

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Item	Symbol	Min	TYP	Max	Unit	
Temperature	TA	-30		+85	С	
GPS module main Input voltage	VDD	3.1	3.3	5.0	V	
Backup power	D1.5VCC	2.0	3.0	5.0	V	
RTC Power	D1.5VCC	2.0	3.0	5.0	V	
GPIO supply voltage	IOVDD	3.1	3.3	5.0	V	

### **Power consumption**

Item		TYP	Unit
Operating	Navigation	116	mW
Tracking		86	mW
Hibernate		30	uW

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#### Inputs

All Power inputs have EMI filtering (10nF, 12pF) on the external circuit. All Power inputs have the external protection circuit and EMI filtering capacitor.

#### B/S(Boot select)

This pin is for program download.

This pin should be high when the program is downloaded.

If the B/S is high then the module will boot from the serial port. and

If the B/S is low then the module will begin execution from the on-board FLASH.

#### Reset

On module power up, this signal should remain low until power stable.

This input is low active. This module has need external reset circuit that has Min 300 msec reset time.

#### **ECLK (External Clock)**

The ECLK input is also the input pin for clock correction in AGPS. The frequency stability of this signal should be better than +/- 0.1ppm for best results and free of any externally controlled "steering" during the time of measurement.

#### **TimerSync**

This pin is used for time transfer information into the GPS receiver with AGPS code ONLY, and also for alternate applications. When use as a TIMERSYNC input, this input pulse is rising edge triggered, and must be 100ns wide as a minimum, and 1ms wide as an approximate maximum.

#### Wake Up

Edge triggered (Rising Edge) soft or Hard on/off request. Active High. Should only be used to wake up chip. You must set low in normal operating

#### **Outputs**

GPIO should have EMI filtering capacitors (10nF, 18pF/50V) in external circuit for protecting *RF* radiation and keeping DAGM-S1613-L0R isolated from other devices.

#### **RF Connections**

DAGM-S1613-L0R port 1 is connected to the GPS antenna input.

\* The active antenna input should have the proper impedance matching.

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## **GPS Antenna Specification (Recommended)**

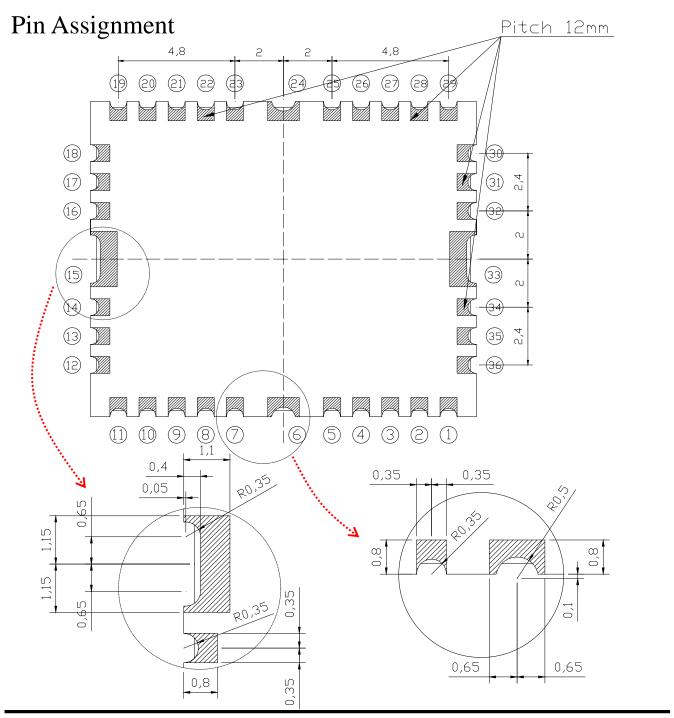
It is important that the antenna gets a clear view of the sky and is positioned on a surface level to the horizon for best results. The following specification has to meet for the use with DAGM-S1613-L0R reference design.

Characteristic	Specification
Polarization	Right-hand circular polarized
Receive frequency	1.57542GHz+/-1.023 MHz
Power supply	3V
DC current	< 8mA @ 3V
Total gain	Max +15dBi
Output VSWR	< 2.5

Typical active antenna characteristics

<sup>\*</sup> Line width should be designed to match  $50\Omega$  characteristic impedance, depending on PCB material and thickness.





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Pin no	Name	Description
1	ANT	GPS RF input, 1575.42MHz, 50ohm,3V active antenna Bias output with LNA (Module without LNA)
2	AGND	Analog system ground
3	AGND	Analog system ground
4	AGND	Analog system ground
5	D1.5Vcc	BBSRAM Power, Min 2.0V
6	GND	Analog system ground (Chassis GND)
7	B/S	This pin is for program download. This pin should be High when the program is downloaded. If the B/S is High then the module will boot from the serial port. and If the B/S is Low then the module will begin execution from the on-board FLASH. Please set Low during operating Mode
8	AGND	Analog system ground
9	AGND	Analog system ground
10	AGND	Analog system ground
11	VDD	Main Power input(3.0V) to on-board regulator
12	AGND	Analog system ground
13	RESET	On module power up this signal should remain low until power stable. This input is low active. The module has need external power on reset circuit.
14	AGND	Analog system ground
15	AGND	Analog system ground
16	ECLK	External Clock For Correcting Clock (10MHz ~ 50MHz)(Only Asist)
17	AGND	Analog system ground
18	AGND	Analog system ground

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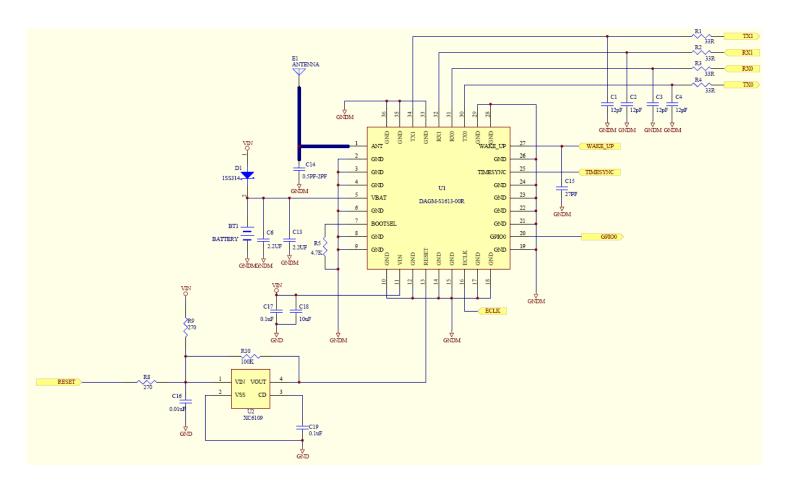


Pin no	Name	Description
19	AGND	Analog system ground
20	GPIO0	GIPO0 output use LNA Control Enable
21	AGND	Analog system ground
22	AGND	Analog system ground
23	AGND	Analog system ground
24	AGND	Analog system ground
25	TIMESYNC	Time Synchronous Signal For Correcting Time(Only Asist)
26	AGND	Analog system ground
27	WAKE_UP	External wake-up input Pull low via 4.7k to 10kohm. (Only APM)
28	AGND	Analog system ground
29	AGND	Analog system ground
30	TX0	Serial UART interface to BB processor, module input,3V_I/O
31	RX0	Serial UART interface to BB processor, module output,3V_I/O
32	RX1	Auxiliary Serial UART interface,unused
33	AGND	Analog system ground
34	TX1	Serial UART interface ,unused
35	AGND	Analog system ground
36	AGND	Analog system ground



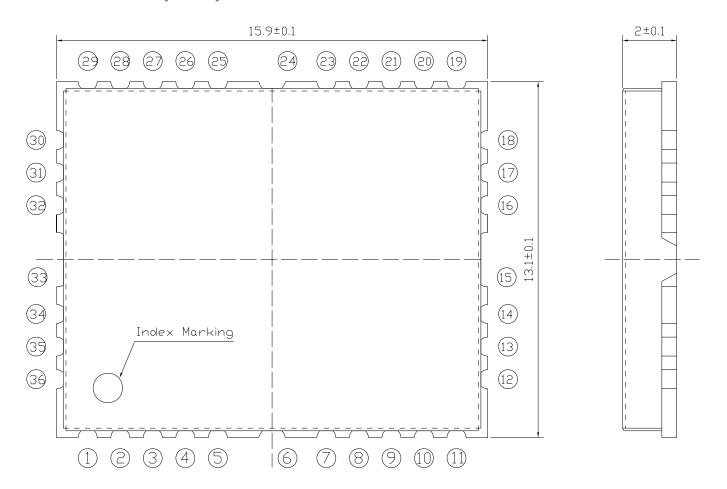
# Reference design

### **Application Circuit of UART Interface**





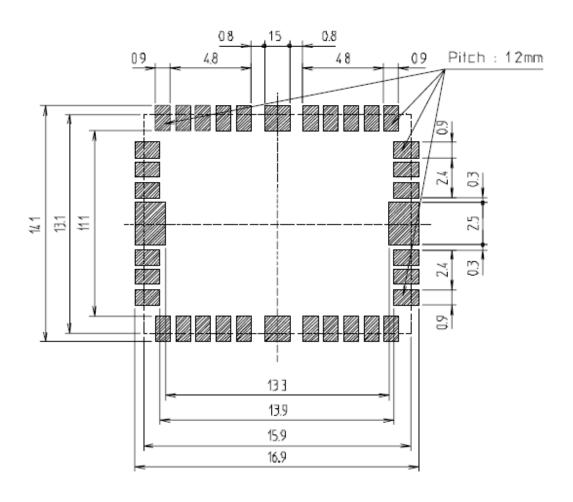
# **Dimension(mm)**



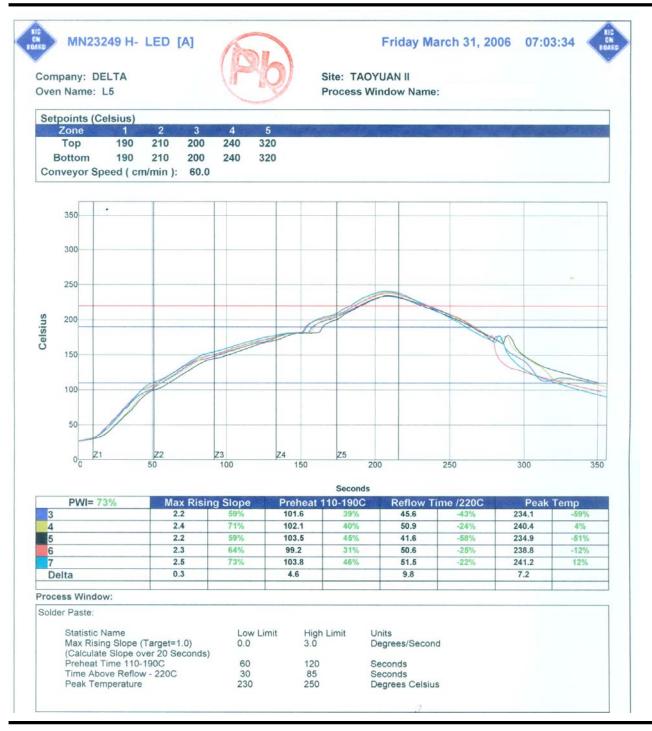
**TOP View** 



# **Appendix EVM Module Mounting Details**







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## **Record of changes**

Date	Content of change	Maker
May 15, 2006	DAGM-S1613-L0R Data-Sheet (1) FEATURES (2) Specification (3) Pin Assignment (4) Dimension(mm)	Ming Cheng
Sep 25,2006	(1) DAGM-S1613-L0R Sample Baudrate:9600	Ming Cheng
Jan 5, 2007	(1) Revise Power consumption	Ming Cheng
	(1)	
	(1)	

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