CATAT71991

2.0A 380KHz 23V High Efficiency Step-Down DC/DC Converter

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General Description

The CAT71991 is a high efficiency and up to 2A output current step-down DC/DC converter series that integrates a low on resistance NMOS on high side. Including on the substrate with the listed features is a high performance trans-conductance error amplifier that provides tight voltage regulation and accuracy under transient conditions. An under voltage lockout circuit is built in to prevent start up until the input voltage reaches to 4.75V. Other features include an over current protection and thermal shutdown. The CAT71991 is available in an 8 pins SOIC package.

Application

- Set-Top-Box, DVD, LCD Displays
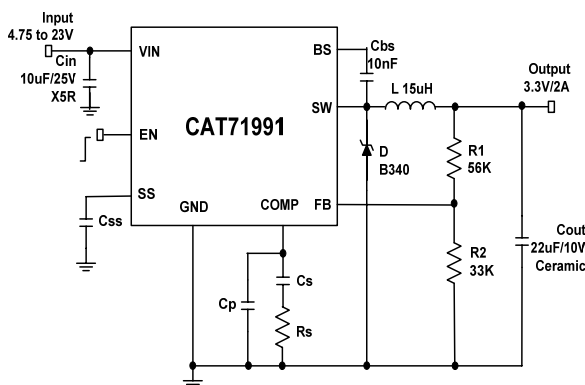- High Power LED Power Supply
- Distributed Power System
- Data comm. xDSL CPE
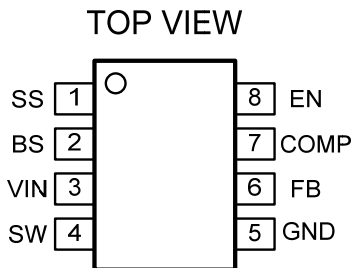
Features

- High Efficiency up to 92%
- 4.75V to 23V Wide Input Voltage Range
- Output Adjustable from 1.23 to 17V
- 2.0A Output Current
- 380kHz constant Frequency Operation
- Current Mode Control
- Over-temperature Protection
- Over Current Protection
- Under Voltage Lockout
- 25µA Shutdown Current
- CAT71991 with Soft Star Function
- SOP8 Package
- RoHS Compliant (100% Green available)

Ordering Information

Part Number	Package	Ship
CAT71991CA	SOP8	2500/ Tape & Reel

Pin Configuration

TOP VIEW

SS	1		8	EN
BS	2		7	COMP
VIN	3		6	FB
SW	4		5	GND

Efficiency Table

Efficiency VS Output Current at V_{IN}=12V

Typical Application
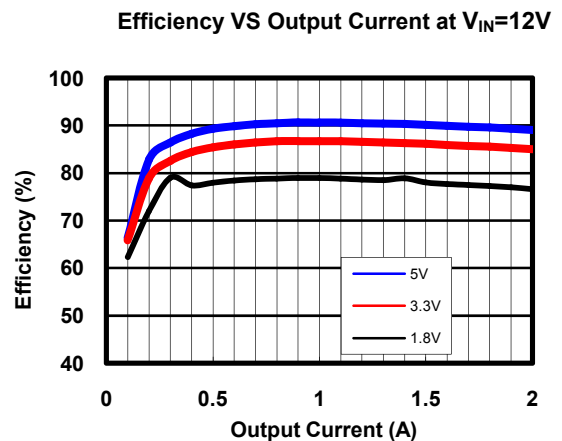
Pin Description

Pin	Symbol	Description
1	SS	Connect SS to an external capacitor to control soft-start timing. If SS is open, internal soft-start about 160uS will be used.
2	BS	High Side Gate Drive Boost Input. A capacitor must be connected from SW to BS. This capacitor boosts the gate drive to the internal NMOS above VIN to fully turn it ON.
3	VIN	Power Supply Pin. The input voltage for the power supply is connected to Pin3.
4	SW	Power Switch Output. This is the output of a power MOSFET switch connected directly to the input voltage.
5	GND	Ground Pin. This is the ground reference connection for all components in the power supply.
6	FB	Voltage Feedback Pin. This is the input to an error amplifier, which drives the PWM controller. It's necessary to connect this pin to the actual output of power supply to set the DC output voltage.
7	COMP	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a series RC network from COMP pin to GND pin to compensate the regulation control loop.
8	EN	Enable Pin. This input provides an electrical ON/OFF control of the power Supply.

Function Block Diagram

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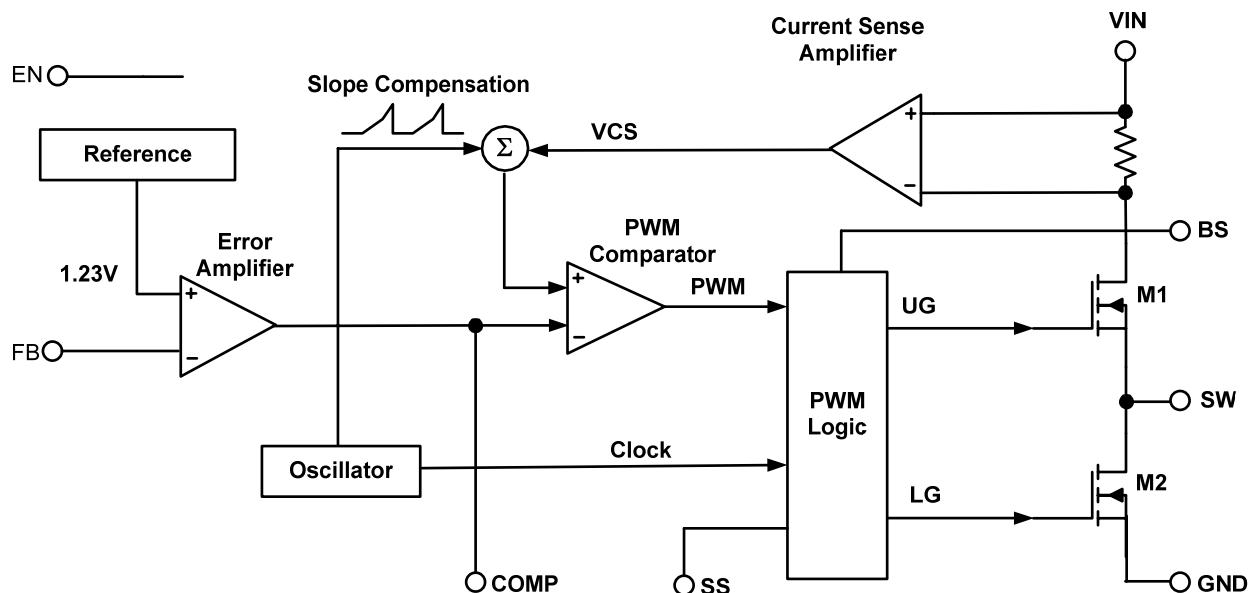
Absolute Maximum Ratings

Input Supply Voltage…………..GND - 0.3V to +25V

SW Voltage…………………………..- 1 to VIN+0.3V

EN Voltage……………………………- 1 to VIN+0.3V

Other Pins………………………………- 0.3V to +6V

Boost Voltage ………..………………Vsw+6V

(<30V)

SW Peak Current…………………………………..5.5 A

ESD Classification…………………………..Class 2

Junction Temperature Range…………………..150°C

Storage Temperature Range…………-65°C to 150°C

Lead Temperature (Soldering 10s)……………..260°C

Recommended Operating Conditions

Supply Voltage (VIN)……………………4.75V to 23V

Operating Temperature……………..–40°C to +85°C

Thermal Resistance: θ_{JA} θ_{JC}

SOIC Package………………..…..91   43 (°C/W)

*Note: The IC has a protection circuit against static electricity. Do not apply high static electricity or high voltage that exceeds the performance of the protection circuit to the IC.

Electrical Characteristic

(Recommended Operating Conditions, Unless Otherwise Noted; VIN = 12V; TA = 25 °C)

| Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage		4.75		23	V
Shutdown Supply Current	VEN = 0V				µA
Regulated Feedback Voltage	4.75V≦VIN≦23V	1.19	1.23	1.26	V
Error Amplifier Transconductance	△ICOMP = ±10µA		830		µA/V
Current sense to COMP Transconductance			2.2		A/V
Current Limit			4		A
SW Leakage Current	VEN = 0V, VSW = 0V				µA
High Side On Resistance			0.25		Ω
Low Side On Resistance	I		10		Ω
Oscillation frequency			380		KHz
Short Circuit Oscillation Frequency	VFB=0V		190		KHz
Maximum Duty Cycle	VFB=1.0V		90		%
Minimum Duty Cycle	VFB=1.5V			0	%
Under Voltage Lockout Threshold	VIN Rising	3.9	4.1	4.3	V
Under Voltage Lockout Threshold Hysteresis			200		mV
Thermal Shutdown Threshold			160		℃
EN High Level		2.6			V
EN Low Level				0.9	V
EN Input Current	VEN = 0V	1.1	1.8	2.5	µA
Soft Start	Pin is opened		160		us

Typical Performance Characteristics

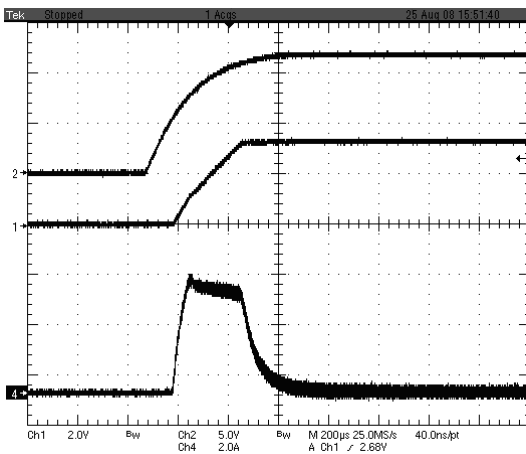Cin=10u F , Cout = 470u F , L=15Uh , T_A=25 ℃ , unless otherwise noted.

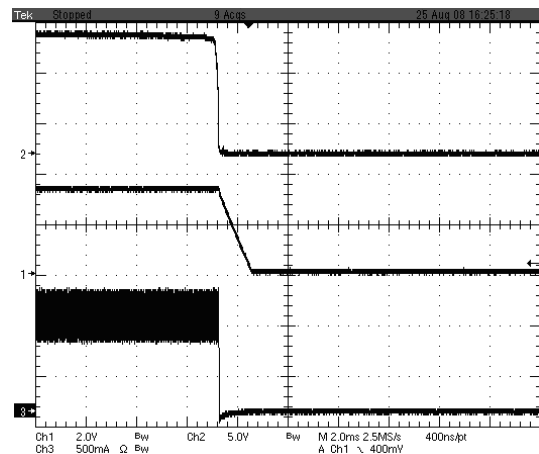### Frequency vs. Input Voltage
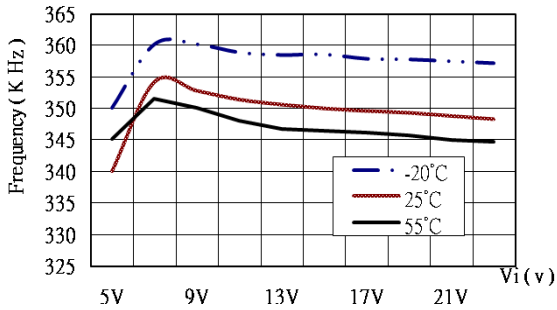
I_load vs. Vo Voltage
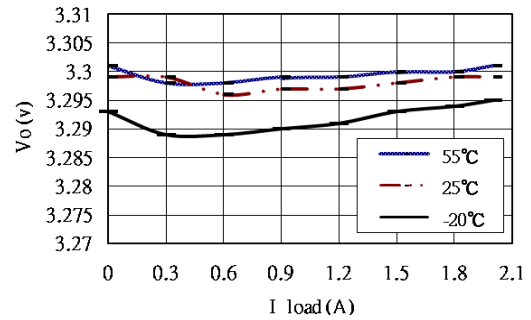
Power on From EN

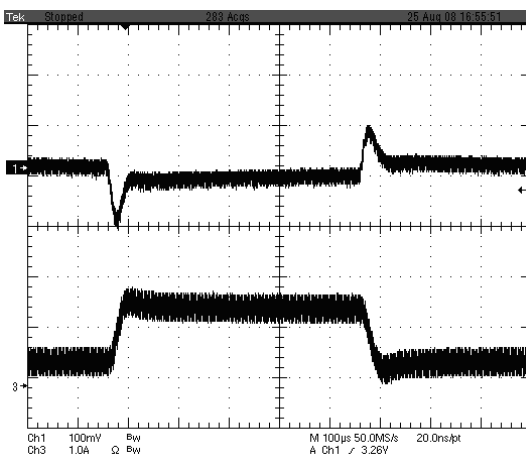

CH1: VO   CH2: EN   CH3: I_L

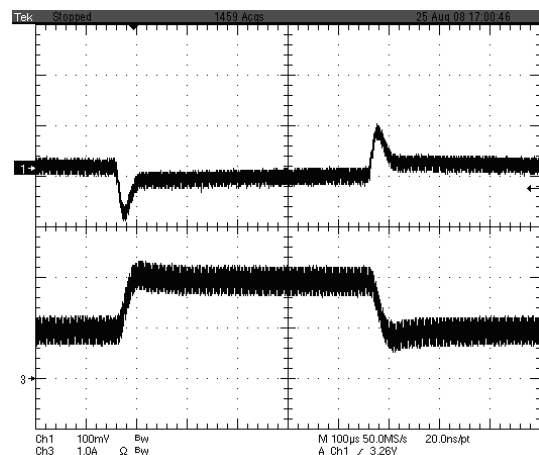### Power off From EN

CH1: VO   CH2: EN   CH3: I_L

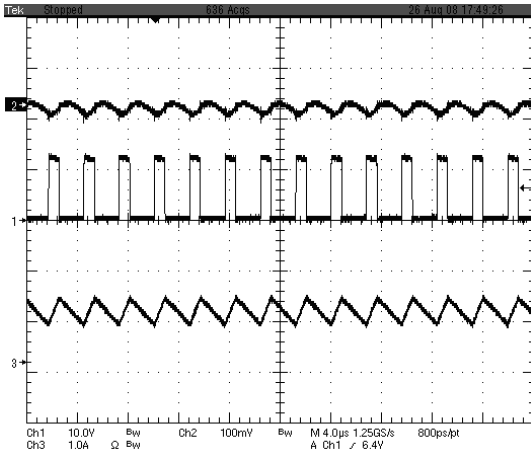### Load Transient   Response

CH1: VO   CH3: I_L   (IL=0.5~1.5A)

Load Transient Response

CH1: VO   CH3: I_L   (IL=1~2A)

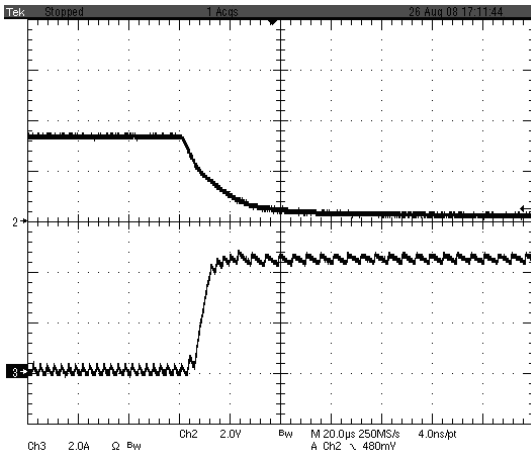## Load Transient   Response

CH1: SW   CH2:VO   CH3: I_L

Load Transient   Response

V_{IN}=12V , VO=3.3V ,   I_L= 2A
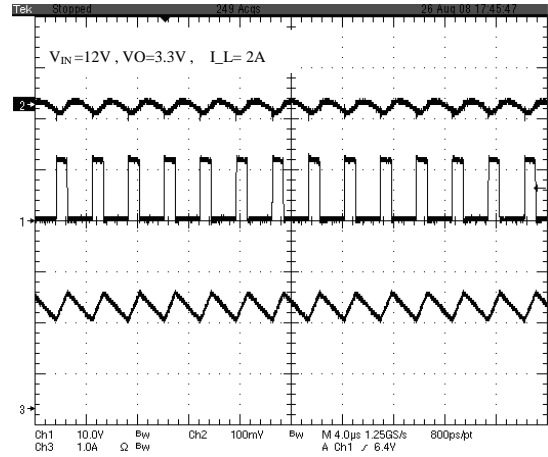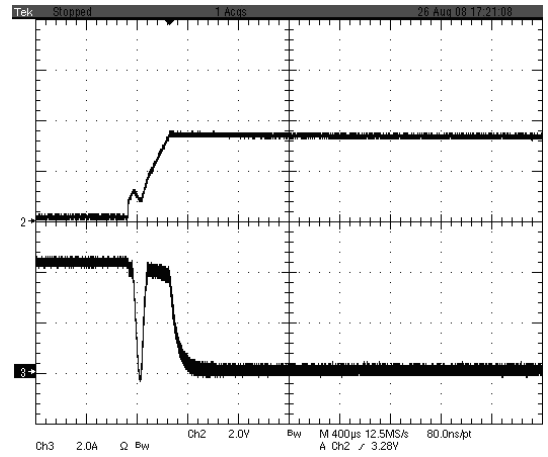
CH1: SW   CH2:VO   CH3: I_L

Short   Protection

CH2 : VO   CH3: I_L

Short   Protection

CH2: VO   CH3: I_L

Function Description

The CAT71991 is a fixed switching frequency current mode PWM step-down converter. It regulates input voltages from 4.75V to 23V down to an output voltage as low as 1.23V, and is able to supply up to 2A of load current.

Oscillator Frequency

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for superior load and line response. It also provides protection of the internal main switch and synchronous rectifier. The CAT71991 switches at a fixed frequency (380 KHz) and regulates the output voltage. During each cycle the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the low side MOS will be turned on immediately and stay on until either the next cycle starts.

Short Circuit Protection

The CAT71991 has short circuit protection. When the output is shorted to ground, the oscillator frequency is reduced to prevent the inductor current from increasing beyond the NMOS current limit. The NMOS current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches 1.23V.

Maximum Load current

The CAT71991 can operate down to 4.75V input voltage; however the maximum load current decreases at lower input due to large I*R voltage drop on the main switch and low side switch. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%.

Enable

The EN pin provides electrical on/off control of the regulator. Once the EN pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the EN pin voltage is pulled below the threshold, the regulator stops switching and the internal slow start resets. Connecting the pin to ground or to any voltage less than 0.9V will disable the regulator and activate the shutdown mode.

Under Voltage Lockout

The CAT71991 incorporates an under voltage lockout circuit to keep the device disable when VIN is below the UVLO start threshold. During power up, internal circuit are held inactive until VIN exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, device start-up begins. The device operates until VIN fall below the UVLO stop threshold voltage. The typical hysteretic in the UVLO comparator is 200mV.

Soft Start

CAT71991 built in the soft start function to reduce input inrush current while turn on. If let this pin open it will provide about 160us timing such that the duty from small to specific duty during turn on period. Thus this function can lower the current stress on input power, MOSFET, and freewheeling diode. Connect a capacitor on this pin to program the soft start time. It is defined as

tss=τ*Css ----- To be defined from RD.

Boost Capacitor

Connect a 10nF low ESR ceramic capacitor between the BS pin and SW pin. This capacitor provides the gate drive voltage for the high side MOSFET.

Thermal Shutdown

The CAT71991 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown threshold, the voltage reference is grounded and high side MOSFET is turned off.

Compensation

The system stability is controlled through COMP pin. It will present a general design procedure to help insure a stable and operational circuit. The design in this data sheet is optimized for particular requirements. If different conversions are requires, some of the components may need to be changed

to ensure stability. The power components and their effects will be determined first, and then the compensation components will be chosen to produce stability.

The converters compensation steps are listed below:

(1). Choose reasonable inductor and output capacitance according to the allowed output voltage ripple and load transient.

(2). Place F_C sufficiently below F_S. Typically, F_C is approximately below 1/4 ~ 1/10 of F_S.

(3). Set the compensation R_C to zero to cancel the $R_{LOAD} C_{OUT}$ pole.

$$R_C = \frac{2\pi \times F_C \times C_{OUT} \times V_{OUT}}{G_M \times G_{CS} \times V_{REF}}$$

$$C_C = \frac{C_{OUT} \times R_{LOAD}}{R_C}$$

G_M: error amp transconductance

G_{CS}: current sense transconductance

(4). Determine C_P if is required.

If Z_{ESR} (zero occurs by output capacitor ESR) is less than F_C, it should be cancelled with a pole set by capacitor C_P connected from C_C to GND.

$$C_P = C_{OUT} \times \frac{R_{ESR}}{R_C}$$

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$I_{IN} RMS = I_{OUT} \sqrt{D \times (1-D)}$$

where D is the duty cycle, I_{inRMS} is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. Losses in the input capacitors can be calculated with the following equation:

$$P_{CIN} = ESR_{CIN} \times I_{IN} RMS^2$$

where P_{CIN} is the power loss in the input capacitors and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and affects the load transient response. Higher inductance reduces the inductor's ripple current and induces lower output ripple voltage. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{in} - V_{out}}{F_S \times L} \bullet \frac{V_{out}}{Vin}$$

$$\Delta V_{out} = \Delta I \times ESR$$

Although increase the inductance reduce the ripple current and voltage, but the large inductance reduces the regulator's response time to load transient. Increasing the switching frequency (Fs) for a given inductor also reduces the ripple current and voltage but it will increase the switching loss of the power MOS.

To select the inductor value, a guideline is to choose the ripple current ($\triangle$I) to be approximately 10%~50% of the maximum output current. Once the inductor value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. It is also important to have the inductance tolerance specified to keep the accuracy of the system controlled. Using 20% for the inductance (at room temperature) are reasonable tolerances that most manufacturers can meet. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitors Selection

An output capacitor is required to filter the output and supply the load transient current. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. These requirements are met with a mix of capacitors and careful layout.

In typical switching regulator design, the ESR of the output capacitor bank dominates the transient response. The number of output capacitors can be determined by using the following equations:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

$$Number \quad Of \quad Capacitors = \frac{ESR_{CAP}}{ESR_{MAX}}$$

$\triangle V_{ESR}$ = change in output voltage due to ESR

(Assigned by the designer).

$\triangle IOUT$ = load transient.

ESR_{CAP} = maximum ESR per capacitor (specified

in manufacturer's data sheet).

ESR_{MAX} = maximum allowable ESR.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Consult the capacitors manufacturer to make sure the decoupling requirements.

Output Voltage

The output voltage is set using the FB pin and a resistor divider connected to the output as shown in next page AP Circuit. The FB pin voltage is 1.23V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$V_{FB} = V_{out} \times \frac{R_2}{(R_1 + R_2)}$$

Thus the output voltage is:

$$V_{out} = 1.23 \times \frac{(R_1 + R_2)}{R_2}$$

External Bootstrap Diode

It is recommended that an external bootstrap diode be added when the system has a 5V fixed input (Strongly recommend to add) or the power supply generates a 5V output. This helps improve the efficiency of the CAT71991 regulator. The boost diode can be a low cost one such as IN4148 or BAT54.
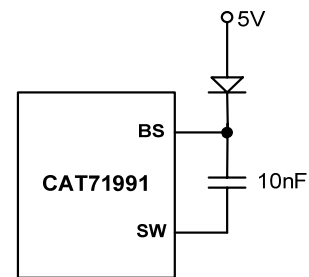
This diode is also recommended for high duty cycle operation when Duty Cycle>65% (Example: VIN=5V & Vout=3.3V; Duty Cycle=66%) and high output voltage (VOUT>12V) applications.

Layout Consideration

For proper operation of the converter, some layout rules should be followed. One should know the CAT71991 which pin is sensitive and insensitive. And to see where will produce noise on circuit and where is the clear ground for the small signal ground to refer.
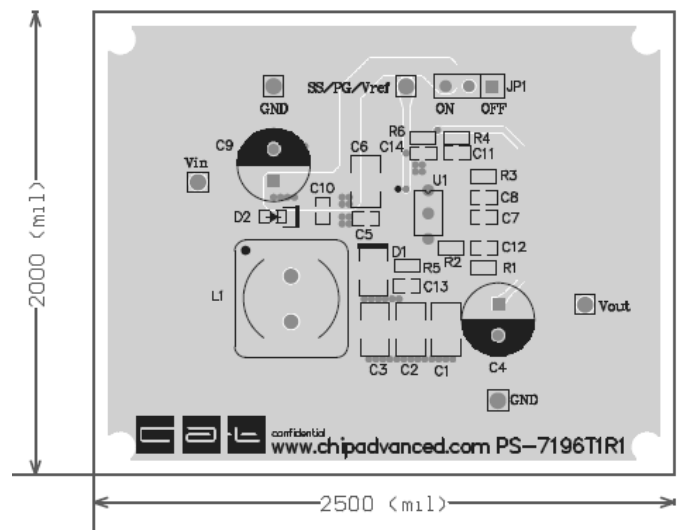

Top Layer:

Bottom Layer: (Top view)
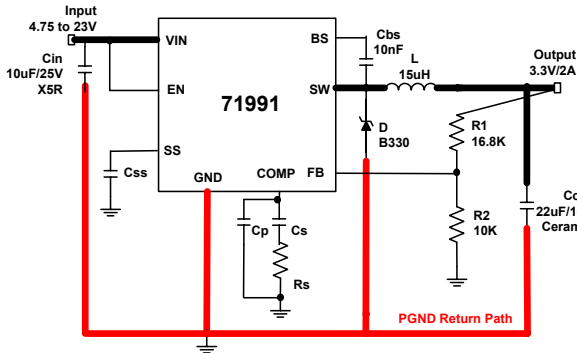
1.) Put the input capacitor (C_{IN}) as close as possible to the VIN pin firstly.

2.) Secondarily place the Cs, Rs, Cp, Css and R2 as close as CAT71991 and connect these analog grounds (Clear AGND) to CAT71991's GND pin. These AGND pins recommend used a dot short or via contact to connect CAT71991' GND pin.

3.) The large current loop as showed in bold lines in above figure circuit should be routed as short and wide as possible. And the switch node is a high dv/dt. It easily couples noise to other trace by capacitive path. Therefore the sensitive signals like FB, COMP and AGND should be routed away with this noise source.

4.) The feedback network resistors (R1 & R2) should be routed away from the inductor and switch node to minimize noise and EMI issue. And the R1 resistor should be sensed the output capacitor or device loading, not the inductor's output node.
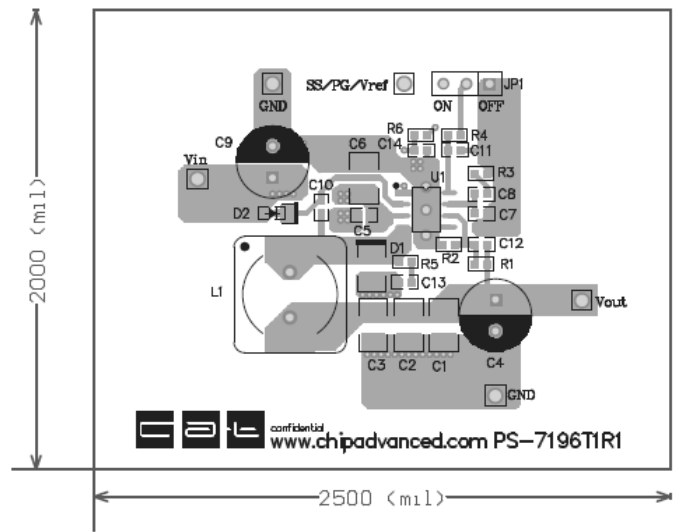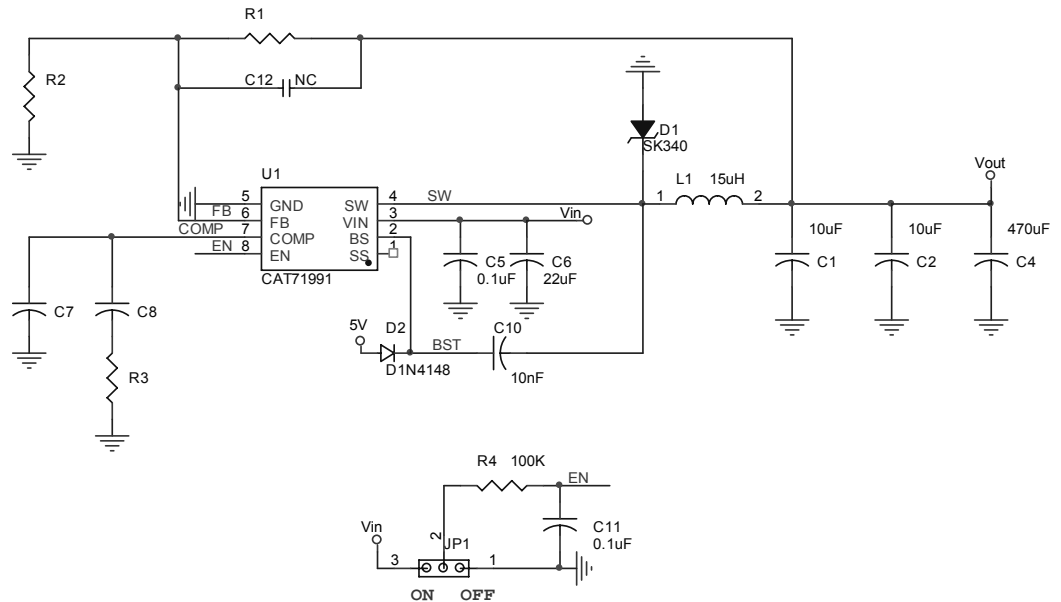
Application & BOM List Table:

Vout	C12	C7	C8	R3	L1	R1	R2
5V	NC	33pF	2.2nF	4.7k	15uH	68k	22k
3.3V	NC	33pF	2.2nF	5.6k	15uH	56k	33k
1.8V	NC	33pF	2.2nF	5.6k	15uH	4.7k	10k
1.23V	NC	33pF	2.2nF	3k	15uH	4.7k	NC

CAT71991 AP Circuit

$Vout=1.23V*(1+R1/R2)$

Package Dimensions

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (MM).
2. DIMENSION D1&E1 DOES NOT INCLUDE MOLD PROTRUSION.
3. COPLANARITY OF ALL LEADS SHALL BE (BEFORE TEST) 0.089 MAX. FROM THE SEATING PLANE. UNLESS OTHERWISE SPECIFIED.

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Classification Reflow Profiles

Reflow Profile	Green Assembly
Average Ramp-Up Rate (Ts$_{max}$ to Tp)	3℃/second max.
Preheat -Temperature Min(Ts$_{min}$) -Temperature Max(Ts$_{max}$) -Time(ts$_{min}$ to ts ts$_{max}$)	150℃ 200℃ 60-180 seconds
Time maintained above: -Temperature(T$_L$) -Time(t$_L$)	217℃ 60-150 seconds
Peak Temperature(Tp)	260 +0/-5 ℃
Time within 5 ℃ of actual Peak Temperature(tp)	20-40 seconds
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

Note: All Temperatures refer to topside of the package, measured on the package body surface.
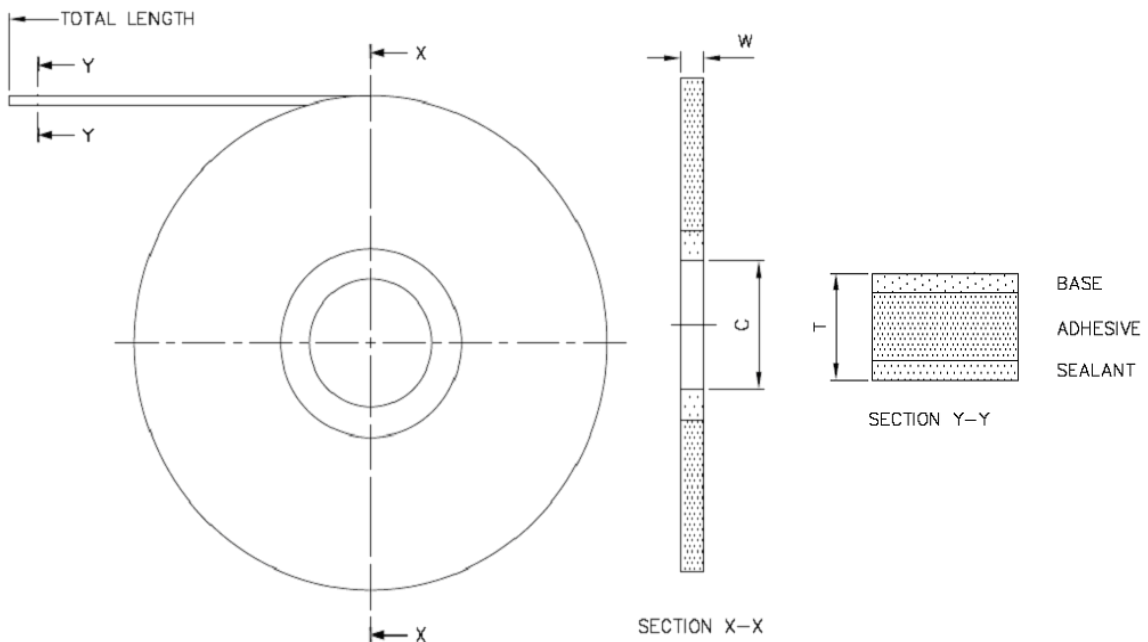
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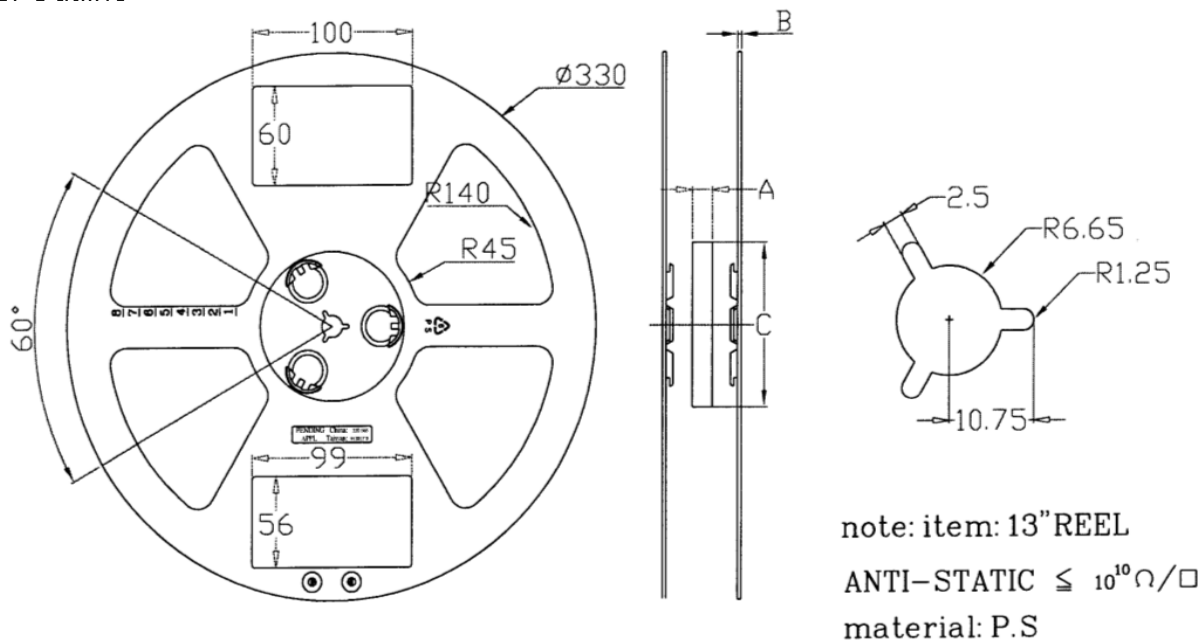2008 Chip Advanced Technology Inc. – All Right Reserved.

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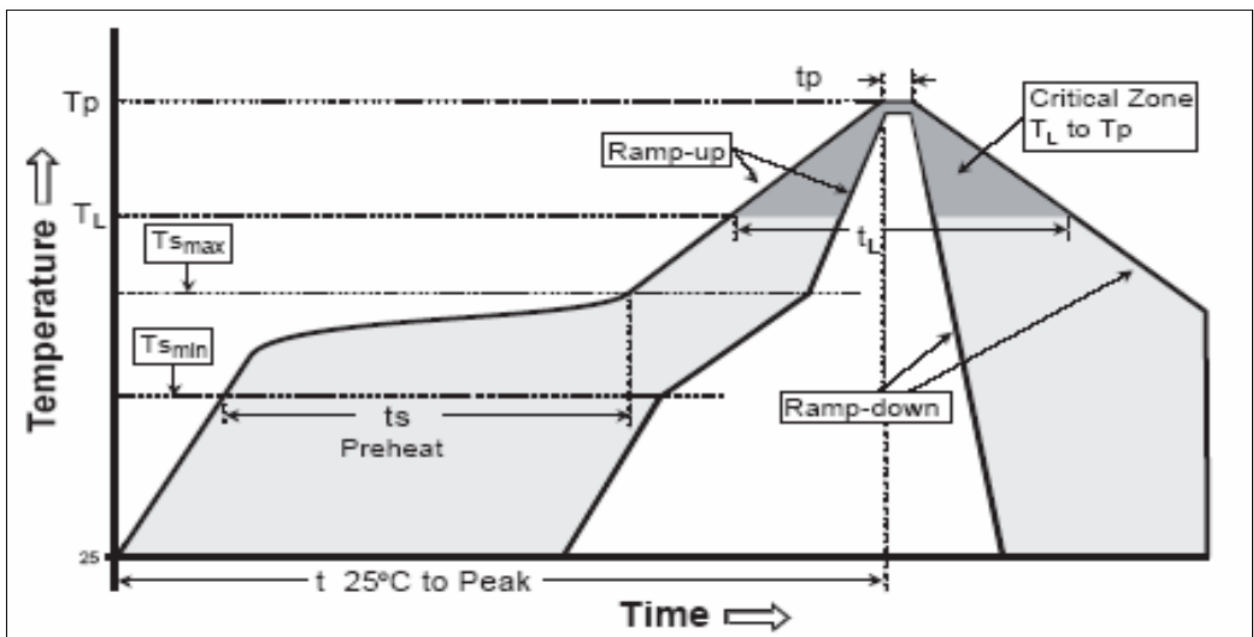
Carrier Tape & Reel Dimensions

Carrier Tape
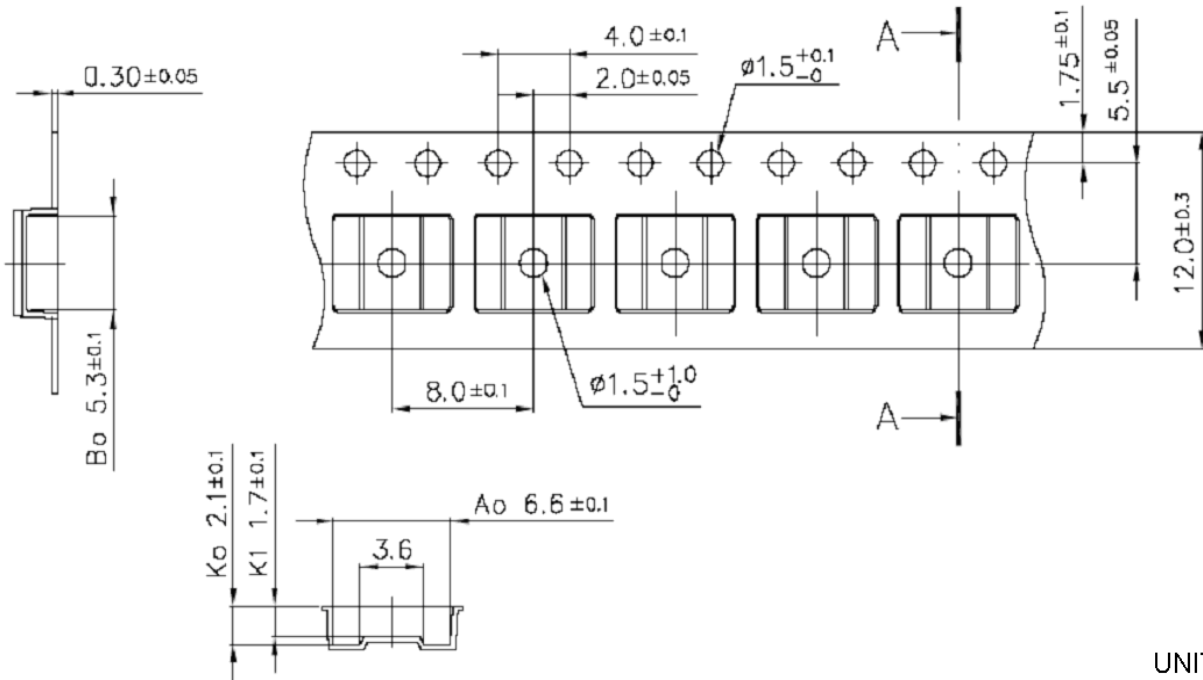
UNIT: mm.

Cover Tape

CARRIER TAPE WIDTH	C NOMINAL	T	W	TOTAL LENGTH
12mm	76.2mm	0.06±0.01mm	9.3±0.1mm	300M

Reel Outline

note: item: 13"REEL

ANTI−STATIC ≤ $10^{10}\Omega/\square$

material: P.S

SPEC	12	16	24	32	44	56	72
DIM A $^{+1.5}_{-0.5}$	12.5	16.5	24.5	32.5	44.5	57	73
DIM B ±0.2	2.3	2.3	2.3	2.3	2.3	2.3	2.3
DIM C ±1.5	99	99	99	99	99	99	99

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