Tensky International Co.,Ltd.

Expertise on thin film process

& circuit protection

Founded：March.2007

Factory Area：370.76m^2

Address：No.1,Lane 137,Sec 3,Jhongshan RD,Hukou Township,Hsinchu County 303,Taiwan(R.O.C)

Office:No.135, Chenggong 2nd St . ,Jhubei City , Hsinchu County 302,Taiwan (R.O.C.)

2007 founded for ceramic parts and process ceramic by CNC.

2009 Cooperate with PCB and semiconductor factory dedicated to apply the thin film & lithography process on Alumina / Aluminium Nitride substrate to make passive and circuit components. With both circuit design and processing capabilities, Tensky can offer OEM/ODM manufacturing service for products with circuits on ceramic substrate.

2010 Building branch office in Ningbo and Shenzhen China in near months.

Company advance:

POTENT MACHINERY & INDUSTRY CO.,LIMITED(Xiamen)

- Tensky was established by a group of engineers with innovative processing on ceramic capability.
- Our vision is to be the most advanced manufacturing service provider on ceramic parts and substrate to designers, and become the most reliable partner for all customers.
- Tensky will strive to provide superior manufacturing service on thin/thick film processing integration for all application fields.

Design Rule of Ceramic Substrate

- Substrate Materials
- Wafer Drawing
- Metalized Materials/Design

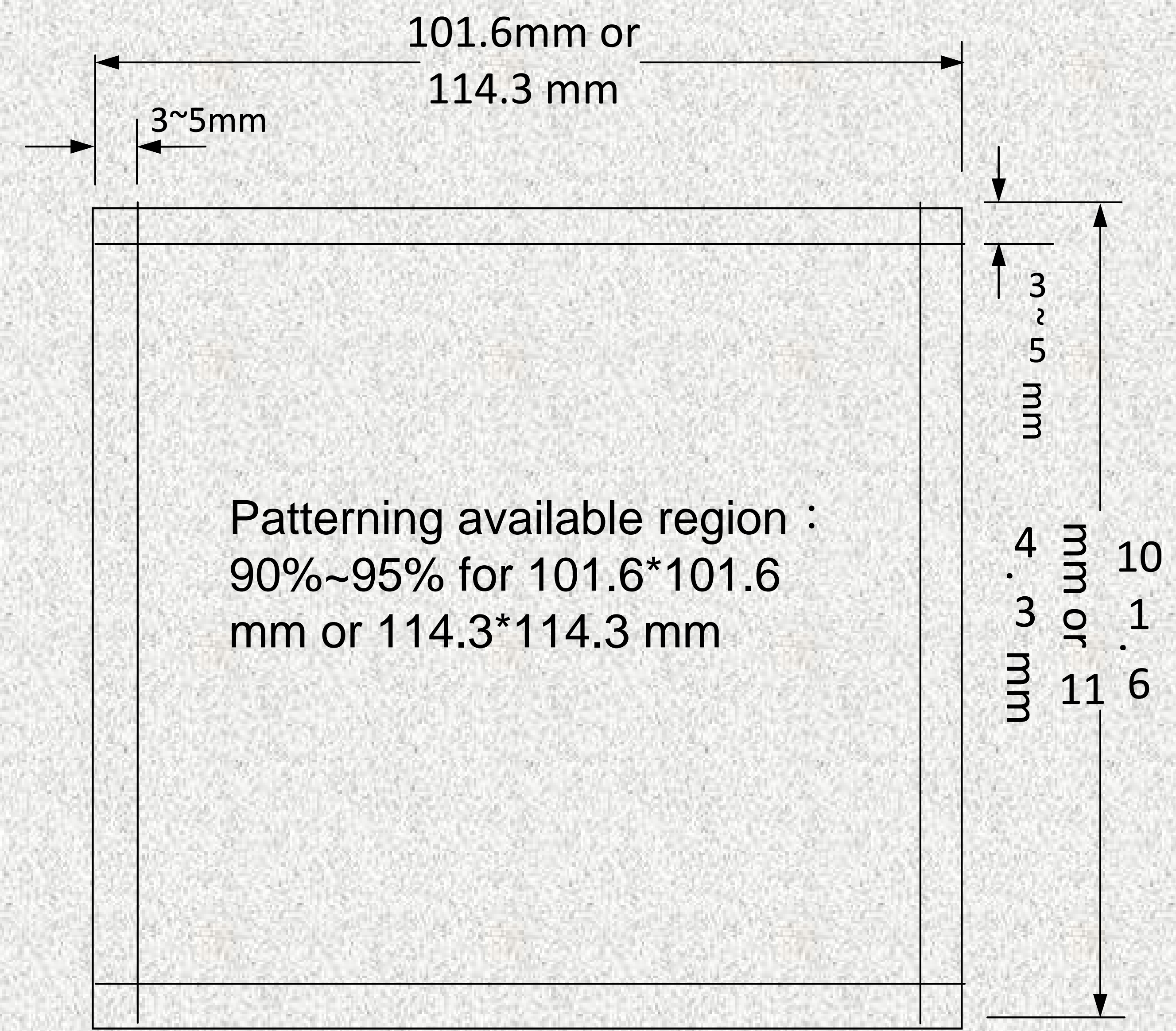
Substrate Materials

Material	Typical thickness (mm)	Typical dimension	Thermal conductivity
Al2O3 Wafer	0.38/ 0.5 /0.635/1mm	3"/ 4"/ 4.5"	20~27 W/mK
Al2O3 Chip	0.38/ 0.5 /0.636	Customized	
AlN Wafer	0.38/ 0.5 /0.637	3"/ 4"/ 4.5"	170~200 W/mK
ALN Chip	0.38/ 0.5 /0.638	Customized	

Wafer Drawing

Material	Pattern construction	Laser drill for via-holes	Laser scribing	Line width for dicing saw	Clearance distance from edge to metalized pattern
Al2O3 Wafer	Single Face Double face With Via-holes Customized	80~200 um, 150 um typically	1/4~1/2 substrate thickness , 1/3 substrate thickness typically	150~300 um, 200 um typically	6mm (as the thickness of the metalized layer less than 30 um)； 8 mm (as the thickness of the metalized layer higher than 30 um)
AlN Wafer					
Al2O3 Chip					
ALN Chip					

Patterning Available Region



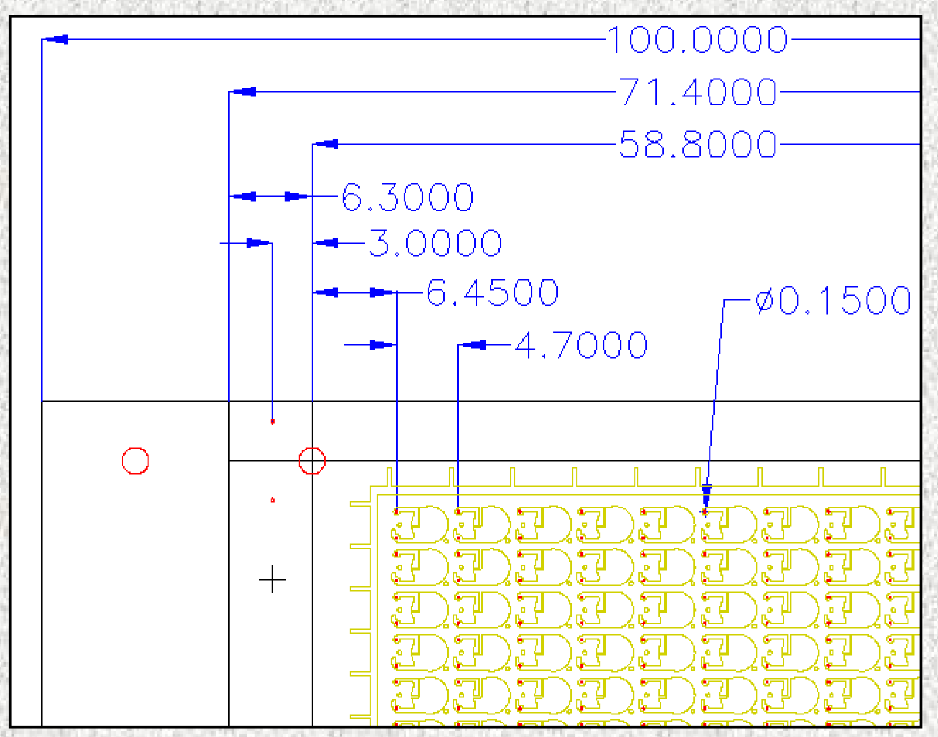
Metalized Materials

<table>
<tr><th rowspan="2">Material</th><th colspan="3">Matalized Material/Thickness</th><th rowspan="2">Conducting material of the via-holes</th><th rowspan="2">Line width* tolerance</th></tr>
<tr><th>Cu</th><th>Ni</th><th>Au</th></tr>
<tr><td>Al2O3 Wafer</td><td rowspan="4">1 μm
10 μm
20 μm
30 μm
60 μm
70um
100um
Customized</td><td rowspan="4">2~5 um,
3~4 um
typically</td><td rowspan="4">0.03~1 um,
0.25~0.35
um typically</td><td rowspan="4">Sliver
Cooper
Sliver/Copper</td><td rowspan="4">50 μm
typically</td></tr>
<tr><td>AlN Wafer</td></tr>
<tr><td>Al2O3 Chip</td></tr>
<tr><td>ALN Chip</td></tr>
</table>

Note*：The limit of the line width of the metalized pattern is depended on the thickness of the metalized material. The ratio of the line width limit and metalized metal thickness is 3:1 (For example: As the metalized metal thickness is 33 um and the line width limit will be 99 um).

Engineering Drawing

- Yellow line ：
  Metalized pattern.
- Black line ：
  Scribing line.
- Red line ：
  Through holes.
- Blue line ：
  Dimension marked.



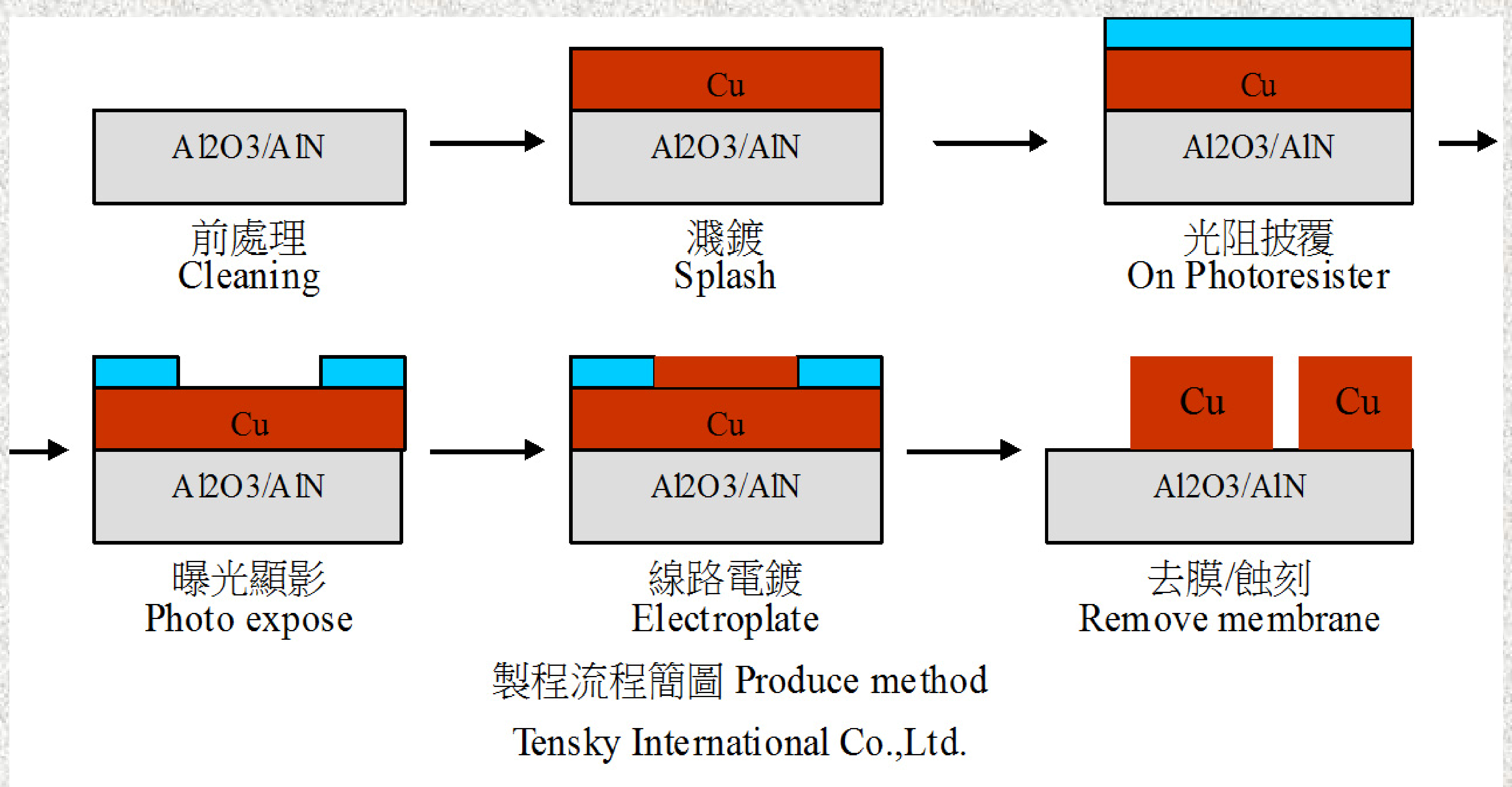
Benchmark of Various Substrate Materials

	FR-4 PCB	Metal Core PCB (MCPCB)	LTCC Ceramic Substrate	Thick-Film Ceramic substrate	DPC/Thin-Film Ceramic Substrate (Al2O3)	DPC/Thin-Film Ceramic Substrate (AlN)
Thermal conductivity	0.3~0.4 W/mK	0.7~3 W/mK	2~5 W/ mK	15~20 W/mK	20~27 W/ mK	170~190 W/mK
Resolution	50 μm	50 μm	150 μm	150 μm	10 μm	10 μm
Graduated Difference	<10 μm	<10 μm	> +/- 200 μm	> +/- 200 μm	<10 μm	<10 μm
Applications	Suitable for low power applications (<0.5W)	Suitable for middle power applications (<1W)	Suitable for middle power applications (<1W)	Suitable for middle power applications (<1 W)	Suitable for high power applications (1~3W)	Suitable for high power applications (1~10W)
Cost	Low	Middle	Middle-high	Middle	Middle-high	Higher
Wire bonding available	Yes	Yes	Yes	Yes	Yes	Yes
Eutetic bonding available	N/A	N/A	No	Poor	Yes	Yes
Flip chip bonding available	N/A	N/A	No	Poor	Yes	Yes

Compare with Thick & Thin Film Process

Item	Thick film	Thin film /DPC
Accuracy	+/- 10%	+/- 1%
Adhesion	Low (especially on AlN substrate)	High
Surface roughness	Low (1~3 μm)	High (<0.3 μm)
Real image		

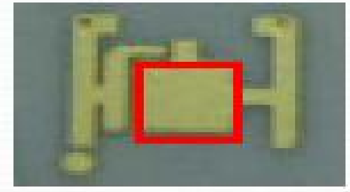
Sketch of Produce flow chart



Thermal Shock Test Content

- Test date：2010/06/10~2010/06/30
- Test Item：LED Heat-Sink Substrate of 3535
- Purpose：Ceramic substrate reliable thermal test to observe and the pulling affection
- Condition：-40℃(30 min)~125℃(30min), 500 cycle - (MIL-STD-202.107G)
- Manner：The pulling machine to test adhesion
- Standard： Pulling ≧3Kgf。
- Test result：

Item	Pulling (Kgf)	Result	Item	Pulling (Kgf)	Result
1	3.84	OK	6	3.94	OK
2	3.93	OK	7	3.58	OK
3	3.42	OK	8	3.67	OK
4	4.04	OK	9	3.66	OK
5	3.56	OK	10	3.83	OK
				Average	**3.75**



Testing position

Application of the Manufacturing Process

- High power LED ceramic substrate
- Flip chip /eutectic substrate manufacturing
- HCPV heat-sink of the solar cell
- Sensor ceramic substrate
- ESD/EMI protect design
- Thin film passive/protect devices

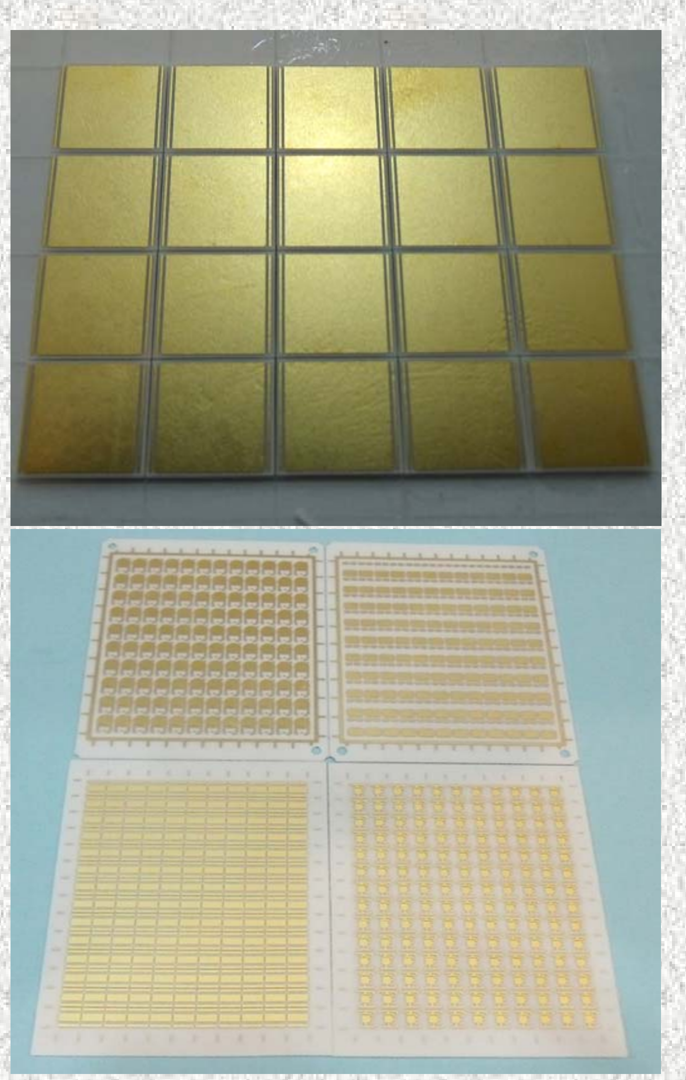
Manufacturing technology for ceramic substrate

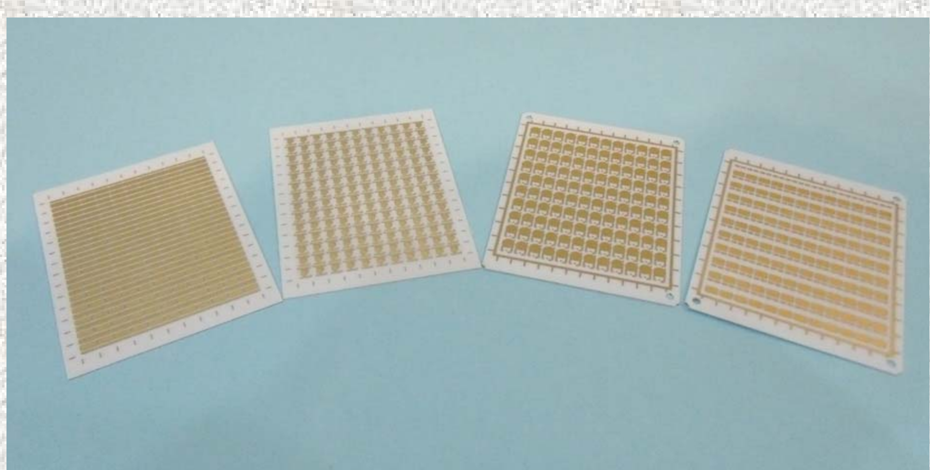
- Thin-film deposition technology
- Photo-lithography technology
- Electrode/electroless plating technology
- Micro-pattern design and manufacturing integrated technology

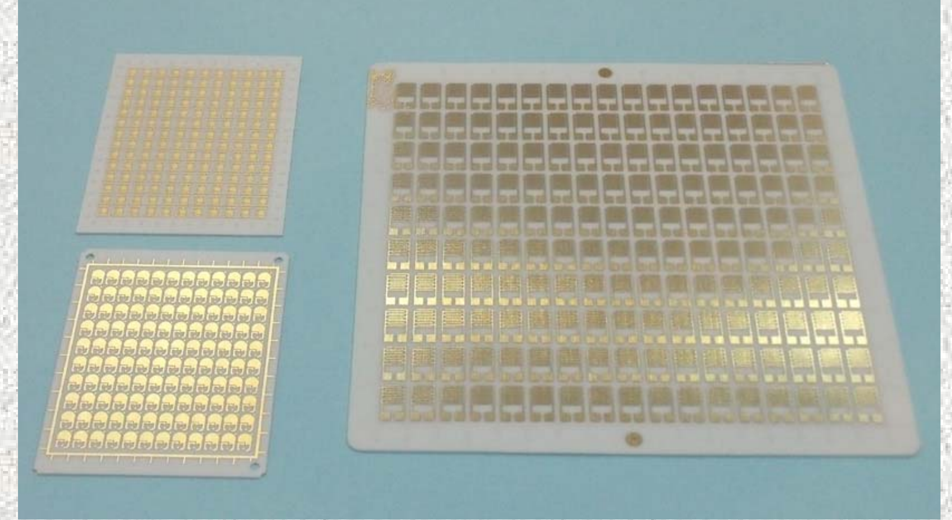
Manufacturing technology (I)

- Major manufacturing equipment for substrate

Thin Film(DPC) Manufacturing Products







Thanks for Your Attention