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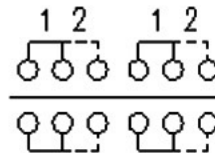
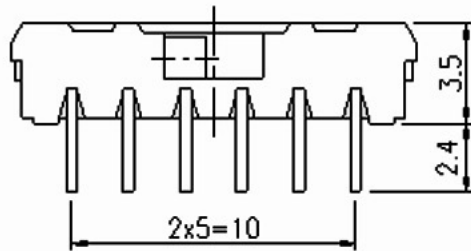
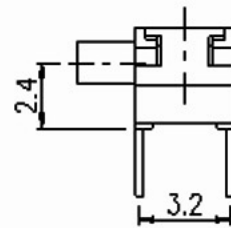
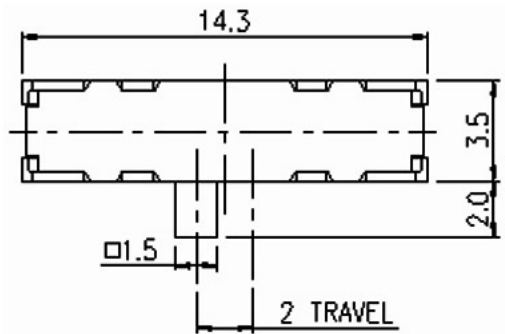
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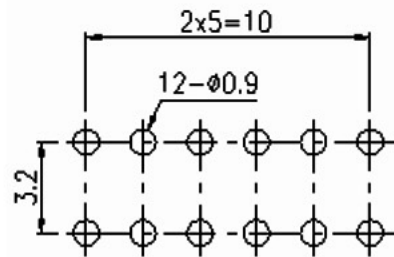
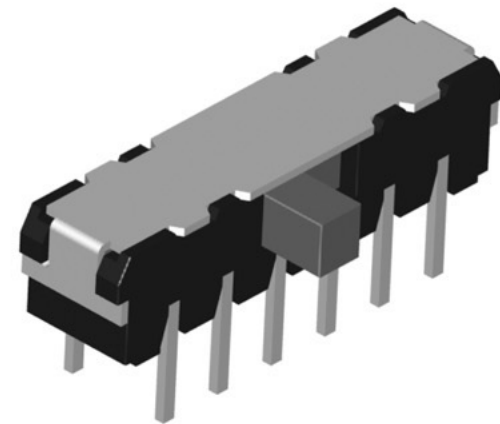
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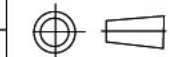
CIRCUIT



HOLE LAYOUT

KEMEI ELECTRONICS CO., LTD

TITLE:		MODEL NO:	
DRAWING No	MSK-42D01-G2	TOLERANCE	± 0.2
DRAWN BY	周细鹏	DATE	2008/11/22
CHECKED BY	付任保	DATE	2008/11/24
APPROVED BY		DATE	



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