Product specification

UBA2014

600V driver IC for HF fluorescent lamps

Tentative specification

2001 September 28
v2.2

Philips
Semiconductors

PHILIPS

600V driver IC for HF fluorescent lamps UBA2014

FEATURES

- adjustable preheat time
- adjustable preheat current
- current controlled operating
- single ignition attempt
- adaptive non-overlap time control
- integrated high voltage level-shift function
- powerdown function
- protection against lamp failures or lamp removal
- capacitive mode protection

GENERAL DESCRIPTION

The IC is a monolithic integrated circuit for driving electronically ballasted fluorescent lamps, with mains voltages up to 277V-rms (nominal value).
The circuit is made in a 650V BCD power-logic process.It provides the drive function for the 2 discrete power MOS-FET's.
Beside the drive function the IC also includes the level-shift circuit, the oscillator function, a lamp voltage monitor, a current control function, a timer function and protections.

APPLICATION

The circuit topology enables a broad range of ballast applications at different mains voltages for driving lamp types from e.g. T8, T5, PLC, T10, T12, PLL and PLT.

ORDERING INFORMATION

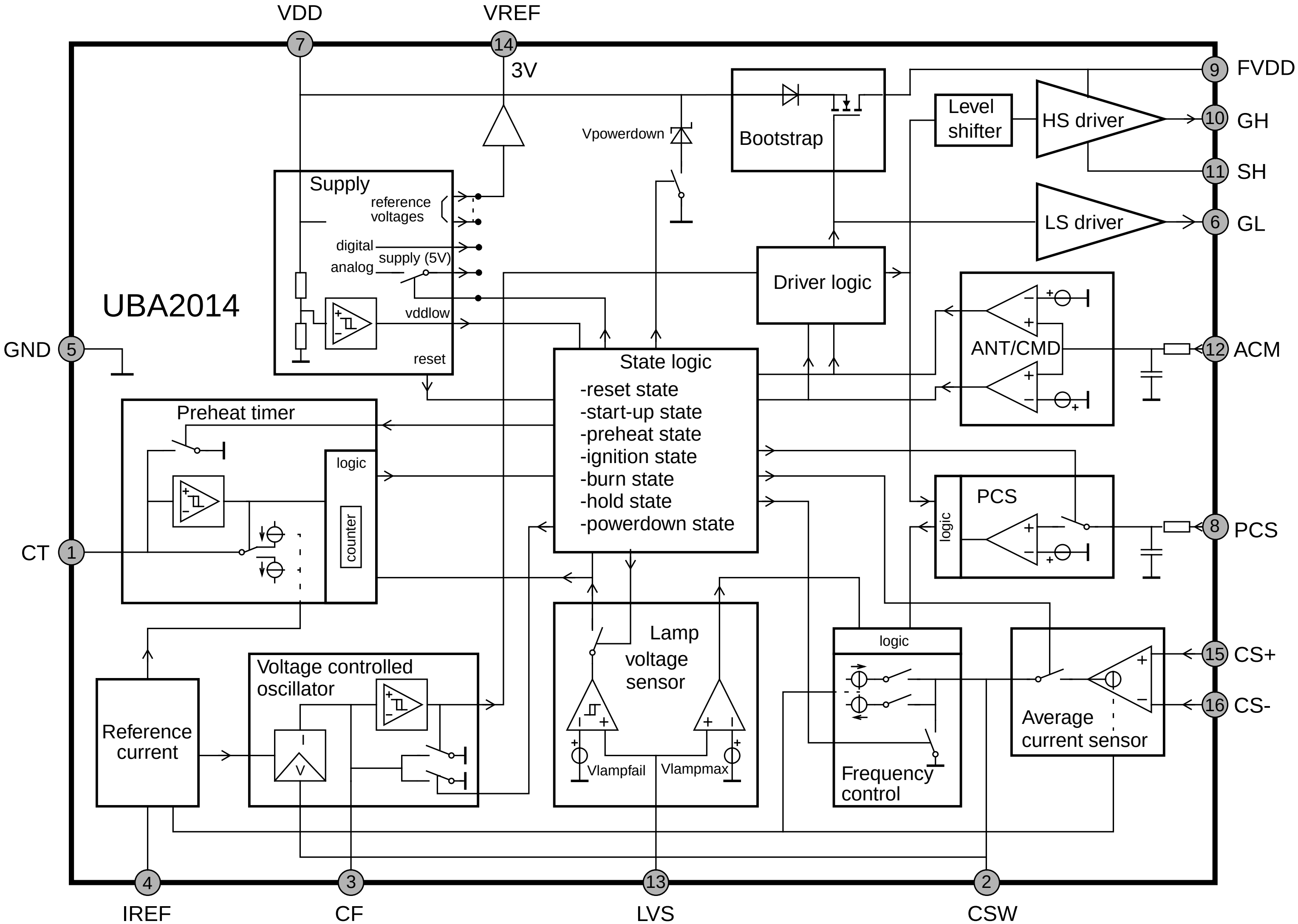
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA2014T	SO16	plastic small outline package; 16 leads	SOT109
UBA2014P	DIP16	dual in line package; 16 leads	SOT38

QUICK REFERENCE

(Voltages with respect to the GND pin, VDD=13V and V_{FVDD}-V_{SH}=13V, and Tamb=25^{0}C unless otherwise specified) see test application circuit.

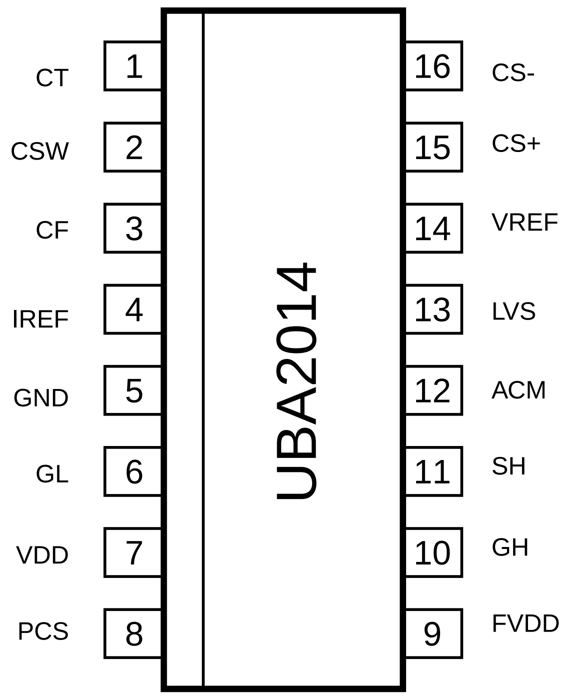
PARAMETER	CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
HIGH VOLTAGE SUPPLY						
High side supply	I_{HS}<30µA t<1s	V_{HS}			600	V
START-UP STATE						
Start of oscillation		VDD_{high}	12.4	13.0	13.6	V
Stop of oscillation		VDD_{low}		9.1		V
Start-up current	VDD<VDD_{high}	$I_{VDDstart}$		170	200	µA
REFERENCE VOLTAGE						
Reference voltage	Iload = 10µA	V_{VREF}		2.95		V
VOLTAGE CONTROLLED OSCILLATOR						
Max. bridge frequency		f_{max}		100		kHz
Min. bridge frequency		f_{min}	38.9	40.5	42.1	kHz
OUTPUT DRIVERS						
Ouput driver source current	V_{GH}-V_{SH}=0, V_{GL}=0	I_{GHo}		180		mA
Output driver sink current	V_{GH}-V_{SH}=13V	I_{GHi}		300		mA
PREHEAT CURRENT SENSOR						
Preheat voltage level	at the PCS pin	V_{pre}		0.60		V
LAMP VOLTAGE SENSOR						
Lampfail voltage level	at the LVS pin	$V_{lampfail}$	0.77	0.81	0.85	V
Max. lampvoltage level	at the LVS pin	$V_{lampmax}$	1.44	1.49	1.54	V
AVERAGE CURRENT SENSOR						
Offset voltage	V_{CS} is 0 to 2.5V	V_{offset}	-2	0	+2	mV
Transconductance	f=1kHz	g_m		3800		µA/mV
TIMER						
Preheat time	C_{CT}=330nF and R_{IREF}=33kΩ	T_{pre}	1.6	1.8	2.0	s
Low level CT		CT_{low}		1.4		V
High level CT		CT_{high}		3.6		V

BLOCK DIAGRAM



PINNING

SYMBOL	PIN	DESCRIPTION
CT	1	output of the preheat timer
CSW	2	input of the voltage controlled oscillator
CF	3	output oscillator
IREF	4	input for the internal reference current
GND	5	ground
GL	6	gate of the low-side switch
VDD	7	low voltage supply
PCS	8	input preheat current sensor
FVDD	9	floating supply, supply for the high-side switch
GH	10	gate of the high-side switch
SH	11	source of the high-side switch
ACM	12	input capacitive mode
LVS	13	input lamp voltage sensor
VREF	14	reference voltage
CS+	15	positive input of the average current sensor
CS-	16	negative input of the average current sensor



PIN CONFIGURATION
(package drawn is SO16)

FUNCTIONAL DESCRIPTION

Start-up state

Initial start-up can be achieved by means of charging the VDD capacitor (C7 in the test application circuit) with an external start-up resistor. Start-up of the circuit under the condition that both half-bridge transistors TR1 and TR2 are non-conductive. In the start-up state the circuit will be resetted. If the low voltage supply (VDD) reaches the value of VDD_{high} the circuit starts oscillating. A DC reset circuit is incorporated in the high-side (HS) driver. Below the lockout voltage at the FVDD pin the output voltage (V_{GH}-V_{SH}) is zero. The voltages at CF and CT are zero during the start-up state.

Oscillation

The internal oscillator is a voltage-controlled circuit (VCO) which generates a sawtooth between the CF_{high} level and 0V. The frequency of the sawtooth is determined by capacitor C_{CF}, resistor R_{IREF}, and the voltage at the CSW pin. The minimum and maximum switching frequency are determined by R_{IREF} and C_{CF}. Their ratio is internally fixed. The sawtooth frequency is twice the half-bridge frequency. The UBA2014 brings alternately the transistors TR1 and TR2 in conduction with a duty cycle of about 50%. An overview of the oscillator signal and driver signals is given in Fig.2. The oscillator starts oscillating at f_{max}. During the first switching cycle the low-side (LS) transistor is switched on. The first conducting time is made extra long to be able to charge the bootstrap capacitor.

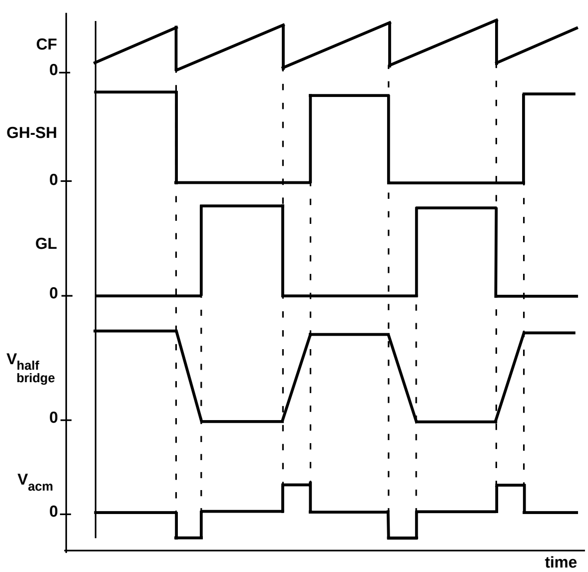


Fig. 2 Oscillator and driver signals

Adaptive non-overlap

The non overlap time is realized with an adaptive non-overlap circuit (ANT). With an adaptive non-overlap, the application determines the duration of the non-overlap and makes the non-overlap time optimal for each frequency (also see Fig. 2). The non-overlap time is determined by the slope of the half bridge voltage, and is detected by the signal across resistor R16 directly connected to the ACM pin. The minimum non-overlap time is internally fixed. The maximum non-overlap time is internally fixed at about 25% of the bridge period time. An internal filter of 30ns is included at the ACM pin to increase the noise immunity.

Timing circuit

A timing circuit is included to determine the preheat time and the ignition time. The circuit consists of a clock generator and a counter. The preheat time is defined by C_{CT} and R_{IREF} and consists of 7 pulses at C_{CF}. The (maximum) ignition time is 1 pulse at C_{CF}. The timing circuit starts operating after the start-up state, as soon as the supply (VDD) has reached VDD_{high} or when a critical value of the lamp voltage ($V_{lampfail}$) is exceeded. When the timer is not operating C_{CF} is discharged to 0V by 1mA.

Preheat state

After starting at f_{max}, the frequency decreases until the momentary value of the voltage across sense resistor R14 reaches the internally fixed preheat voltage level (PCS pin). At crossing the preheat voltage level, the output current of the preheat current sensor circuit (PCS) discharges the capacitor C_{CSW}, thus raising the frequency. The preheat time begins at the moment that the circuit starts oscillating. During the preheat time the average current sensor circuit (ACS) is disabled. An internal filter of 30ns is included at the PCS pin to increase the noise immunity.

Ignition state

See Fig.3. After the preheat time the ignition state is entered and the frequency will sweep down due to charging the capacitor at the CSW pin with an internally fixed current. During this continuously decreasing in frequency, the circuit approaches the resonance frequency of the load. This will cause a high voltage across the load, which normally ignites the lamp.
The ignition voltage of a lamp is designed above the $V_{lampfail}$ level. If the lampvoltage passes the $V_{lampfail}$ level the ignition timer is started.

Burn state

See Fig.3. If the lampvoltage does not exceed the $V_{lampmax}$ level the voltage at the CSW pin will remain increasing until the clamp level at the CSW pin is reached. As a consequence the frequency will decrease until the minimum frequency is reached.
When the frequency reaches its minimum it is assumed that the lamp has ignited and the circuit enters the burn state. The average current sensor circuit (ACS) will be enabled. As soon as the averaged voltage across sense resistor R14, measured at the input CS-, reaches the reference level at CS+, the average current sensor circuit will take over the control of the lamp current. The average current through R14 is transferred to a voltage at the voltage controlled oscillator and regulates the frequency and, as a result, the lamp current.

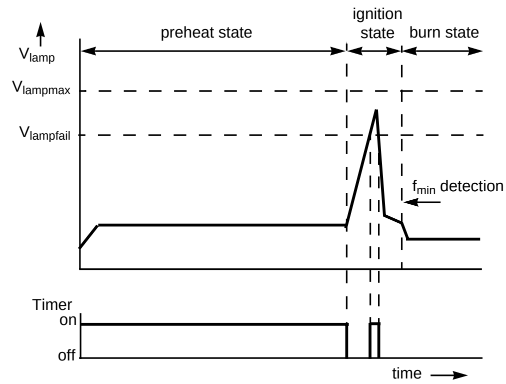


Fig.3 Normal ignition behaviour

Lamp failure mode

-During ignition state
See Fig.4a. If the lamp does not ignite, the voltage level increases. When the lamp voltage crosses the $V_{lampmax}$ level, the voltage will be regulated at the $V_{lampmax}$ level. At crossing the $V_{lampfail}$ level the ignition timer was already started. If the voltage at the LVS pin is above the $V_{lampfail}$ level at the end of the ignition time the circuit stops oscillation and is forced in a powerdown-mode. The circuit will be reset only by powering down the supply.

-During burn state
See Fig.4b. If the lamp fails during normal operation, the voltage across the lamp will increase, and the lamp voltage will cross the $V_{lampfail}$ level. At that moment the ignition timer is started. If the lamp voltage increases further it will reach the $V_{lampmax}$ level. This forces the circuit to re-enter the ignition state and results in an attempt to re-ignite the lamp. If during restart the lamp still fails, the voltage remains high until the end of the ignition time. At the end of the ignition time the circuit stops oscillating and the circuit will enter in the powerdown mode.

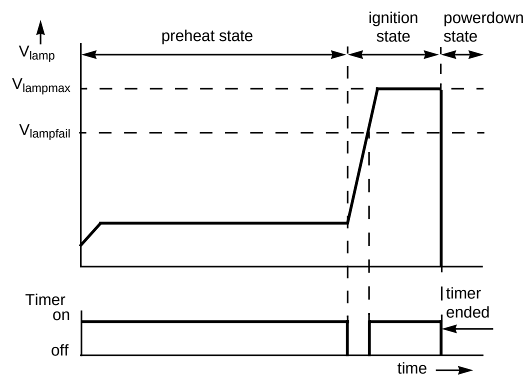


Fig.4a Failure mode during ignition

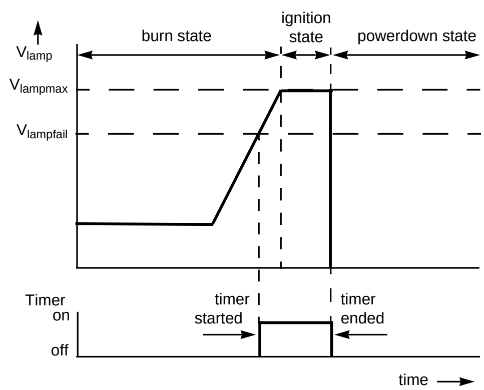


Fig.4b Failure mode during burn

Power down state

The powerdown state will be entered if at the end of the ignition time the voltage at the LVS pin is above $V_{lampfail}$. In the powerdown mode the oscillation will be stopped and both TR1 and TR2 are non-conductive. The VDD supply is internally clamped. The circuit is released out of the power down state by lowering the VDD below VDD_{reset}.

Capacitive mode protection

The signal across R16 also gives information about the switching behaviour of the half bridge.
If, after the preheat state, the voltage at ACM resistor R16 does not exceed the V_{CMD} during the non-overlap time, the capacitive mode detection circuit (CMD) assumes that the circuit is in capacitive mode of operation. As a consequence the frequency will directly be increased to f_{max}. Until C_{CSW} has been discharged to zero, the frequency behaviour is decoupled from the voltage at the CSW pin.

Charge coupling

Due to parasitic capacitive coupling to the high voltage circuitry are all pins burdened with a repetitive charge injection. Given the typical application the pins IREF and CF are sensitive to this charge injection. For charge coupling of +/-8pC, a safe functional operation of the IC is guaranteed, independent of the current level.
Charge coupling at current levels below 50 µA will not interfere with the accuracy of the V_{CS}, V_{PCS} and V_{ACM} levels.
Charge coupling at current levels below 20 µA will not interfere with the accuracy of any parameter.

Design equations

The following design equations are used to calculate the desired preheat time, the (maximum) ignition time, and the minimum and the maximum switching frequency.

$$T_{pre} = 1.7 \cdot 10^{-4} \cdot C_{CT} \cdot R_{IREF} \qquad [s]$$

$$T_{ign} = 3.1 \cdot 10^{-5} \cdot C_{CT} \cdot R_{IREF} \qquad [s]$$

$$f_{min} = 1.2 \cdot 10^{-2} \cdot C_{CF} \cdot R_{IREF} \qquad [kHz]$$

$$f_{max} = 2.5 \cdot f_{min} \qquad [kHz]$$

with C_{CT} in nF, R_{IREF} in kΩ, and C_{CF} in pF. Start of ignition is defined as the moment at which the measured lamp voltage crosses the $V_{lampfail}$ level, see section “Lamp failure mode”.

LIMITING VALUES (according to IEC134)

(Voltages with respect to the ground pin)

No		CONDITION	SYMBOL	MIN.	MAX.	UNIT
A	High side supply	I_{HS}<30µA t<1s	V_{HS}	600		V
B	High side supply	I_{HS}<30µA	V_{HS}	510		V
C	Max. voltage at pin ACM		V_{ACM}	-5	+5	V
D	Max. voltage at pin PCS		V_{PCS}	-5	+5	V
E	Max. voltage at pin LVS		V_{LVS}	0	+5	V
F	Max. voltage at pin CS+		V_{CS+}	0	+5	V
G	Max. voltage at pin CS-		V_{CS-}	-0.3	+5	V
H	Max. voltage at pin CSW		V_{CSW}	0	+5	V
I	Ambient temperature		T_{amb}	-25	+80	^{0}C
J	Junction temperature		T_j	-25	+150	^{0}C
K	Storage temperature		T_{stg}	-55	+150	^{0}C
L	electrostatic handling	see Note 1	V_{es}			
	pins FVDD,GH, SH and VDD			–	±1000	V
	pins GL, ACM, PCS, CS+, CS-, CSW, LVS, CF, IREF, CT and VREF			–	±2500	V

Note 1:

In accordance with the human body model, i.e. equivalent to discharging a 100pF capacitor through a 1.5kΩ series resistor.

THERMAL CHARACTERISTICS

SO16

SYMBOL	PARAMETER	VALUE	UNIT
Rth j-a	thermal resistance from junction to ambient in free air	100	K/W
Rth j-pin	thermal resistance from junction to pcb	50	K/W

DIP16

SYMBOL	PARAMETER	VALUE	UNIT
Rth j-a	thermal resistance from junction to ambient in free air	60	K/W
Rth j-pin	thermal resistance from junction to pcb	30	K/W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”*

CHARACTERISTICS

(Voltages with respect to the GND pin, VDD=13V and V_{FVDD}-V_{SH}=13V and T_{amb}=25^{0}C unless otherwise specified) see test application circuit.

No		CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
HIGH VOLTAGE SUPPLY							
1.0	Leakage current high voltage pins	FVDD, GH, SHS = 600V	$I_{leakage}$			30	µA
START-UP STATE							
3.0	Supply voltage for defined driver output	TR1=off, TR2=off	VDD			6	V
3.1	Start of oscillation		VDD_{high}	12.4	13.0	13.6	V
3.2	Stop of oscillation		VDD_{low}	8.6	9.1	9.6	V
3.3	Start-stop hysteresis		VDD_{hys}	3.5	3.9	4.4	V
3.4	Start-up current	$VDD<VDD_{high}$	$I_{VDDstart}$		170	200	µA
3.5	Clamp voltage	powerdown mode	VDD_{clamp}	10	11	12	V
3.6	Powerdown current	VDD=9V	I_{pdown}		170	200	µA
3.7	Reset voltage	TR1=off, TR2=off	VDD_{reset}	4.5	5.5	7.0	V
3.8	Operating supply current	f_{bridge}=40kHz without gate-drive	I_{VDD}		1.5	2.2	mA
REFERENCE VOLTAGE							
4.0	Reference voltage	Iload = 10µA	V_{VREF}	2.86	2.95	3.04	V
4.1	Current capability	source	I_{VREF}	1			mA
4.2	Current capability	sink	I_{VREF}	1			mA
4.3	Output impedance	Iload = 1 mA source	Z_{VREF}		3.0		Ω
4.4	Temp. coefficient	Iload = 10µA, 25-150˚C	$\Delta V_{VREF}/\Delta T$		-0.64		%/K
CURRENT SUPPLY							
5.0	Voltage at IREF		V_{IREF}		2.5		V
5.1	Reference current range		I_{IREF}	65		95	µA
VOLTAGE CONTROLLED OSCILLATOR							
6.0	Control voltage range		V_{CSW}	2.7	3.0	3.3	V
6.1	Clamp voltage	Burn state	V_{clamp}	2.8	3.1	3.4	V
6.2	CF start current	CF=1.5V	$I_{CFstart}$	3.8	4.5	5.2	µA
6.2a	First CF stroke		t_{start}		50		µs
6.3	Min. CF current	CF=1.5V	I_{CFmin}		21		µA
6.4	Max. CF current	CF=1.5V	I_{CFmax}		54		µA
6.5	Max. bridge frequency		f_{max}	90	100	110	kHz
6.6	Min. bridge frequency		f_{min}	38.9	40.5	42.1	kHz
6.7	Frequency stability	T_{amb}:-20 to +80ºC	Δf		1.3		%
6.8	High level CF	$f=f_{min}$	CF_{high}		2.5		V
6.9	Min. non overlap time GH-GL		T_{ncmin}	0.68	0.90	1.13	µs
6.A	Min. non overlap time GL-GH		T_{ncmin}	0.75	1.00	1.25	µs
6.B	Max. non overlap time	f_{bridge}=40kHz - see Note 2	T_{ncmax}		7.5		µs

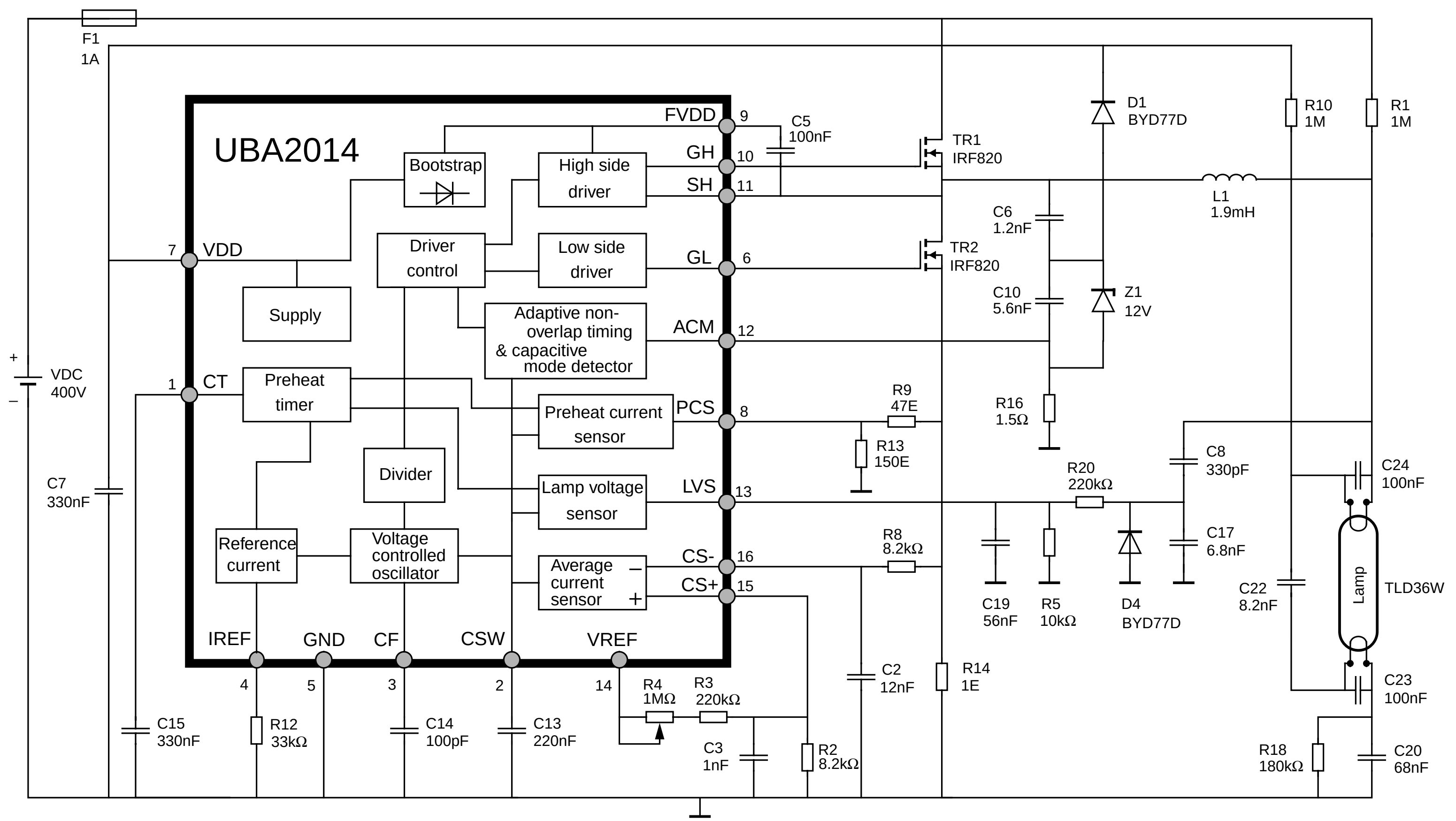
No		CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
OUTPUT DRIVERS							
7.0	High side output source current	V_{GH}-V_{SH}=0	I_{GHo}	135	180	235	mA
7.1	High side output sink current	V_{GH}-V_{SH}=13V	I_{GHi}	265	330	415	mA
7.2	Low side output source current	V_{GL}=0	I_{GLo}	135	200	235	mA
7.3	Low side output sink current	V_{GL}=13V	I_{GLi}	265	330	415	mA
7.4	Highside output voltage ‘high’	Iout=10mA	V_{GHh}	12.5			V
7.5	Highside output voltage ‘low’	Iout=10mA	V_{GHl}			0.5	V
7.6	Lowside output voltage ‘high’	Iout=10mA	V_{GLh}	12.5			V
7.7	Lowside output voltage ‘low’	Iout=10mA	V_{GLl}			0.5	V
7.8	High side on resistance	Iout=10mA	R_{HSon}	32	39	45	Ω
7.9	High side off resistance	Iout=10mA	R_{HSoff}	16	21	26	Ω
7.A	Low side on resistance	Iout=10mA	R_{LSon}	32	39	45	Ω
7.B	Low side off resistance	Iout=10mA	R_{LSoff}	16	21	26	Ω
7.C	Bootstrap diode fwd drop	I=5mA	V_{boot}	1.3	1.7	2.1	V
7.D	Lockout voltage		V_{FVDD}	2.8	3.5	4.2	V
7.E	Floating well supply current	DC at V_{GH}-V_{SH}=13V	I_{FVDD}		35		µA
PREHEAT CURRENT SENSOR							
8.0	Input current	V_{PCS}=0.6V	I_{PCS}			1	µA
8.1	Preheat voltage level	at the PCS pin	V_{pre}	0.57	0.60	0.63	V
8.2	Output source current	V_{CSW}=2.0V	I_{CSW}	9.0	10	11	µA
8.3	Effective output sink current	V_{CSW}=2.0V	I_{CSW}		10		µA
ADAPTIVE NON-OVERLAP AND CAPACITIVE MODE DETECTION							
8.5	Input current	V_{ACM}=0.6V	I_{ACM}			1	µA
8.4a	Capacitive mode detection level		V_{CMD+}	+80	+100	+120	mV
8.4b	Capacitive mode detection level		V_{CMD-}	-68	-85	-102	mV
LAMP VOLTAGE SENSOR							
9.0	Input current	V_{LVS}=0.81V	I_{LVS}			1	µA
9.1	Lampfail voltage level	at the LVS pin	$V_{lampfail}$	0.77	0.81	0.85	V
9.2	Hysteresis lampfail voltage level	at the LVS pin	V_{lfhys}	119	144	169	mV
9.3	Max. lampvoltage level	at the LVS pin	$V_{lampmax}$	1.44	1.49	1.54	V
9.4	Output sink current	V_{CSW}=2.0V	I_{CSW}	27	30	33	µA
9.5	Ignition output source current	V_{CSW}=2.0V	I_{CSW}	9.0	10	11	µA
AVERAGE CURRENT SENSOR							
10.0	Input current	Vcs=0V	I_{CS}			1	µA
10.1	Offset voltage	$V_{CS+/-}$ is 0 to 2.5V	V_{offset}	-2	0	+2	mV
10.2	Transconductance	f=1kHz	g_m	1900	3800	5700	µA/mV

No		CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
10.3	Output current	source and sink, V_{CSW}=2V	I_{CSW}	85	95	105	µA
TIMER							
11.0	CT current	V_{CT}=2.5V	I_{CT}	5.5	5.9	6.3	µA
11.1	Low level CT		CT_{low}		1.4		V
11.2	High level CT		CT_{high}		3.6		V
11.3	Hysteresis CT		CT_{hys}	2.05	2.20	2.35	V
11.4	Preheat time	C_{CT}=330nF and R_{IREF}=33kΩ	T_{pre}	1.6	1.8	2.0	s
11.5	Ignition time	C_{CT}=330nF and R_{IREF}=33kΩ	T_{ign}		0.26		s

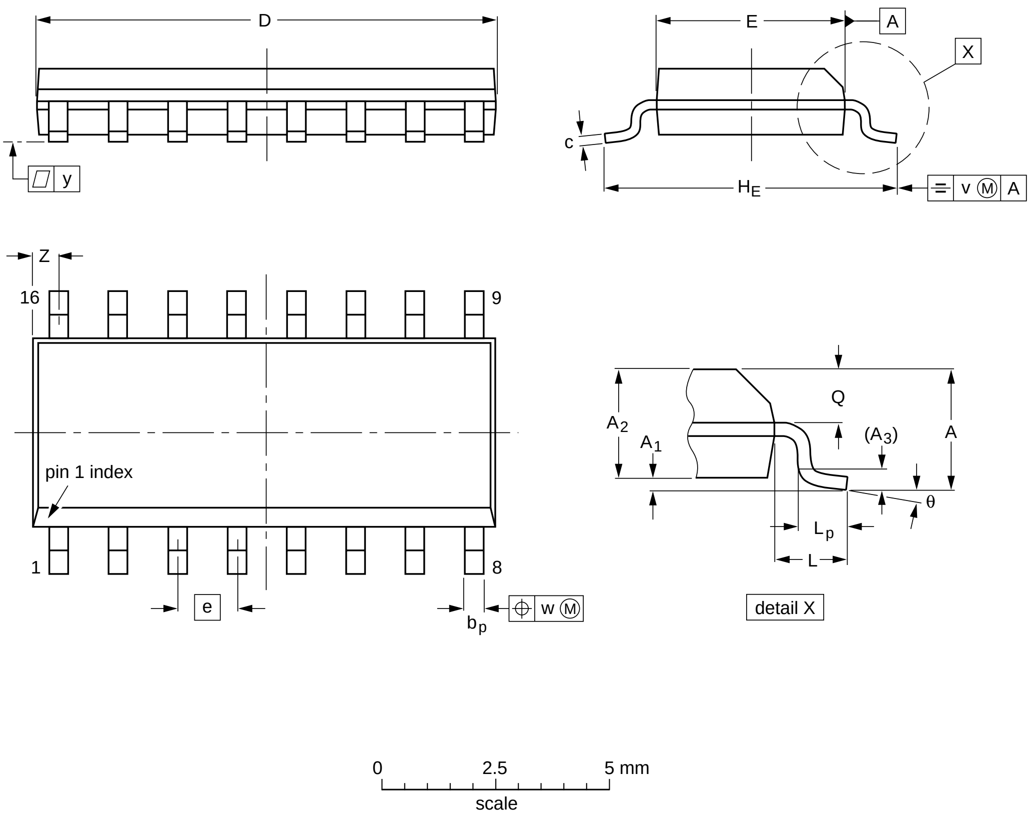
Note 2:

The maximum non-overlap is determined by the level of the CF signal. If this signal crosses a level of 1.25V the non-overlap will end, resulting in a maximum non-overlap time of 7.5µs at a bridge frequency of 40kHz.

TEST APPLICATION CIRCUIT



SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

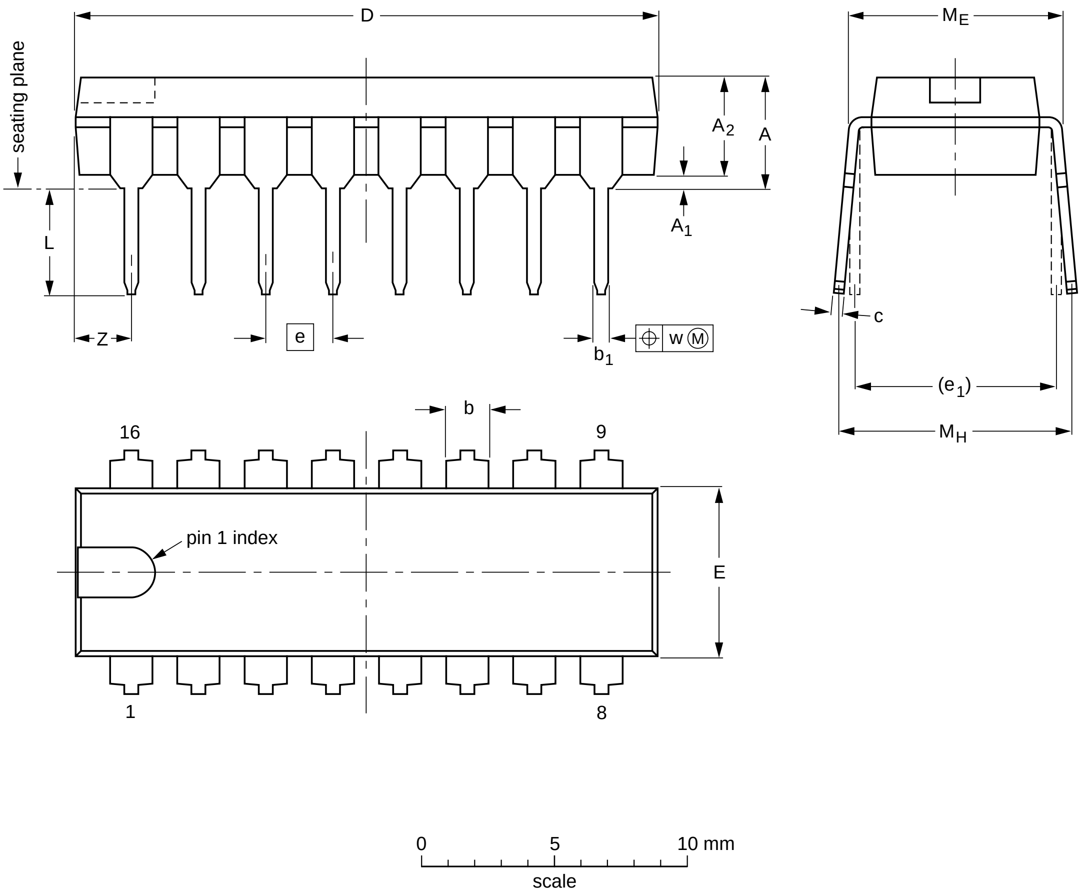
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

36W TLD application with UBA2014

FACT SHEET

Philips Semiconductors

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FACT SHEET

36W TLD application with UBA2014

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CONTENTS

1. INTRODUCTION

The UBA2014 integrated Half Bridge driver IC has been designed for driving electronically ballasted fluorescent lamps. The IC provides the drive function for 2 discrete Power MosFets. Besides the drive function the IC also includes the level-shift circuit, the oscillator , a lamp voltage monitor, a current control function a timer function and protections.

This fact sheet will give a description of a typical integrated 36W TLD application. The Voltage Fed Half Bridge is supplied by a constant 400Vdc supply (either an external or a PFC supply). This topology allows to easily operate in Zero Voltage Switching (ZVS) series resonant mode, thus reducing the transistor switching losses and the electromagnetic interference. During the preheat time the UBA2014 controls the current which flows in the filament of the lamp. To provide long life and insure an efficient ignition of the lamp the preheat timer and control system determine the optimal preheat time and preheat current. After the preheat time the lamp must be ignited by reducing the switching frequency and thus increasing the voltage across it. The IC controls the maximum ignition voltage and the ignition timer determines the maximum ignition time. During this phase the Capacitive Mode protection ensures a safe operation of the Power MosFets. In the Burn phase the lamp current is controlled by the Average Current System. In this phase the lamp can be dimmed to a low level by frequency dimming.

The UBA2014 has protections for lamp ageing, lamp failures and lamp removal. The Power Down function can safely switch off the power inverter.

2. FEATURES

- Integrated Half Bridge Power IC for fluorescent applications
  - integrated high side / low side , including bootstrap circuitry
  - based upon BCD 650V power-logic technology
  - accurate oscillator and timer
  - adjustable frequency range (with fixed fmax/fmin ratio)
  - adaptive non-overlap time control
  - capacitive mode protection
  - adjustable preheat current and time control
  - single ignition attempt
  - powerdown function
- soft start by frequency sweep down from start frequency
- adjustable ignition voltage control
- lamp current control
- down to 10% dimming
- protection against lamp failures or lamp removal
- SO16, DIP16 package

3. APPLICATION PHOTO

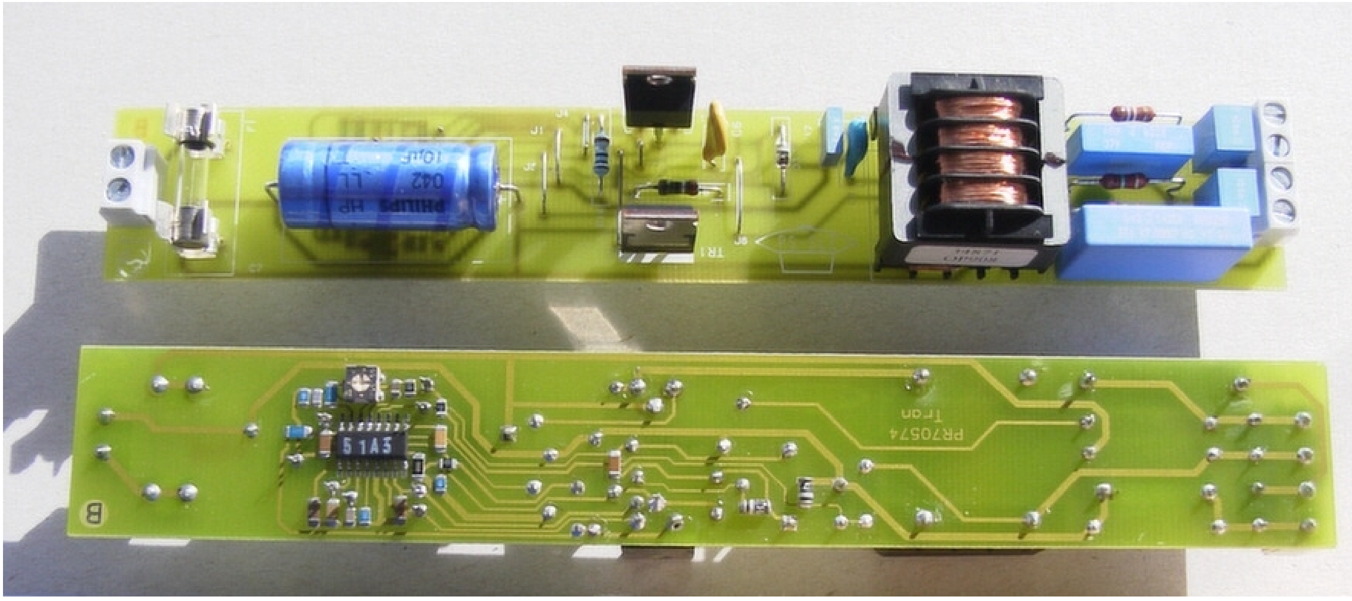

Figure 1: The Printed Circuit Board of the UBA2014 application.

4. CIRCUIT DIAGRAM.

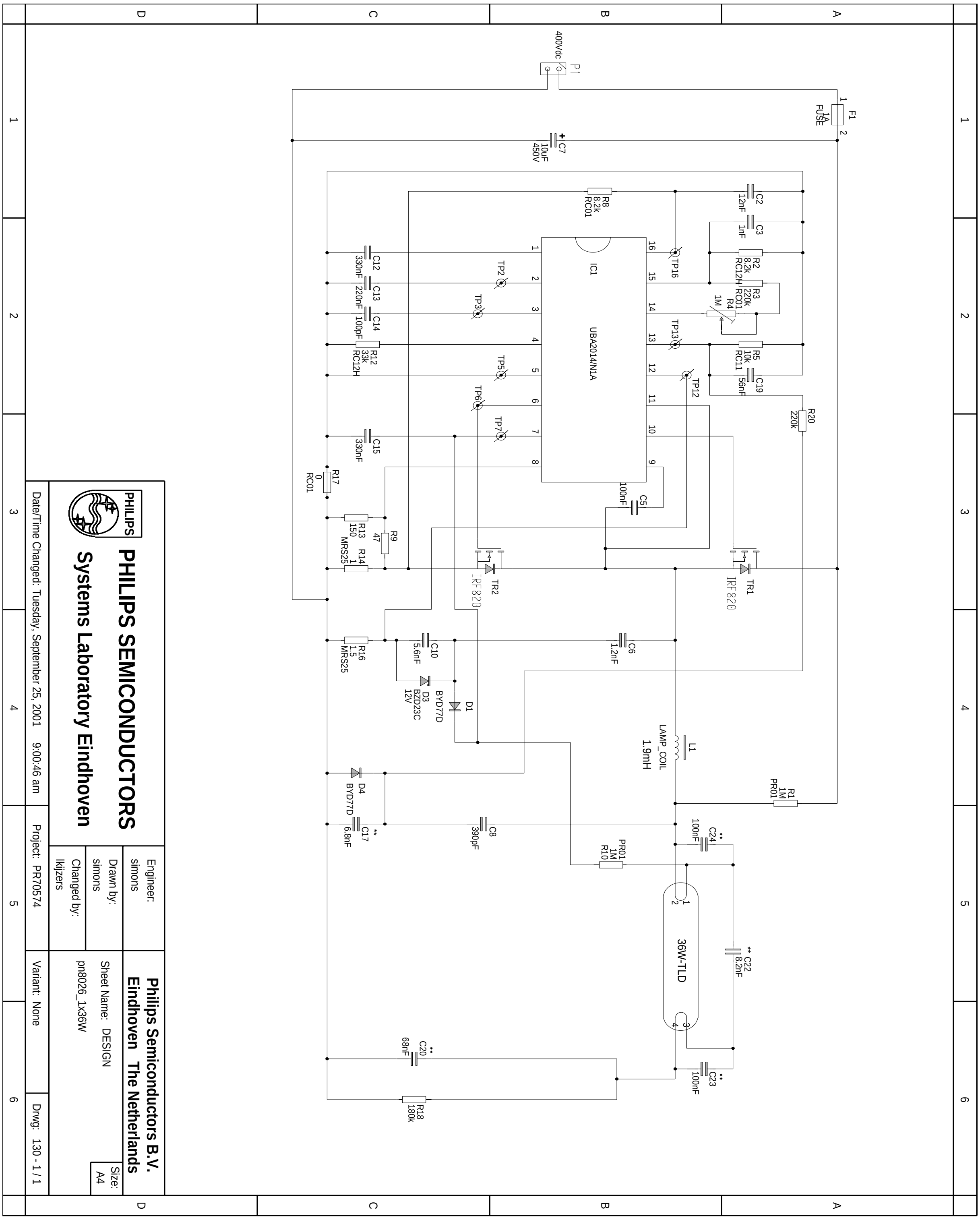

Figure 2

5. PARTSLIST

REFERENCE	PART_NO	COMPONENT	SERIES	RATING	TOLERANCE	VENDOR	GEOMETRY
C2	2222-591-16628	12nF	12NC_update	50V	5%	PHYCOMP	C1206
C3	2222-861-12102	1nF	12NC_update	50V	5%	PHYCOMP	C0805
C5	2222-581-16641	100nF	12NC_update	50V	5%	PHYCOMP	C1206
C6	ECKA3A122KBP	1.2nF	Hi_voltage	1000V	10%	Panasonic	C_B3_L7_P5mm
C7	2222-043-17109	10uF	ASH 043	450V	-20%	BC	CASE_A03
C8	DE0707391K	390pF	Hi_voltage	2000V	10%	muRata	CER3_1
C10	2222-591-16624	5.6nF	12NC_update	50V	5%	PHYCOMP	C1206
C12	2238-911-15656	330nF	X7R	25V	10%	PHYCOMP	C1206
C13	2222-911-16654	220nF	12NC_update	25V	10%	PHYCOMP	C1206
C14	2222-861-12101	100pF	12NC_update	50V	5%	PHYCOMP	C0805
C15	2222-911-16656	330nF	12NC_update	25V	10%	PHYCOMP	C1206
C17	2222-370-41682	6.8nF	MKT 370	250V	10%	BC	C370_A
C19	2222-590-16637	56nF	12NC_update	50V	10%	PHYCOMP	C0805
C20	2222-379-54683	68nF	MKP 379	400V	5%	BC	C_B5_L17.5_P15mm
C22	2222-376-82822	8.2nF	KP/MMKP 376	1600V	5%	BC	C_B7_L26_P22mm5
C23	2222-370-41104	100nF	MKT 370	250V	10%	BC	C370_D
C24	2222-370-41104	100nF	MKT 370	250V	10%	BC	C370_D
D1	9338-123-60115	BYD77D	Rectifier			PHILIPS	SOD87
D3	9337-534-10153	Voltage Regulator	BZD23C	12V		PHILIPS	SOD81
D4	9338-123-60115	BYD77D	Rectifier			PHILIPS	SOD87
F1	2412-086-28238	1A	SLOW			PHILIPS	GLAS_HOLDER
IC1	PN-UBA2014/N1A	UBA2014/N1A	IC_Universal			PHILIPS	SOT109
L1	3128-138-34871	LAMP_COIL	Coil	1.9mH		PHILIPS	LAMP_coil
P1	2422-015-19387	SCREW_CON_2P	SINGLE_ARRAY			MAG45	SCREW_CON_2P
P4	2422-015-19387	SCREW_CON_2P	SINGLE_ARRAY			MAG45	SCREW_CON_2P
P5	2422-015-19387	SCREW_CON_2P	SINGLE_ARRAY			MAG45	SCREW_CON_2P
R1	2322-193-13105	1M	PR01		5%	BC	PR01
R2	2322-734-68202	8.2k	RC12H		1%	PHYCOMP	R0805
R3	2322-711-61224	220k	RC01		5%	PHYCOMP	R1206
R4	3314J-1M	1M	Typ3314		-0.2	BOURNS	3314J
R5	2322-730-61103	10k	RC11		5%	PHYCOMP	R0805
R8	2322-711-61822	8.2k	RC01		5%	PHYCOMP	R1206
R9	2322-730-61479	47	RC11		5%	PHYCOMP	R0805
R10	2322-193-13105	1M	PR01		5%	BC	PR01
R12	2322-734-63303	33k	RC12H		1%	PHYCOMP	R0805
R13	2322-734-61501	150	RC12H		1%	PHYCOMP	R0805
R14	2322-156-11008	1	MRS25		1%	BC	MRS25
R16	2322-156-11508	1.5	MRS25		1%	BC	MRS25
R17	2322-711-91032	0	RC01		5%	PHYCOMP	R1206
R18	2322-193-13184	180k	PR01		5%	BC	PR01
R20	2322-730-61224	220k	RC11		5%	PHYCOMP	R0805
TP2	2422-034-15068	SOLDER-PIN_small	-			PHILIPS	SOLDER_PIN_small
TP3	2422-034-15068	SOLDER-PIN_small	-			PHILIPS	SOLDER_PIN_small
TP5	2422-034-15068	SOLDER-PIN_small	-			PHILIPS	SOLDER_PIN_small
TP6	2422-034-15068	SOLDER-PIN_small	-			PHILIPS	SOLDER_PIN_small
TP7	2422-034-15068	SOLDER-PIN_small	-			PHILIPS	SOLDER_PIN_small
TP12	2422-034-15068	SOLDER-PIN_small	-			PHILIPS	SOLDER_PIN_small
TP13	2422-034-15068	SOLDER-PIN_small	-			PHILIPS	SOLDER_PIN_small
TP16	2422-034-15068	SOLDER-PIN_small	-			PHILIPS	SOLDER_PIN_small
TR1		IRF820	fets			INT. RECT.	TO220
TR2		IRF820	fets			INT. RECT.	TO220

Figure 3

6. LAMP CIRCUIT OPERATION AND DIMENSIONING

In this chapter a description will be given how the lamp circuit for a 36W TLD lamp can be dimensioned. It is assumed that the supply of 400V is constant and that typical working frequency is equal to 45kHz. As the lamp voltage and lamp current of the 36W TLD lamp are known, ballast coil (L1 = 1.9mH) is determined.

The minimum frequency is determined by R12 and C14 which results in: fmin = 1.2 x 10^{-2} x R12 x C14 = 40kHz. As a result the maximum frequency is equal to: fmax = 2.5 x fmin = 100kHz. During the start-up phase the working frequency starts at the maximum frequency. As the load on the Half Bridge circuit consists of the series connected LC circuit, this is a safe frequency at which currents and voltages are low. To obtain a long lifetime and an efficient ignition of the lamp, the electrodes must be preheated. During the preheating phase the preheat timer determines the preheating time: Tpre = 1.7 x 10^{-4} x R12 x C12. The preheating current, which is flowing through the electrodes and lamp capacitor C22, is controlled by the preheat current sensor circuit (PCS) and is determined by R14, R13 and R9. As the lamp voltage should not exceed during this phase a certain maximum value, C22 (= 8.2nF) is determined.

During the ignition phase the working frequency is decreased due to the charging of C13 by an internally fixed current. During this continuously decrease in frequency, the circuit approaches the resonance frequency of the load (L1 and C22). The ignition voltage of the lamp is designed above the Vlafail level. If the lamp voltage passes the Vlafail level the ignition timer is started. If the preheating of the electrodes was correct, the increasing voltage across the lamp will ignite it. The frequency will further decrease until the minimum frequency is reached. Then it is assumed that the lamp is ignited and the Burn state begins. If however at the end of the ignition time the lamp voltage still exceeds the lamp fail level (Vla>Vlafail), then it is assumed that the lamp is not ignited and the IC will be switched in the Power Down state.

During the ignition of the lamp and the Burn phase the Capacitive Mode protection (ACM) ensures a safe operation of the Power MosFets. The ignition voltage increases however with the ageing of the lamp. To avoid overload of the key components, the maximum ignition voltage (Vlampmax) is limited and controlled by the lamp voltage sensor (LVS) circuit (pin 13). The maximum ignition time, in which the lamp should ignite, is determined by Tign = 3.1 x 10^{-5} x R 12 x C12.

In the Burn state the average current sensor circuit (ACS) of the UBA2014 controls the lamp current. As the system efficiency is high, the lamp power (Pla) is almost equal to input power . As the 400V-supply voltage is constant, Pla can be kept constant by controlling the averaged voltage across resistor R14. In this way the lamp current is controlled. Dimming is performed by changing the reference level at the CS+ pin (pin 15) by turning potentiometer R4. In this way the input voltage of the voltage controlled oscillator regulates the frequency and herewith the lamp current.

The start-up current for the UBA2014 is derived from the 400V via R1, R10 and one of the lamp electrodes. If the lamp is not present, the IC will not start-up. As soon as VDD_{high} is exceeded the IC starts oscillating. The HB voltage together with dv/dt capacitors behave like a current source, which supplies not only the IC and the gates of the MosFets but generates also a stable 12V supply.

For more information about HF driving the 36W T8 lamp see IEC60081 sheet 7420. It can be found on web site: pww.standardisation.philips.com

IEC

TC34

SC34A

7. QUICK MEASUREMENTS

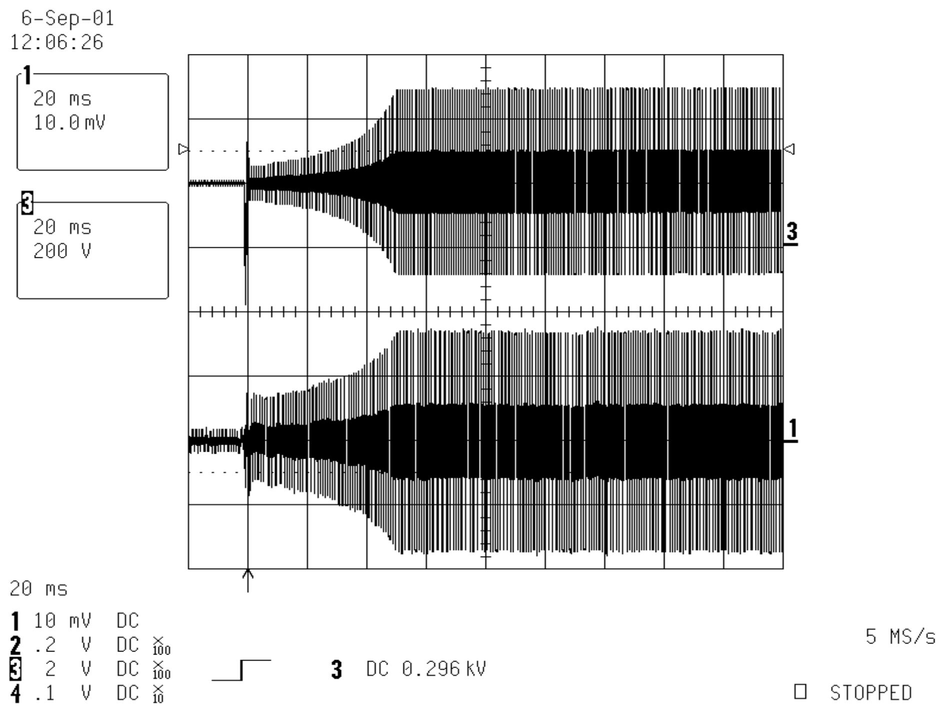

Figure 4: Ielectrode (1) and Ulamp (3) during start-up and preheat phase

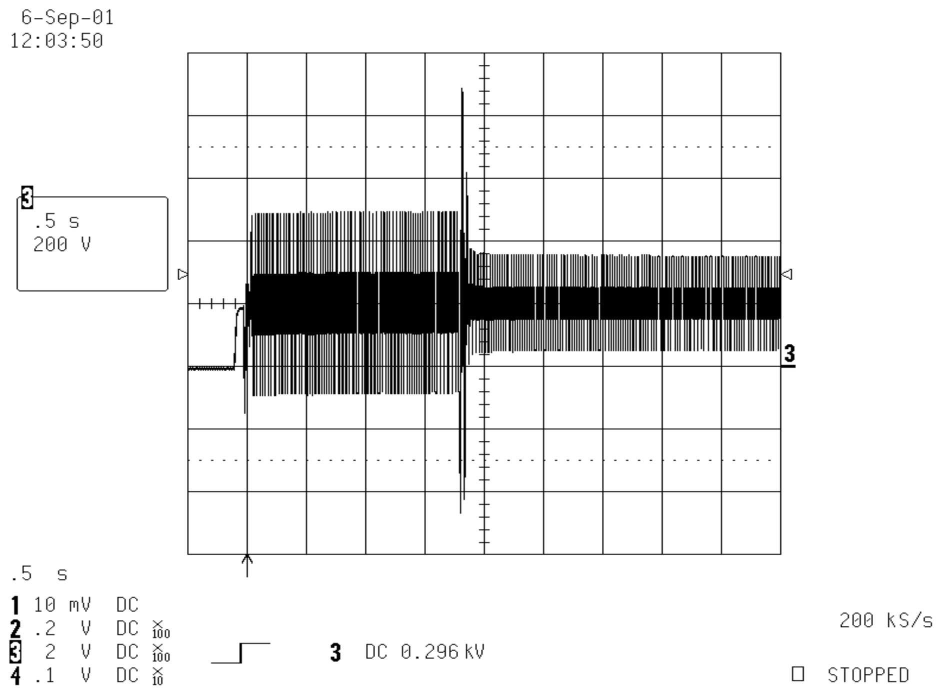

Figure 5: Ulamp during the preheat, ignition and burn phase

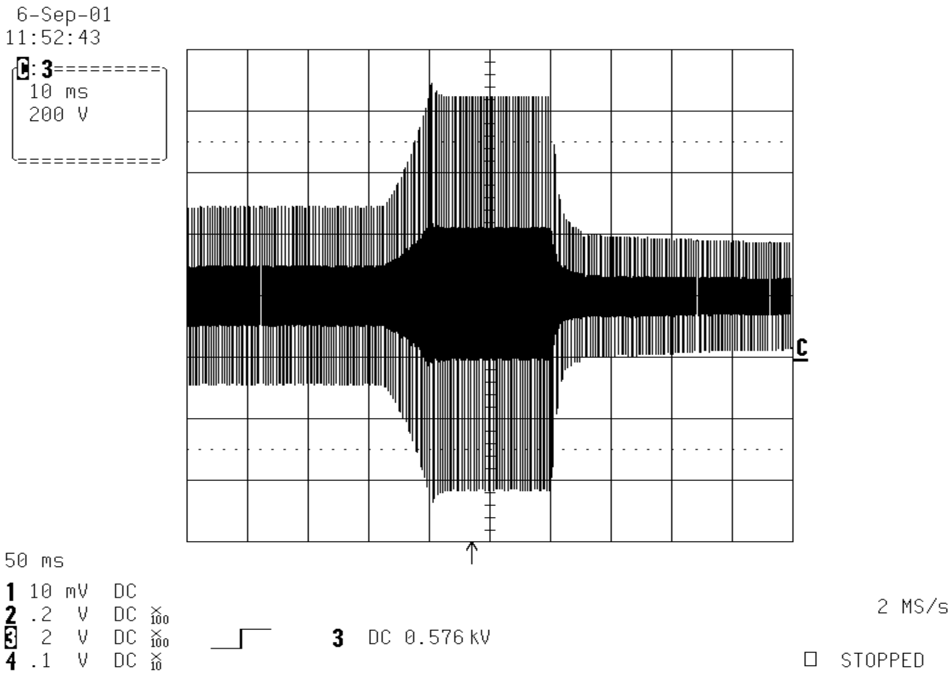

Figure 6: Ulamp during the ignition phase. The lamp voltage is controlled at the calculated Vlamax level. After 20ms the lamp ignites and we see the transition to the Burn phase. If the lamp would be not ignited at the end of the ignition time, than the IC would be switched in the Power Down state.