

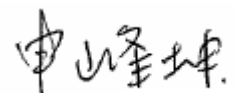
Version :1.0**TECHNICAL SPECIFICATION****MODEL NO. : PD032VX1**

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Prepared By _____

Revision History

Rev.	Issued Date	Revised Contents
0.1	Dec. 25, 2008	Preliminary
1.0	Apr. 08, 2009	New

TECHNICAL SPECIFICATION

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1. Application

This data sheet applies to a color TFT LCD module, PD032VX1. The module applies to OA product, GPS, which require high quality flat panel display. If you must use in high reliability environment can't over reliability test condition. If you use PD032VX1, Prime View advises your system sides must use PVI-2003A which one generates signal to control PD032VX1

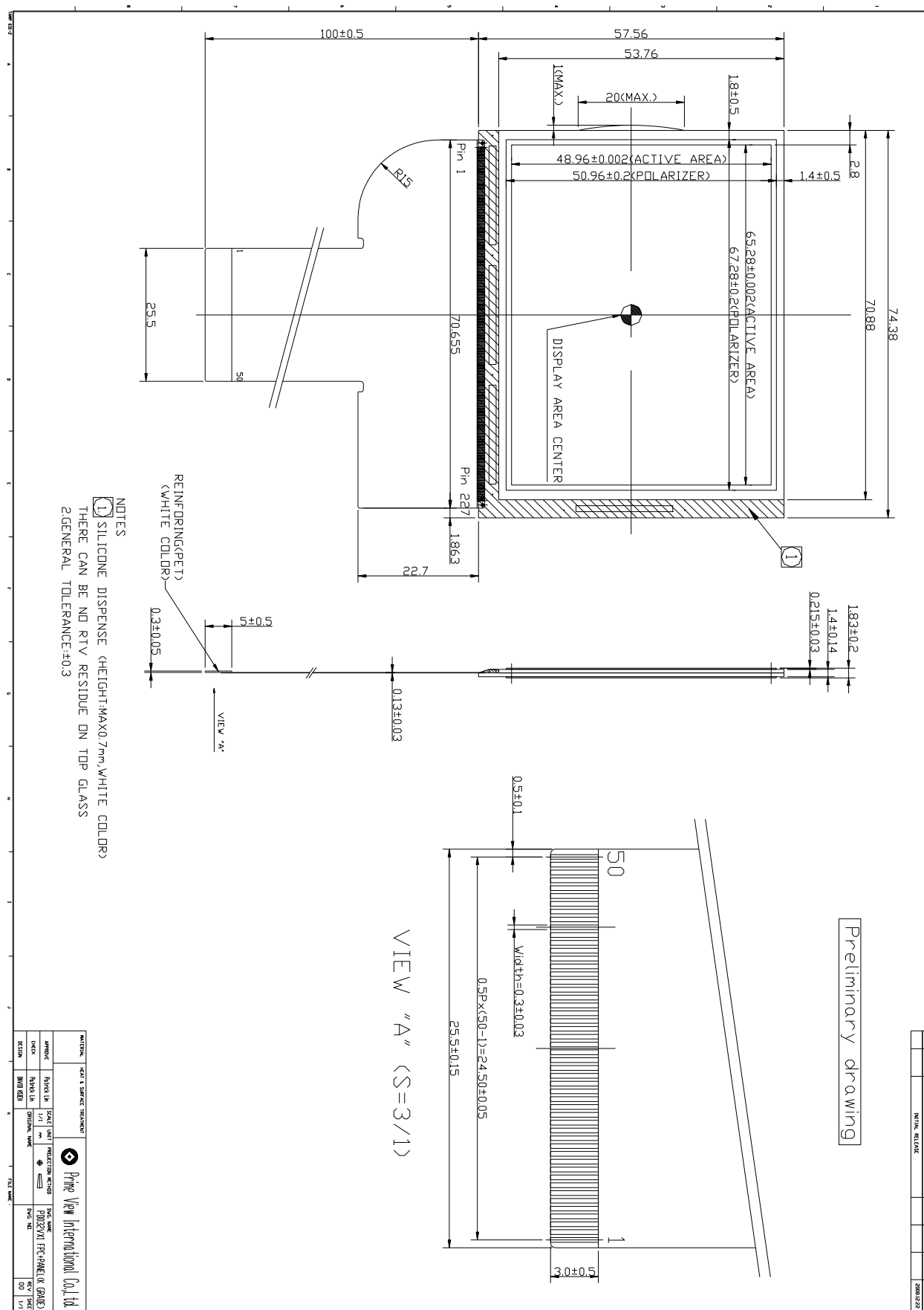
2. Features

- . Amorphous silicon TFT LCD panel
- . Pixel in stripe configuration
- . Display Colors : 262,144 colors
- . TTL transmission interface
- . Optimum Viewing Direction : 6 o'clock

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	3.2(diagonal)	inch
Display Format	640×(R, G, B)×480	dot
Display Colors	262,144	
Active Area	65.28(H)×48.96(V)	mm
Pixel Pitch	0.102(H)×0.102(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	74.38(W)×57.56 (H)×1.83 (typ.) (D)	mm
Weight	18±2	g
Surface treatment	Normal	
Display mode	Normally White	
Gray scale inversion direction	6 o'clock [ref to Note13-1]	

4. Mechanical Drawing of TFT-LCD Module



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5. Input / Output Terminals

TFT-LCD Panel Driving

Pin No.	Symbol	I/O	Function	Remark
1	DIO1	I/O	Horizontal Start Pulse Signal Input or Output 1	Note5-3
2	VSS2	I	Ground	
3	VDD1	I	Power Supply	
4	CLK	I	Horizontal Shift Clock	
5	R/L	I	Left/Right Selection	Note 5-3
6	R0	I	Red Data (LSB)	
7	R1	I	Red Data	
8	R2	I	Red Data	
9	R3	I	Red Data	
10	R4	I	Red Data	
11	R5	I	Red Data (MSB)	
12	VSS2	I	Ground	
13	G0	I	Green Data (LSB)	
14	G1	I	Green Data	
15	G2	I	Green Data	
16	G3	I	Green Data	
17	G4	I	Green Data	
18	G5	I	Green Data (MSB)	
19	B0	I	Blue Data (LSB)	
20	B1	I	Blue Data	
21	B2	I	Blue Data	
22	B3	I	Blue Data	
23	B4	I	Blue Data	
24	B5	I	Blue Data (MSB)	
25	LD	I	Load output signal	Note5-7
26	REV	I	Data invert control	Note5-8
27	POL	I	Polarity selection	Note5-9
28	DIO2	I/O	Horizontal Start Pulse Signal Input or Output	Note5-3
29	VSS2	I	Ground	
30	V3	I	Gamma Voltage 3	Note5-10
31	V5	I	Gamma Voltage 5	Note5-10
32	V7	I	Gamma Voltage 7	Note5-10
33	V8	I	Gamma Voltage 8	Note5-10
34	V10	I	Gamma Voltage 10	Note5-10
35	V12	I	Gamma Voltage 12	Note5-10
36	VSS2	I	Ground	
37	VDD2	I	Voltage for analog circuit	Note5-10
38	VCOM	I	Common Voltage	
39	OE	I	Output Enable	Note5-5
40	U/D	I	Up/Down Selection	Note5-6
41	CKV	I	Vertical Shift Clock	Note5-4
42	STVU	I/O	Vertical Shift Pulse Signal Input or Output	Note5-6
43	STVD	I/O	Vertical Shift Pulse Signal Input or Output	Note5-6
44	VGG	I	Gate On Voltage	Note5-1
45	VSS1	I	Ground	
46	VCC	I	Voltage for logic circuit	
47	VEE	I	Gate Off Voltage	Note5-2
48	DUMMY	-	No connect	
49	DUMMY	-	No connect	
50	DUMMY	-	No connect	

Note 5-1 : $V_{GG}=17.4V$

Note 5-2 : $V_{EE}=-6.0V$

Note 5-3 : Select left or right shift

R/L	DIO1	DIO2	Shift
1	Input	Hi-Z	Left to right
0	Hi-Z	Input	Right to left

Note 5-4 : Gate driver shift clock

Note 5-5 : When OE is connected to high “1”, the driver outputs are disabled (Gate output = V_{EE}).
Under this condition, the operation of registers will not be affected.

Note 5-6 : Select up or down shift

U/D	STVU	STVD	Shift
1	Hi-Z	Input	Down to Up
0	Input	Hi-Z	Up to Down

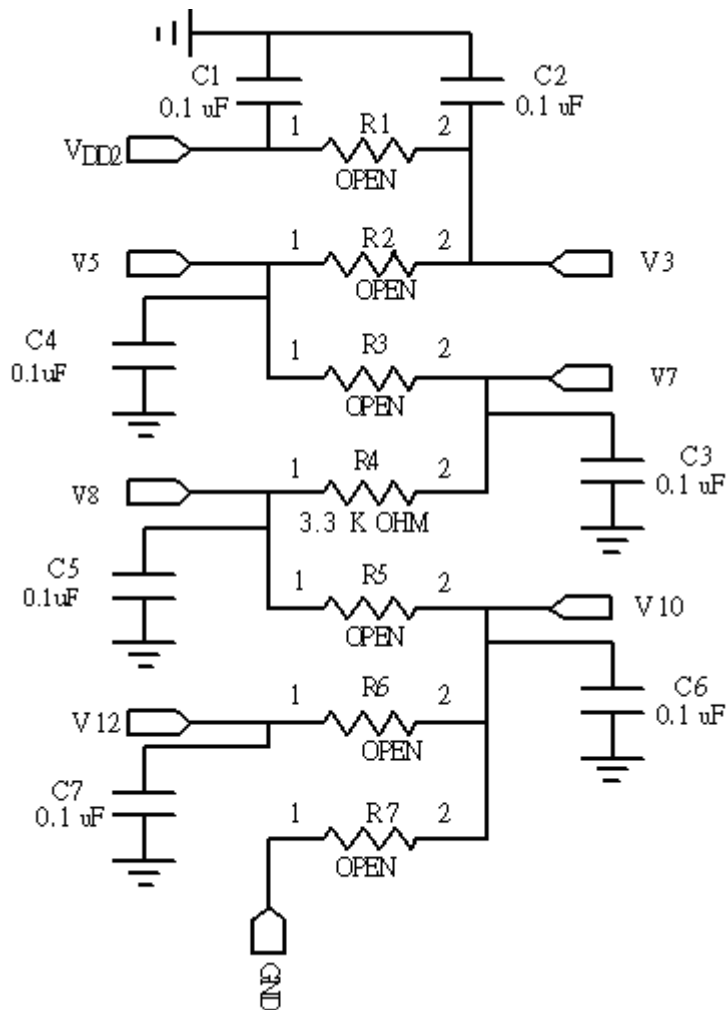
Note 5-7 : Latch the polarity of outputs and switch the new data to outputs
At the rising edge (LD), latch the “POL” signal to control the polarity of the outputs.

Note 5-8 : Control whether the Data R0~G5 are inverted or not. (PVI suggests connecting to GND)
When “REV=1”, these data will be inverted.
EX: “00”→”3F”, “07”→”38”, “15”→”2A”

Note 5-9 : Polarity selector for dot-inversion control. Available at the rising edge of LD.
When POL=1 : Even outputs range from V1~V7, and Odd outputs range from V8~V14.
When POL=0 : Even outputs range from V8~V14, and Odd outputs range from V1~V7.

Note 5-10 : $V_{DD2} = 10.6V$

Typical Application Circuit :



6. Absolute Maximum Ratings :

 $V_{SS1}=V_{SS2}=GND=0V, T_a=25^{\circ}C$

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	V_{DD1}	-0.5	5.0	V	
	V_{CC}	-0.3	6.0	V	
	V_{DD2}	-0.5	13.5	V	
	V_{GG}	-0.3	40.0	V	
	$V_{GG}-V_{EE}$	-	40.0	V	
	V_{EE}	-20	0.3	V	
Operating Temperature	Top	-20	70	$^{\circ}C$	
Storage Temperature	Tst	-30	80	$^{\circ}C$	

7. Electrical Characteristics

7-1) Recommended Operating Conditions

 $V_{SS1}=V_{SS2}=GND = 0V, T_a = 25^{\circ}C$

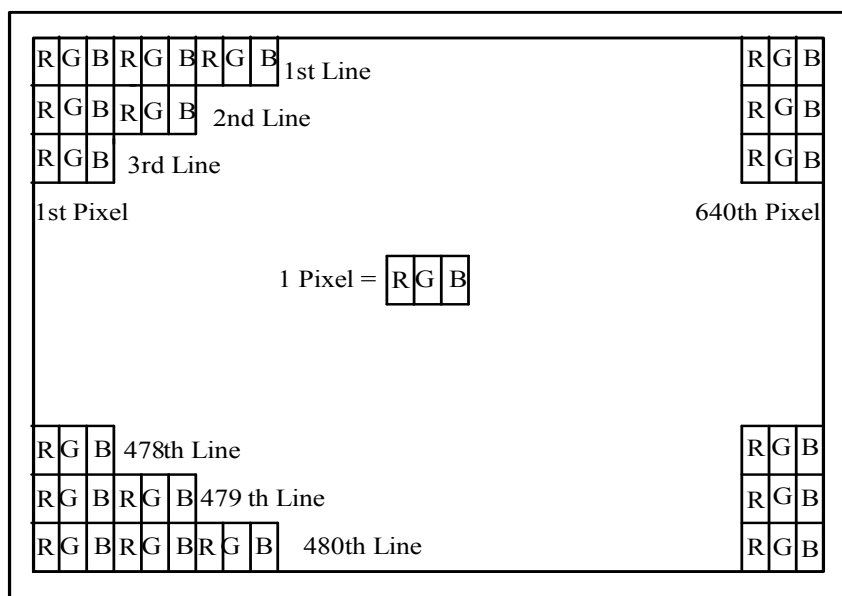
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	V_{DD1}	3.0	3.3	3.6	V	
	V_{DD2}	-	10.6	-		
Supply Voltage for Gate Driver	V_{GG}	-	17.4	-	V	
	V_{EE}	-	-6.0	-	V	
	V_{CC}	3.0	3.3	3.6	V	
Supply Voltage for Vcom	V_{com}	-	3.1	-	V	
Digital Input Voltage	V_{IH}	$0.8V_{DD1}$	-	V_{DD1}	V	
	V_{IL}	0	-	$0.2V_{DD1}$	V	

7-2) Power Consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	I_{GG}	$V_{GG}=17.4V$	0.10	0.30	mA	
Supply Current for Gate Driver (Low level)	I_{EE}	$V_{EE}=-6.0V$	0.10	0.30	mA	
Supply Current for Source Driver (Digital)	I_{DD1}	$V_{DD1}=3.3V$	4.39	8.78	mA	
Supply Current for Source Driver (Analog)	I_{DD2}	$V_{DD2}=10.6V$	29.30	58.60	mA	
Supply Current for Gate Driver (Digital)	I_{CC}	$V_{CC}=3.3V$	0.10	0.30	mA	
LCD Panel Power Consumption	-	-	327.7	491.6	mW	

8. Pixel Arrangement

The LCD module pixel arrangement is the stripe.

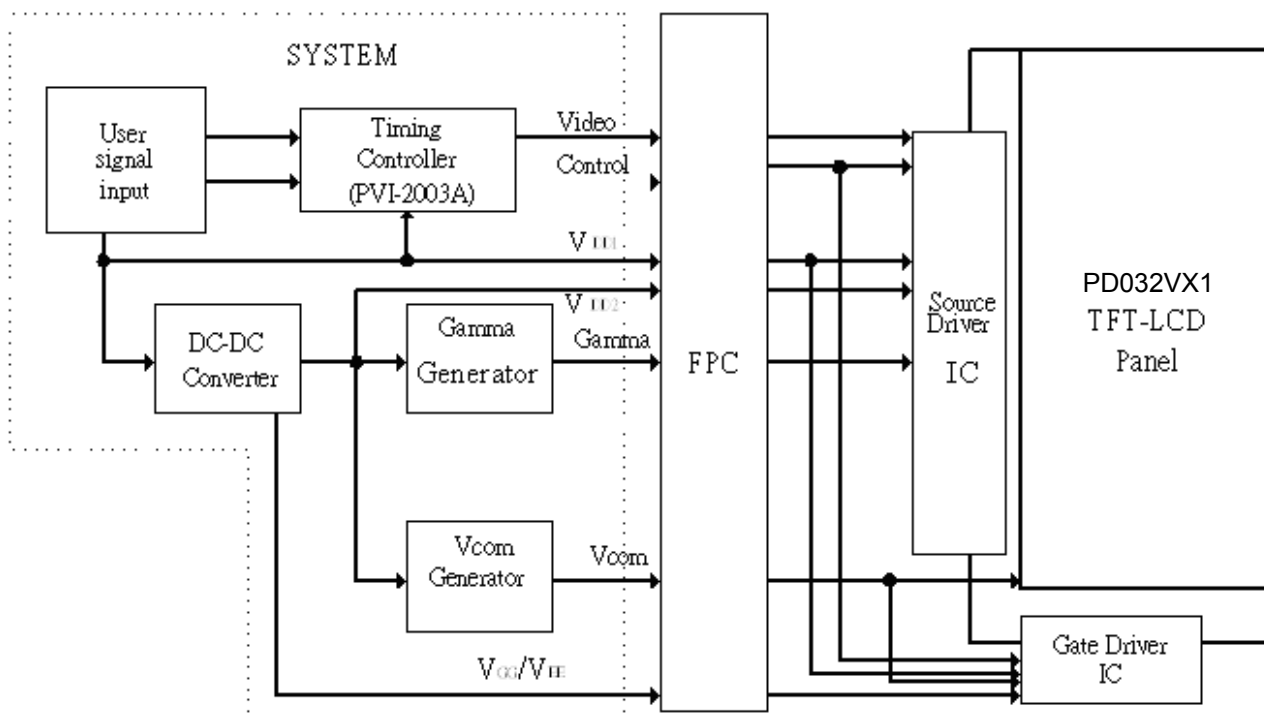


9. Display Color and Gray Scale Reference

Color		Input Color Data																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

10. Block Diagram

10-1) TFT-module Block Diagram



If you use PD032VX1, you must apply PVI-2003A(Timing controller) which Will generate signal to support PD032VX1.

11. Interface Timing

11.1) Timing Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency	Fclk	-	25	40	MHz
CLK Pulse Width	T _{CPH}	25	40	-	ns
Data Set-up Time	T _{su}	4	-	-	ns
Data Hold Time	T _{hd}	2	-	-	ns
Propagation Delay of DIO2/1	T _{phl}	6	10	15	ns
Time That The Last Data to LD	T _{ld}	1	-	-	T _{CPH}
Pulse width of LD	T _{wld}	2	-	-	T _{CPH}
Time That LD to DIO1/2	T _{lds}	5	-	-	T _{CPH}
POL Set-up Time	T _{psu}	6	-	-	ns
POL Hold Time	T _{phd}	6	-	-	ns
OE Pulse Width	T _{OE_V}	1	-	-	μs
CKV Pulse Width	T _{CKV}	500	-	-	ns
STV Set-up Time	T _{SUV}	400	-	-	ns
STV Hold Time	T _{HDV}	400	-	-	ns
Horizontal Display Period	T _{HDP}	-	640	-	T _{CPH}
Horizontal Period Timing Range	T _{HP}	-	800	-	T _{CPH}
Horizontal Lines Per Field	T _V	520	525	640	T _{HP}
Vertical Display Timing Range	T _{DV}	-	480	-	T _{HP}

11.2) Timing Diagram

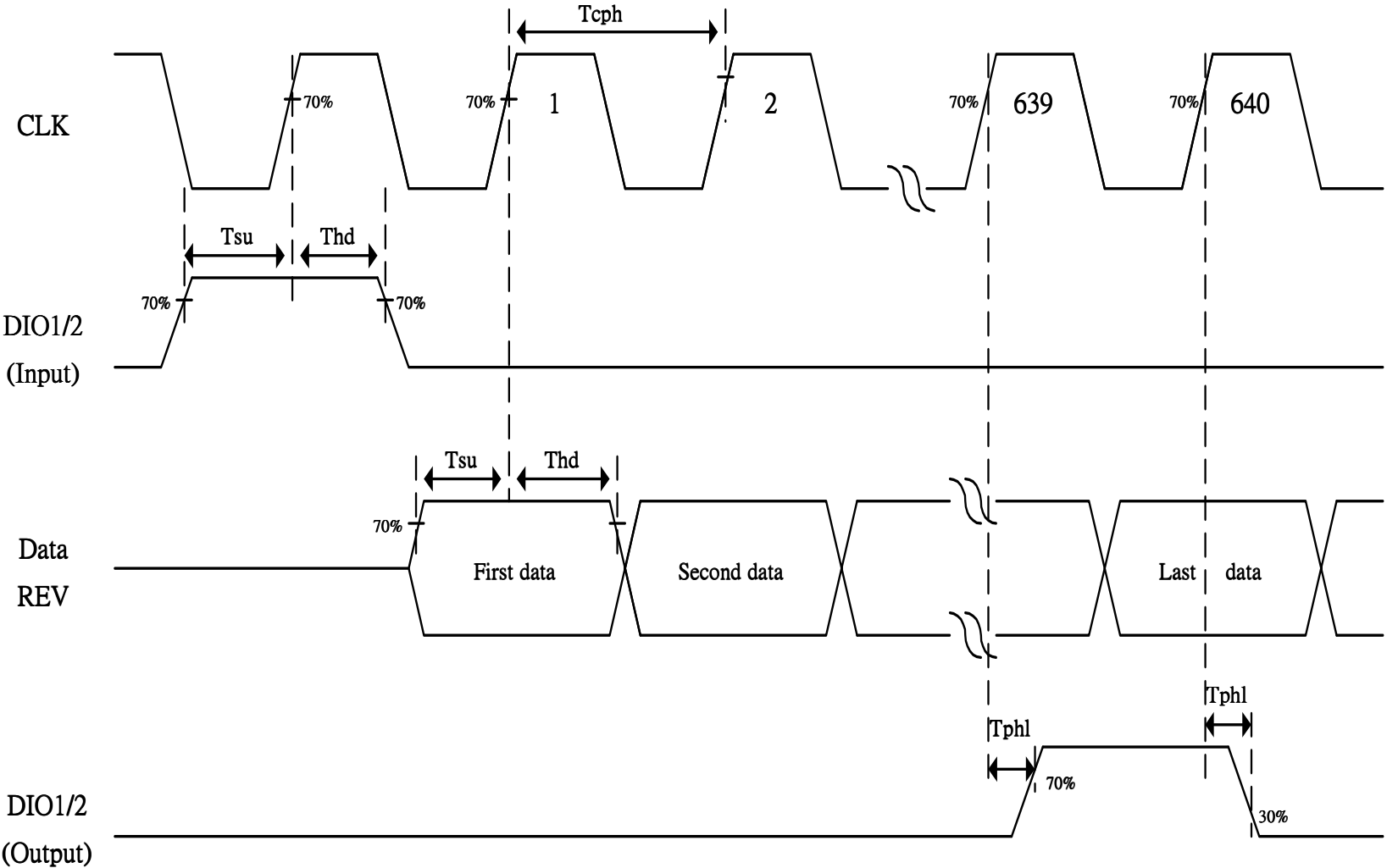


Fig. 11-1 Horizontal timing(1)

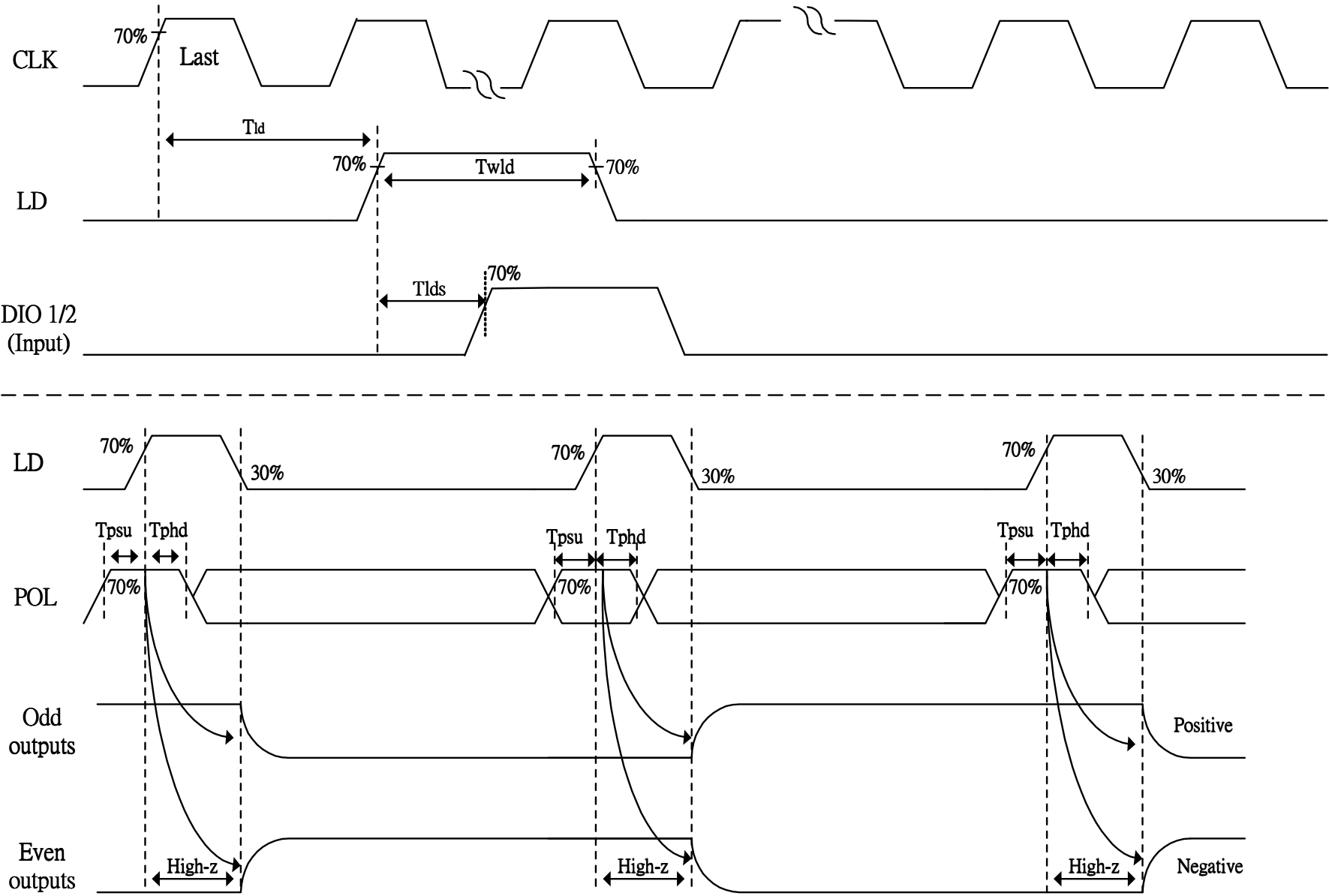


Fig. 11-2 Horizontal timing(2)

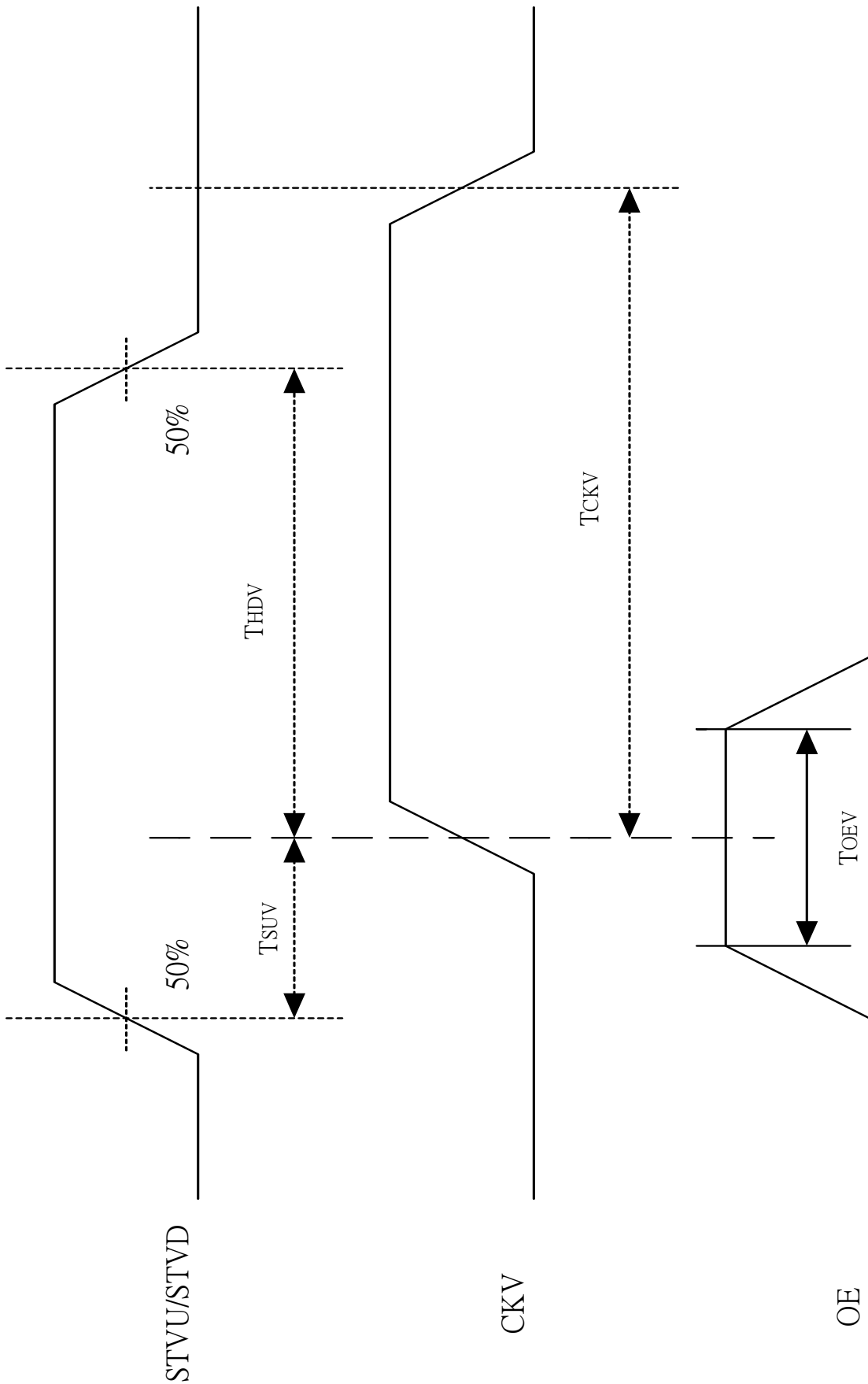


Fig. 11-3 Vertical shift clock timing

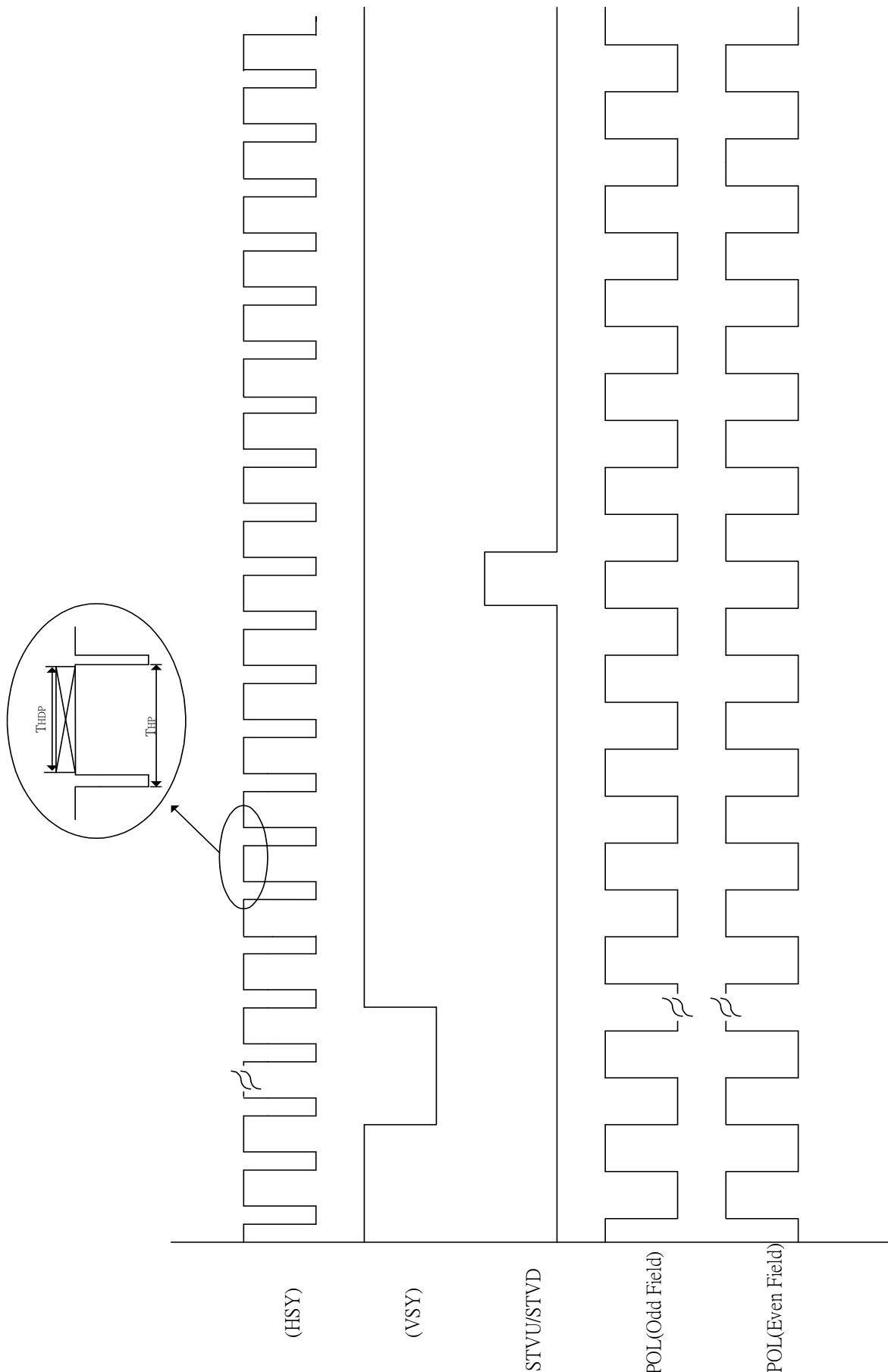
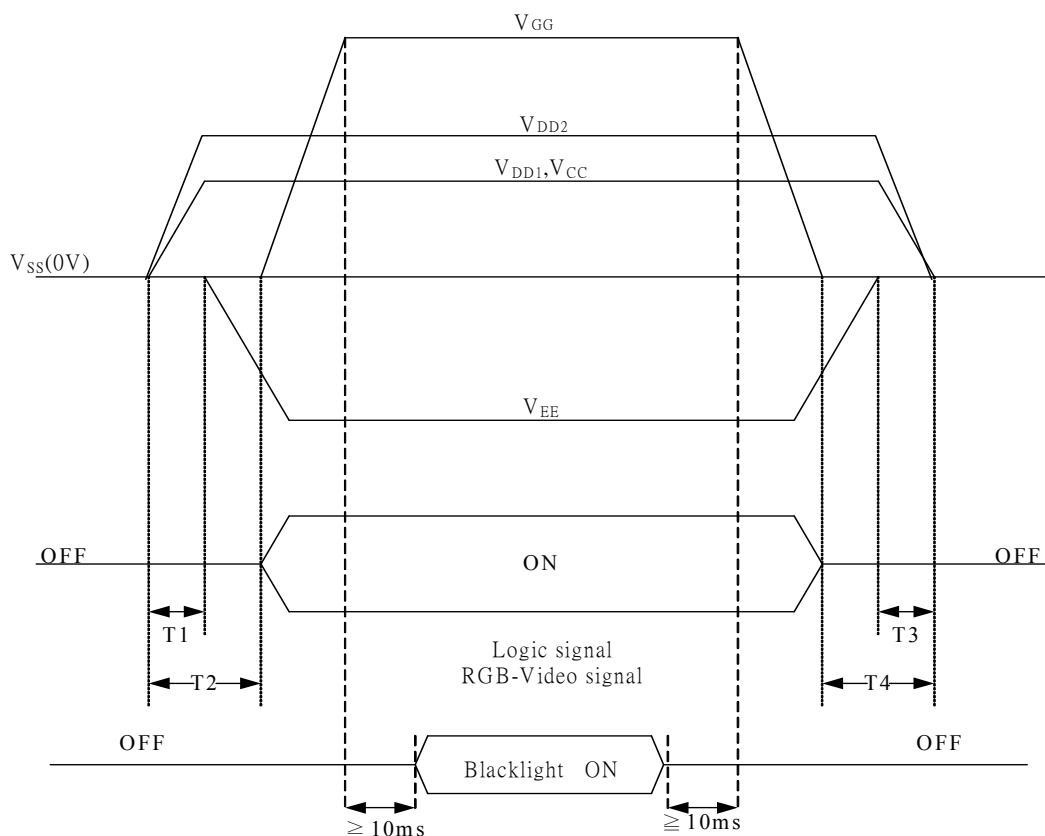


Fig. 11-4 Vertical timing

12. Power On Sequence



- 1) $10ms \leq T1 < T2$
- 2) $0ms < T3 \leq T4 \leq 10ms$

13. Optical Characteristics

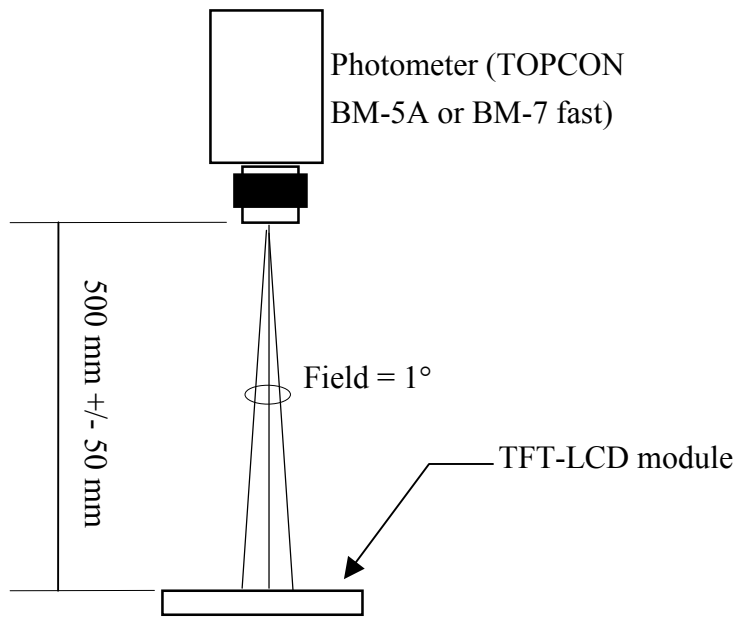
13-1) Specification :

The backlight which PVI used is CCFL for optical measuring and the specification of average brightness is $5500(cd/m^2)$.

$T_a=25^{\circ}C$

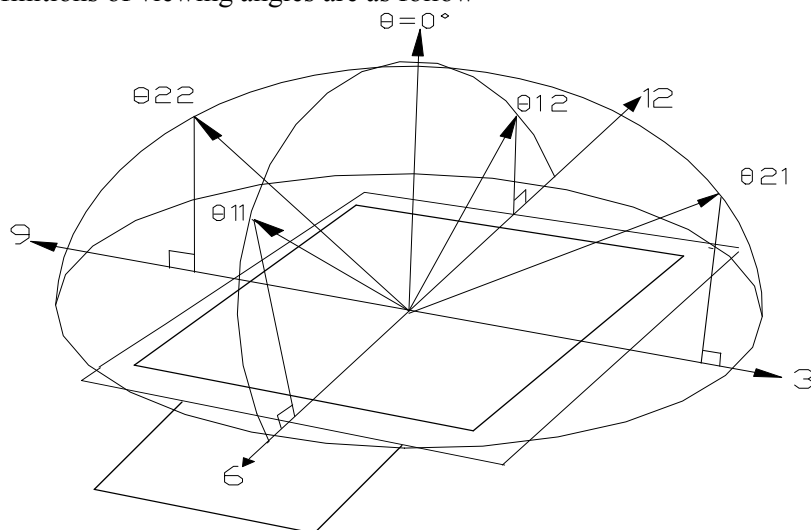
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	$\theta 21, \theta 22$	45	50	-	deg	Note 13-1
	Vertical	$\theta 12$ (to 12 o'clock)	10	15	-	deg	
		$\theta 11$ (to 6 o'clock)	30	35	-	deg	
Contrast Ratio	CR	At optimized Viewing angle	200	400	-	-	Note 13-3
Response time	Rise	$\theta = 0^{\circ}$	-	15	30	ms	Note 13-2
	Fall		-	25	50	ms	
Transmission ratio	T	$\theta = 0^{\circ}$	6.3	6.8	-	-	-
White Chromaticity	x	$\theta = 0^{\circ}$	0.27	0.30	0.33		Note 13-1
	y		0.32	0.35	0.38		

All the optical measurement shall be executed 30 minute after backlight being turn-on. The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.

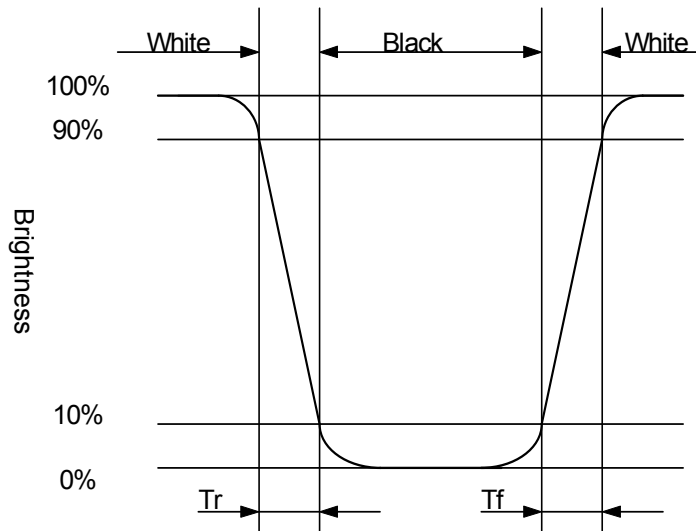


Optical characteristics measuring configuration

Note 13-1 : The definitions of viewing angles are as follow



Note 13-2 : Definition of Response Time T_r and T_f



Note 13-3 : The definition of contrast ratio $CR = \frac{\text{Luminance at White Pattern}}{\text{Luminance at Black Pattern}}$

14. Handling Cautions**14-1) Mounting of module**

- a) Please power off the module when you connect the input/output connector.
- b) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- c) Protective film (Laminator) is applied on surface to protect it against scratches and dirt.
- d) Please following the tear off direction as figure14-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.

14-2) Precautions in mounting

- a) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- b) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- c) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

14-3) Others

- a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- b) Store the module at a room temperature place.
- a) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- b) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- c) Observe all other precautionary requirements in handling general electronic components.
- d) Please adjust the voltage of common electrode as material of attachment by 1 module.

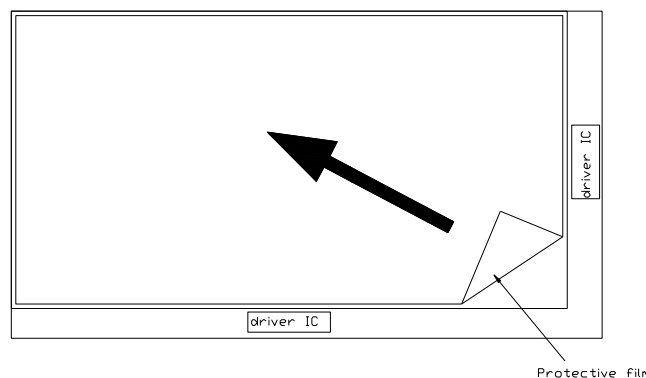


Figure 14-1 the way to peel off protective film

15. Reliability Test

No	Test Item	Test Condition	Remark
1	High Temperature Storage Test	Ta = +80°C, 240 hrs	
2	Low Temperature Storage Test	Ta = -30°C, 240 hrs	
3	High Temperature Operation Test	Ta = +70°C, 240 hrs	
4	Low Temperature Operation Test	Ta = -20°C, 240 hrs	
5	High Temperature & High Humidity Operation Test	Ta = +60°C, 90%RH, 240 hrs (No Condensation)	
6	Thermal Cycling Test (non-operating)	-20°C → +70°C, 200 Cycles (30min – 30min)	
7	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal	

Ta : ambient temperature

Note : The protective film must be removed before temperature test.

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image).All the cosmetic specification is judged before the reliability stress.

16. Packing Diagram

