# CPU Supervisor with 4K SPI EEPROM

## FEATURES

- **Selectable time out watchdog timer**
- **Low $V_{CC}$ detection and reset assertion**
  - **Five standard reset threshold voltages**
  - **Re-program low $V_{CC}$ reset threshold voltage using special programming sequence.**
  - **Reset signal valid to $V_{CC}$ = 1V**
- **Long battery life with low power consumption**
  - **<50µA max standby current, watchdog on**
  - **<10µA max standby current, watchdog off**
  - **<2mA max active current during read**
- **2.7V to 5.5V and 4.5V to 5.5V power supply versions**
- **4Kbits of EEPROM–1M write cycle endurance**
- **Save critical data with Block Lock™ memory**
  - **Protect 1/4, 1/2, all or none of EEPROM array**
- **Built-in inadvertent write protection**
  - **Write enable latch**
  - **Write protect pin**
- **3.3MHz clock rate**
- **Minimize programming time**
  - **16-byte page write mode**
  - **Self-timed write cycle**
  - **5ms write cycle time (typical)**
- **SPI modes (0,0 & 1,1)**
- **Available packages**
  - **8-lead MSOP, 8-lead SOIC, 8-pin PDIP**
  - **14-lead TSSOP**

## DESCRIPTION

These devices combine four popular functions, Power-on Reset Control, Watchdog Timer, Supply Voltage Supervision, and Block Lock Protect Serial EEPROM Memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying power to the device activates the power on reset circuit which holds $\overline{\text{RESET}}$/RESET active for a period of time. This allows the power supply and oscillator to stabilize before the processor executes code.

The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{\text{RESET}}$/RESET signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The device's low $V_{CC}$ detection circuitry protects the user's system from low voltage conditions, resetting the system when $V_{CC}$ falls below the minimum $V_{CC}$ trip point. $\overline{\text{RESET}}$/RESET is asserted until $V_{CC}$ returns to proper operating level and stabilizes. Five industry standard $V_{TRIP}$ thresholds are available, however, Xicor's unique circuits allow the threshold to be reprogrammed to meet custom requirements or to fine-tune the threshold for applications requiring higher precision.
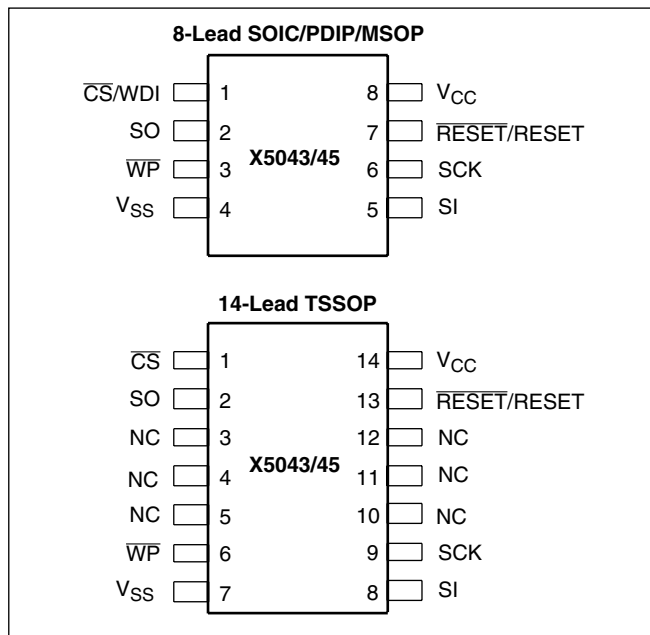
## BLOCK DIAGRAM
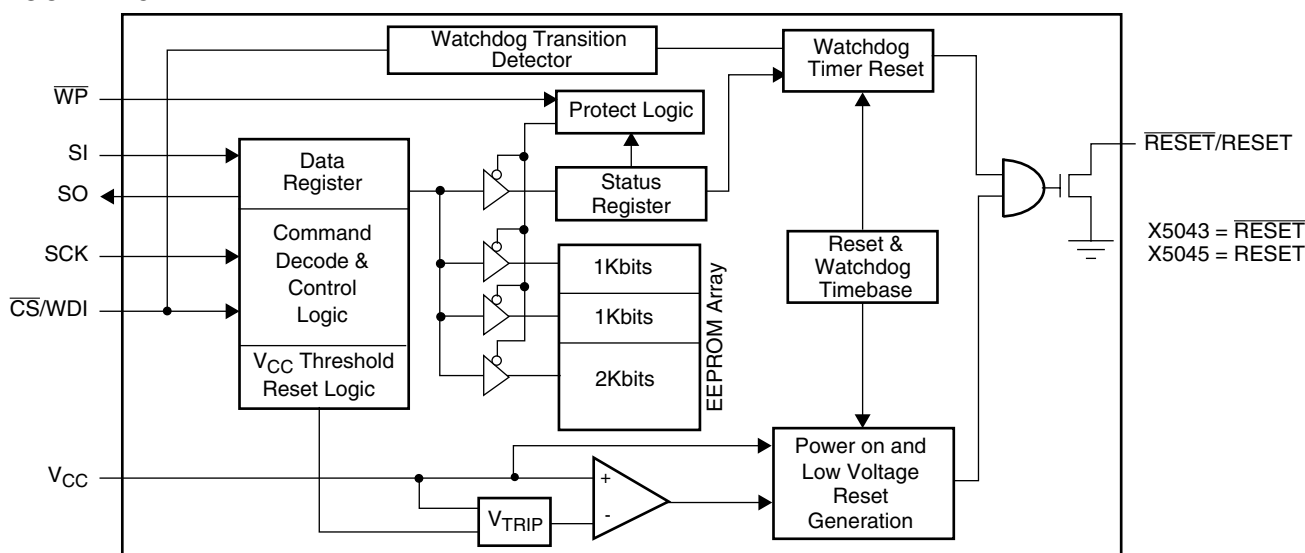
# X5043/X5045

The memory portion of the device is a CMOS Serial EEPROM array with Xicor's block lock protection. The array is internally organized as x 8. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 1,000,000 cycles and a minimum data retention of 100 years.

## PIN CONFIGURATION

**8-Lead SOIC/PDIP/MSOP**

```
$\overline{CS}$/WDI   1          8   V_CC
SO             2          7   $\overline{RESET}$/RESET
$\overline{WP}$      3  X5043/45  6   SCK
V_SS           4          5   SI
```

**14-Lead TSSOP**

```
$\overline{CS}$   1          14   V_CC
SO          2          13   $\overline{RESET}$/RESET
NC          3          12   NC
NC          4  X5043/45  11   NC
NC          5          10   NC
$\overline{WP}$   6           9   SCK
V_SS        7           8   SI
```

## PIN DESCRIPTIONS

### Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

### Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

### Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin is latched on the rising edge of the clock input, while data on the SO pin changes after the falling edge of the clock input.

## Chip Select ($\overline{CS}$)

When $\overline{CS}$ is high, the X5043/45 is deselected and the SO output pin is at high impedance and, unless an internal write operation is underway, the X5043/45 will be in the standby power mode. $\overline{CS}$ low enables the X5043/45, placing it in the active power mode. It should be noted that after power-up, a high to low transition on $\overline{CS}$ is required prior to the start of any operation.

## Write Protect ($\overline{WP}$)

When $\overline{WP}$ is low, nonvolatile writes to the X5043/45 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held high, all functions, including non volatile writes operate normally. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the X5043/45. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no affect on a write.

## Reset ($\overline{RESET}$, RESET)

X5043/45, $\overline{RESET}$/RESET is an active low/HIGH, open drain output which goes active whenever V_CC falls below the minimum V_CC sense level. It will remain active until V_CC rises above the minimum V_CC sense level for 200ms. $\overline{RESET}$/RESET also goes active if the Watchdog timer is enabled and $\overline{CS}$ remains either high or low longer than the Watchdog time out period. A falling edge of $\overline{CS}$ will reset the watchdog timer.

## PIN NAMES

| Symbol | Description |
|---|---|
| CS | Chip Select Input |
| SO | Serial Output |
| SI | Serial Input |
| SCK | Serial Clock Input |
| $\overline{WP}$ | Write Protect Input |
| V_SS | Ground |
| V_CC | Supply Voltage |
| $\overline{RESET}$/RESET | Reset Output |

## PRINCIPLES OF OPERATION

### Power On Reset

Application of power to the X5043/X5045 activates a Power On Reset Circuit. This circuit pulls the $\overline{RESET}$/RESET pin active. $\overline{RESET}$/RESET prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator. When $V_{CC}$ exceeds the device $V_{TRIP}$ value for 200ms (nominal) the circuit releases $\overline{RESET}$/RESET, allowing the processor to begin executing code.

### Low Voltage Monitoring

During operation, the X5043/X5045 monitors the $V_{CC}$ level and asserts $\overline{RESET}$/RESET if supply voltage falls below a preset minimum $V_{TRIP}$ The $\overline{RESET}$/RESET signal prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{RESET}$/RESET signal remains active until the voltage drops below 1V. It also remains active until $V_{CC}$ returns and exceeds $V_{TRIP}$ for 200ms.

### Watchdog Timer

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the WDI input. The microprocessor must toggle the $\overline{CS}$/WDI pin periodically to prevent an active $\overline{RESET}$/RESET signal. The $\overline{CS}$/WDI pin must be toggled from HIGH to LOW prior to the expiration of the watchdog time out period. The state of two nonvolatile control bits in the Status Register determines the watchdog timer period. The microprocessor can change these watchdog bits. With no microprocessor action, the watchdog timer control bits remain unchanged, even during total power failure.

### $V_{CC}$ Threshold Reset Procedure

The X5043/X5045 is shipped with a standard $V_{CC}$ threshold ($V_{TRIP}$) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard $V_{TRIP}$ is not exactly right, or if higher precision is needed in the $V_{TRIP}$ value, the X5043/X5045 threshold may be adjusted. The procedure is described below, and uses the application of a high voltage control signal.
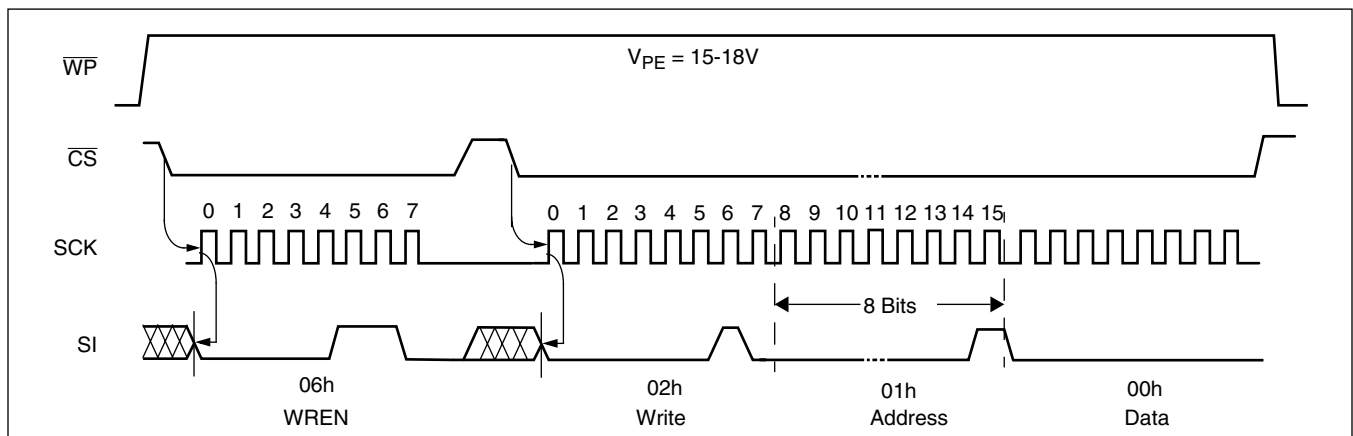
### Setting the $V_{TRIP}$ Voltage

This procedure is used to set the $V_{TRIP}$ to a higher voltage value. For example, if the current $V_{TRIP}$ is 4.4V and the new $V_{TRIP}$ is 4.6V, this procedure will directly make the change. If the new setting is to be lower than the current setting, then it is necessary to reset the trip point before setting the new value.

To set the new $V_{TRIP}$ voltage, apply the desired $V_{TRIP}$ threshold voltage to the $V_{CC}$ pin and tie the $\overline{WP}$ pin to the programming voltage $V_P$ Then send a WREN command, followed by a write of Data 00h to address 01h. $\overline{CS}$ going HIGH on the write operation initiates the $V_{TRIP}$ programming sequence. Bring $\overline{WP}$ LOW to complete the operation.

**Note:** This operation also writes 00h to array address 01h.

Figure 1. Set $V_{TRIP}$ Level Sequence ($V_{CC}$ = desired $V_{TRIP}$ value.)

# X5043/X5045

## Resetting the $V_{TRIP}$ Voltage

This procedure is used to set the $V_{TRIP}$ to a "native" voltage level. For example, if the current $V_{TRIP}$ is 4.4V and the new $V_{TRIP}$ must be 4.0V, then the $V_{TRIP}$ must be reset. When $V_{TRIP}$ is reset, the new $V_{TRIP}$ is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the $V_{TRIP}$ voltage, apply at least 3V to the $V_{CC}$ pin and tie the $\overline{WP}$ pin to the programming voltage $V_P$. Then send a WREN command, followed by a write of Data 00h to address 03h. $\overline{CS}$ going HIGH on the write operation initiates the $V_{TRIP}$ programming sequence. Bring $\overline{WP}$ LOW to complete the operation.

**Note:** This operation also writes 00h to array address 03h.

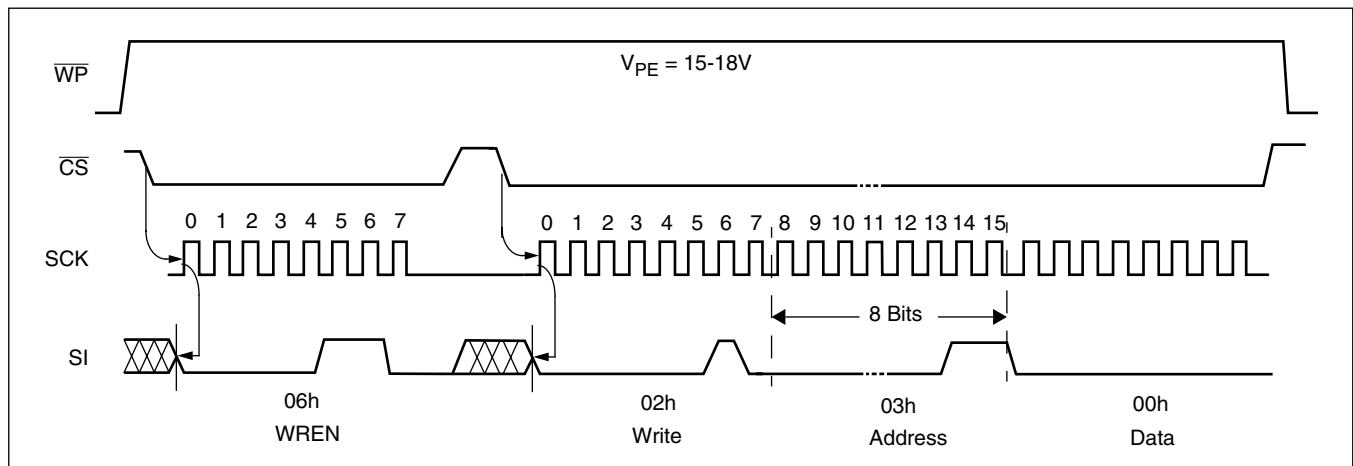**Figure 2. Reset $V_{TRIP}$ Level Sequence ($V_{CC}$ > 3V. $\overline{WP}$ = 15–18V)**
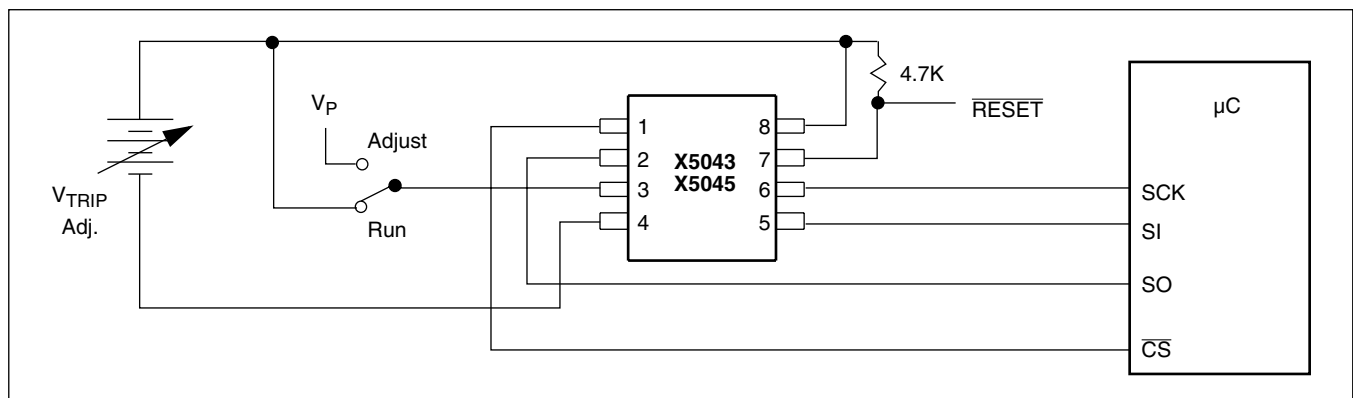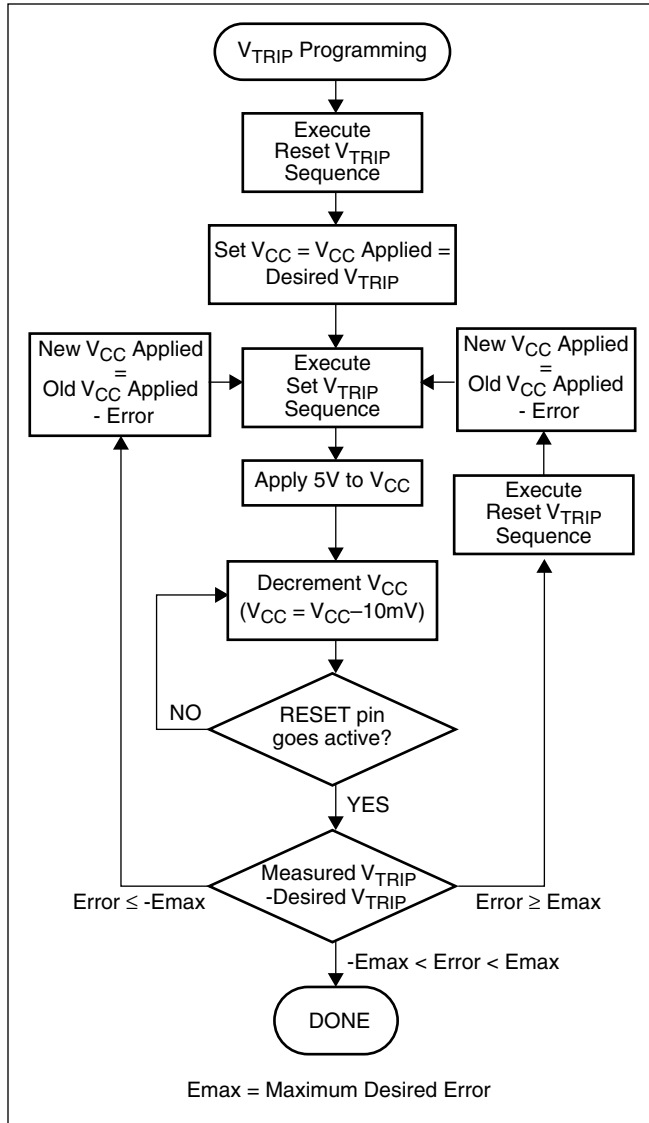


**Figure 3. Sample $V_{TRIP}$ Reset Circuit**

**Figure 4. V$_{TRIP}$ Programming Sequence**



V$_{TRIP}$ Programming

Execute Reset V$_{TRIP}$ Sequence

Set V$_{CC}$ = V$_{CC}$ Applied = Desired V$_{TRIP}$

New V$_{CC}$ Applied = Old V$_{CC}$ Applied - Error

Execute Set V$_{TRIP}$ Sequence

New V$_{CC}$ Applied = Old V$_{CC}$ Applied - Error

Apply 5V to V$_{CC}$

Execute Reset V$_{TRIP}$ Sequence

Decrement V$_{CC}$ (V$_{CC}$ = V$_{CC}$−10mV)

RESET pin goes active? NO

YES

Measured V$_{TRIP}$ -Desired V$_{TRIP}$

Error ≤ -Emax      Error ≥ Emax

-Emax < Error < Emax

DONE

Emax = Maximum Desired Error

## SPI Serial Memory

The memory portion of the device is a CMOS Serial EEPROM array with Xicor's block lock protection. The array is internally organized as x8 bits. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 1,000,000 cycles and a minimum data retention of 100 years.

The device is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families.

The device contains an 8-bit instruction register that controls the operation of the device. The instruction code is written to the device via the SI input. There are two write operations that requires only the instruction byte. There are two read operations that use the instruction byte to initiate the output of data. The remainder of the operations require an instruction byte, an 8-bit address, then data bytes. All instruction, address and data bits are clocked by the SCK input. All instructions (Table 1), addresses and data are transferred MSB first.

## Clock and Data Timing

Data input on the SI line is latched on the first rising edge of SCK after $\overline{CS}$ goes LOW. Data is output on the SO line by the falling edge of SCK. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off. $\overline{CS}$ must be LOW during the entire operation.

**Table 1. Instruction Set**

| Instruction Name | Instruction Format* | Operation |
|---|---|---|
| WREN | 0000 0110 | Set the Write Enable Latch (Enable Write Operations) |
| WRDI | 0000 0100 | Reset the Write Enable Latch (Disable Write Operations) |
| RSDR | 0000 0101 | Read Status Register |
| WRSR | 0000 0001 | Write Status Register (Watchdog and Block Lock) |
| READ | 0000 A$_8$011 | Read Data from Memory Array Beginning at Selected Address |
| WRITE | 0000 A$_8$010 | Write Data to Memory Array Beginning at Selected Address (1 to 16 bytes) |

**Note:** *Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

## Write Enable Latch

The device contains a Write Enable Latch. This latch must be SET before a Write Operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 3). This latch is automatically reset upon a power-up condition and after the completion of a valid byte, page, or status register write cycle. The latch is also reset if $\overline{WP}$ is brought LOW.

When issuing a WREN, WRDI or RDSR commands, it is not necessary to send a byte address or data.

**Figure 5. Write Enable/Disable Latch Sequence**
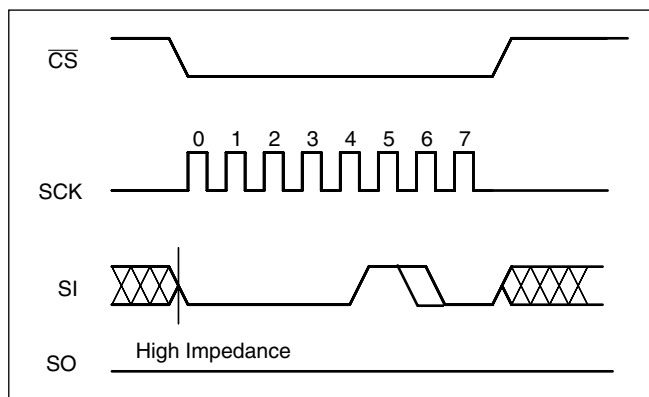


## Status Register

The Status Register contains four nonvolatile control bits and two volatile status bits. The control bits set the operation of the watchdog timer and the memory block lock protection. The Status Register is formatted as shown in "Status Register".

**Status Register: (Default = 00H)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | WD1 | WD0 | BL1 | BL0 | WEL | WIP |

The Write-In-Progress (WIP) bit is a volatile, read only bit and indicates whether the device is busy with an internal nonvolatile write operation. The WIP bit is read using the RDSR instruction. When set to a "1", a non-volatile write operation is in progress. When set to a "0", no write is in progress.

The Write Enable Latch (WEL) bit indicates the status of the "write enable" latch. When WEL = 1, the latch is set and when WEL = 0 the latch is reset. The WEL bit is a volatile, read only bit. The WREN instruction sets the WEL bit and the WRDS instruction resets the WEL bit.

The block lock bits, BL0 and BL1, set the level of block lock protection. These nonvolatile bits are programmed using the WRSR instruction and allow the user to protect one quarter, one half, all or none of the EEPROM array. Any portion of the array that is block lock protected can be read but not written. It will remain protected until the BL bits are altered to disable block lock protection of that portion of memory.

| Status Reg Bits | | Array Addresses Protected |
|---|---|---|
| **BL1** | **BL0** | **X5043/X5045** |
| 0 | 0 | None |
| 0 | 1 | $180–$1FF |
| 1 | 0 | $100–$1FF |
| 1 | 1 | $000–$1FF |

The Watchdog Timer bits, WD0 and WD1, select the Watchdog Time-out Period. These nonvolatile bits are programmed with the WRSR instruction.

| Status Register Bits | | Watchdog Time Out (Typical) |
|---|---|---|
| **WD1** | **WD0** | |
| 0 | 0 | 1.4 seconds |
| 0 | 1 | 600 milliseconds |
| 1 | 0 | 200 milliseconds |
| 1 | 1 | disabled |

## Read Status Register

To read the Status Register, pull $\overline{CS}$ low to select the device, then send the 8-bit RDSR instruction. Then the contents of the Status Register are shifted out on the SO line, clocked by CLK. Refer to the Read Status Register Sequence (Figure 6). The Status Register may be read at any time, even during a Write Cycle.

## Write Status Register

Prior to any attempt to write data into the status register, the "Write Enable" Latch (WEL) must be set by issuing the WREN instruction (Figure 5). First pull $\overline{CS}$ LOW, then clock the WREN instruction into the device and pull $\overline{CS}$ HIGH. Then bring $\overline{CS}$ LOW again and enter the WRSR instruction followed by 8 bits of data. These 8 bits of data correspond to the contents of the status register. The operation ends with $\overline{CS}$ going HIGH. If $\overline{CS}$ does not go HIGH between WREN and WRSR, the WRSR instruction is ignored.

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**Table 2. Device Protect Matrix**

| WREN CMD (WEL) | Device Pin (WP) | Memory Block | | Status Register (BL0, BL1, WD0, WD1) |
|---|---|---|---|---|
| | | **Protected Area** | **Unprotected Area** | |
| 0 | x | Protected | Protected | Protected |
| x | 0 | Protected | Protected | Protected |
| 1 | 1 | Protected | Writable | Writable |

**Figure 6. Read Status Register Sequence**
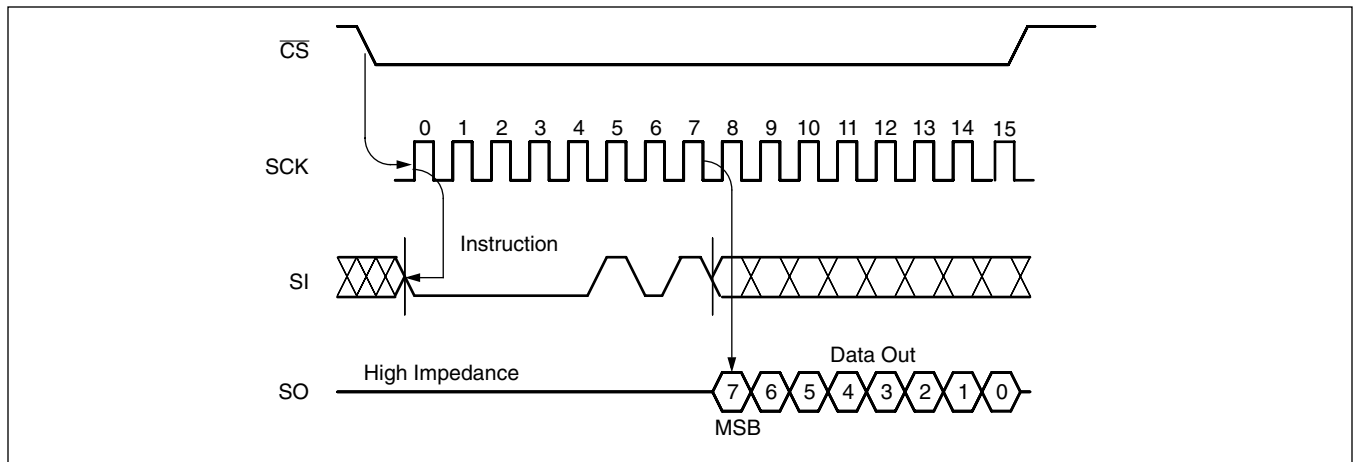


**Figure 7. Write Status Register Sequence**
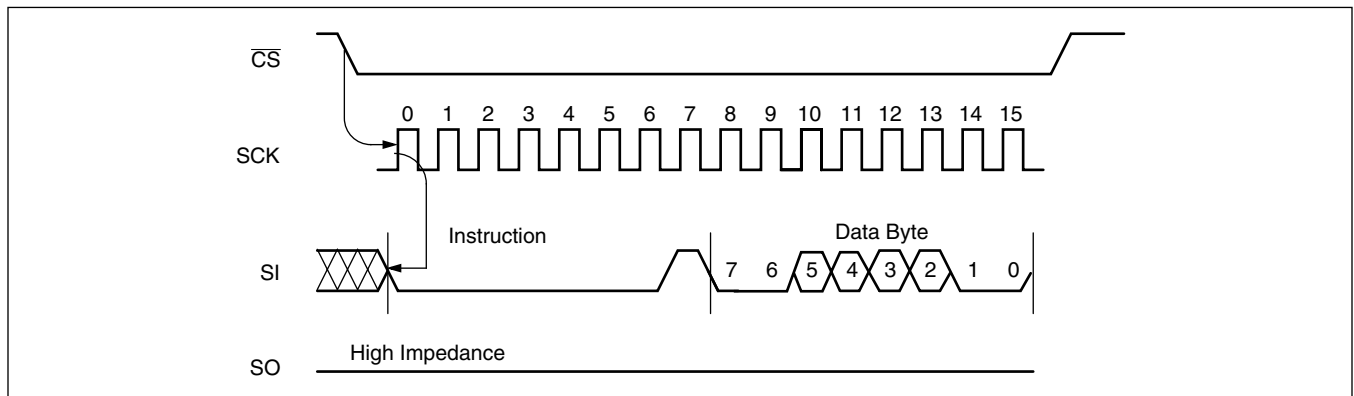


## Read Memory Array

When reading from the EEPROM memory array, $\overline{CS}$ is first pulled low to select the device. The 8-bit READ instruction is transmitted to the device, followed by the 8-bit address. Bit 3 of the READ instruction selects the upper or lower half of the device. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address $000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high. Refer to the Read EEPROM Array Sequence (Figure 8).

**Figure 8. Read EEPROM Array Sequence**
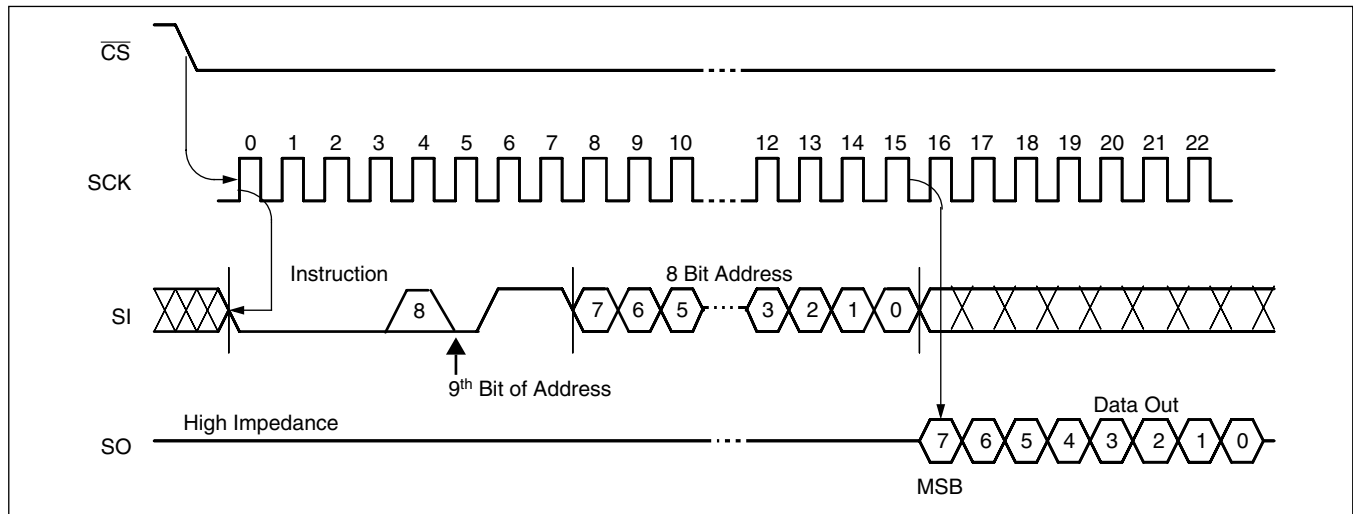


**Write Memory Array**

Prior to any attempt to write data into the memory array, the "Write Enable" Latch (WEL) must be set by issuing the WREN instruction (Figure 5). First pull $\overline{CS}$ LOW, then clock the WREN instruction into the device and pull $\overline{CS}$ HIGH. Then bring $\overline{CS}$ LOW again and enter the WRITE instruction followed by the 8-bit address and then the data to be written. Bit 3 of the WRITE instruction contains address bit $A_8$, which selects the upper or lower half of the array. If $\overline{CS}$ does not go HIGH between WREN and WRITE, the WRITE instruction is ignored.

The WRITE operation requires at least 16 clocks. $\overline{CS}$ must go low and remain low for the duration of the operation. The host may continue to write up to 16 bytes of data. The only restriction is that the 16 bytes must reside within the same page. A page address begins with address [x xxxx 0000] and ends with [x xxxx 1111]. If the byte address reaches the last byte on the page and the clock continues, the counter will roll back to the first address of the page and overwrite any data that has been previously written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ must be brought HIGH after bit 0 of the last complete data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed (Figure 9).

While the write is in progress following a status register or memory array write sequence, the Status Register may be read to check the WIP bit. WIP is HIGH while the nonvolatile write is in progress.

**Figure 9. Write Memory Sequence**
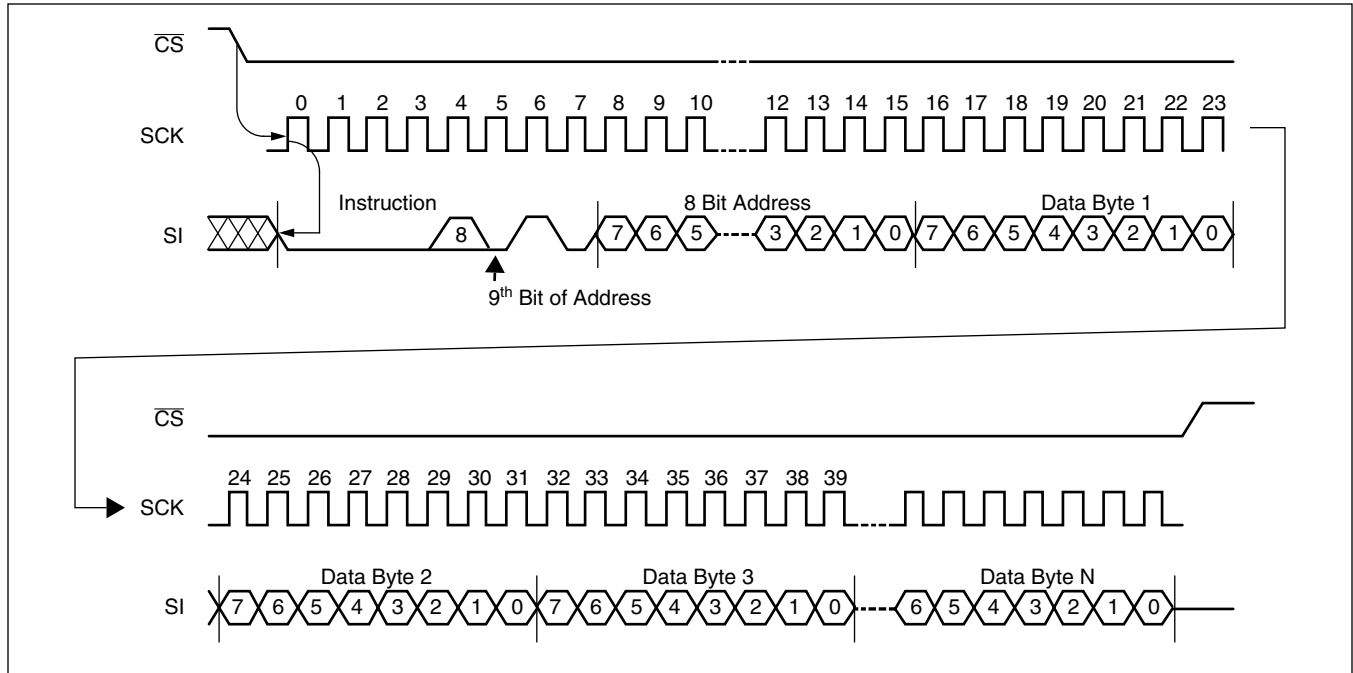


## OPERATIONAL NOTES

The device powers-up in the following state:

– The device is in the low power standby state.
– A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
– SO pin is high impedance.
– The Write Enable Latch is reset.
– The Flag Bit is reset.
– Reset Signal is active for $t_{PURST}$.

## Data Protection

The following circuitry has been included to prevent inadvertent writes:

– A WREN instruction must be issued to set the Write Enable Latch.
– $\overline{CS}$ must come HIGH at the proper clock count in order to start a nonvolatile write cycle.
– Block Protect bits provide additional level of write protection for the memory array.
– The $\overline{WP}$ pin LOW blocks nonvolatile write operations.

## ABSOLUTE MAXIMUM RATINGS

Temperature under bias ....................–65°C to +135°C
Storage temperature .........................–65°C to +150°C
Voltage on any pin with
   respect to $V_{SS}$.......................................–1.0V to +7V
D.C. output current ................................................ 5mA
Lead temperature (soldering, 10 seconds).........300°C

## COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Temperature | Min. | Max. |
|---|---|---|
| Commercial | 0°C | 70°C |
| Industrial | −40°C | +85°C |

| Option | Supply Voltage Limits |
|---|---|
| -2.7, -2.7A | 2.7V to 5.5V |
| Blank, -4.5A | 4.5V to 5.5V |

## D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Limits | | | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[2] | Max. | | |
| $I_{CC1}$ | $V_{CC}$ Write Current (Active) | | | 3 | mA | SCK = 3.3MHz[3]; SO, $\overline{RESET}$, RESET = Open |
| $I_{CC2}$ | $V_{CC}$ Read Current (Active) | | | 2 | mA | SCK = 3.3MHz[3]; SI = $V_{SS}$, $\overline{RESET}$, RESET = Open |
| $I_{SB1}$ | $V_{CC}$ Standby Current WDT = OFF | | | 10 | µA | $\overline{CS}$ = $V_{CC}$, SCK, SI = $V_{SS}$, $V_{CC}$ = 5.5V |
| $I_{SB2}$ | $V_{CC}$ Standby Current WDT = ON | | | 50 | µA | $\overline{CS}$ = $V_{CC}$, SCK, SI = $V_{SS}$, $V_{CC}$ = 5.5V |
| $I_{LI}$ | Input Leakage Current | | 0.1 | 10 | µA | SCK, SI, WP = $V_{SS}$ to $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | 0.1 | 10 | µA | SO, $\overline{RESET}$, RESET = $V_{SS}$ to $V_{CC}$ |
| $V_{IL}$[1] | Input LOW Voltage | −0.5 | | $V_{CC}$ x 0.3 | V | SCK, SI, $\overline{WP}$, $\overline{CS}$ |
| $V_{IH}$[1] | Input HIGH Voltage | $V_{CC}$ x 0.7 | | $V_{CC}$ + 0.5 | V | SCK, SI, $\overline{WP}$, $\overline{CS}$ |
| $V_{OL}$ | Output LOW Voltage (SO) | | | 0.4 | V | $I_{OL}$ = 2mA @ $V_{CC}$ = 2.7V, $I_{OL}$ = 0.5mA @ $V_{CC}$ = 1.8V |
| $V_{OH1}$ | Output HIGH Voltage (SO) | $V_{CC}$ − 0.8 | | | V | $V_{CC}$ > 3.3V, $I_{OH}$ = −1.0mA |
| $V_{OH2}$ | Output HIGH Voltage (SO) | $V_{CC}$ − 0.4 | | | V | 2V < $V_{CC}$ ≤ 3.3V, $I_{OH}$ = −0.4mA |
| $V_{OH3}$ | Output HIGH Voltage (SO) | $V_{CC}$ − 0.2 | | | V | $V_{CC}$ ≤ 2V, $I_{OH}$ = −0.25mA |
| $V_{OLRS}$ | Output LOW Voltage ($\overline{RESET}$, RESET) | | | 0.4 | V | $I_{OL}$ = 1mA |

## CAPACITANCE $T_A$ = +25°C, f = 1MHz, $V_{CC}$ = 5V

| Symbol | Test | Max. | Unit | Conditions |
|---|---|---|---|---|
| $C_{OUT}$[2] | Output Capacitance (SO, $\overline{RESET}$, RESET) | 8 | pF | $V_{OUT}$ = 0V |
| $C_{IN}$[2] | Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$) | 6 | pF | $V_{IN}$ = 0V |

**Notes:** (1) $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not tested.
     (2) This parameter is periodically sampled and not 100% tested.
     (3) SCK frequency measured from $V_{CC}$ x 0.1/$V_{CC}$ x 0.9

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## Equivalent A.C. Load Circuit at 5V V$_{CC}$
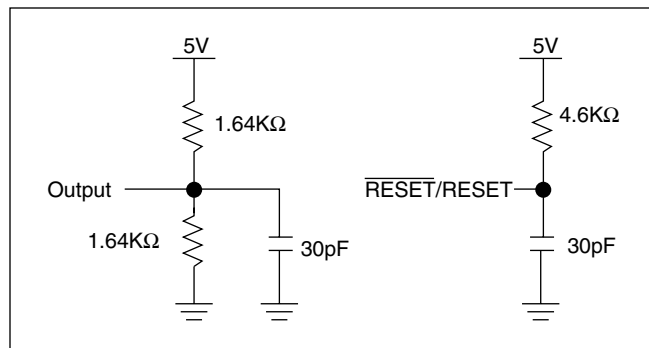


## A.C. Test Conditions

| Input pulse levels | V$_{CC}$ x 0.1 to V$_{CC}$ x 0.9 |
|---|---|
| Input rise and fall times | 10ns |
| Input and output timing level | V$_{CC}$ x0.5 |

**A.C. CHARACTERISTICS** (Over recommended operating conditions, unless otherwise specified)

### Data Input Timing

| Symbol | Parameter | 2.7V–5.5V | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| f$_{SCK}$ | Clock Frequency | 0 | 3.3 | MHz |
| t$_{CYC}$ | Cycle Time | 300 | | ns |
| t$_{LEAD}$ | $\overline{CS}$ Lead Time | 150 | | ns |
| t$_{LAG}$ | $\overline{CS}$ Lag Time | 150 | | ns |
| t$_{WH}$ | Clock HIGH Time | 130 | | ns |
| t$_{WL}$ | Clock LOW Time | 130 | | ns |
| t$_{SU}$ | Data Setup Time | 30 | | ns |
| t$_{H}$ | Data Hold Time | 30 | | ns |
| t$_{RI}$[3] | Input Rise Time | | 2 | μs |
| t$_{FI}$[3] | Input Fall Time | | 2 | μs |
| t$_{CS}$ | $\overline{CS}$ Deselect Time | 100 | | ns |
| t$_{WC}$[4] | Write Cycle Time | | 10 | ms |

### Data Output Timing

| Symbol | Parameter | 2.7–5.5V | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| f$_{SCK}$ | Clock Frequency | 0 | 3.3 | MHz |
| t$_{DIS}$ | Output Disable Time | | 150 | ns |
| t$_{V}$ | Output Valid from Clock Low | | 120 | ns |
| t$_{HO}$ | Output Hold Time | 0 | | ns |
| t$_{RO}$[3] | Output Rise Time | | 50 | ns |
| t$_{FO}$[3] | Output Fall Time | | 50 | ns |

**Notes:** (3) This parameter is periodically sampled and not 100% tested.
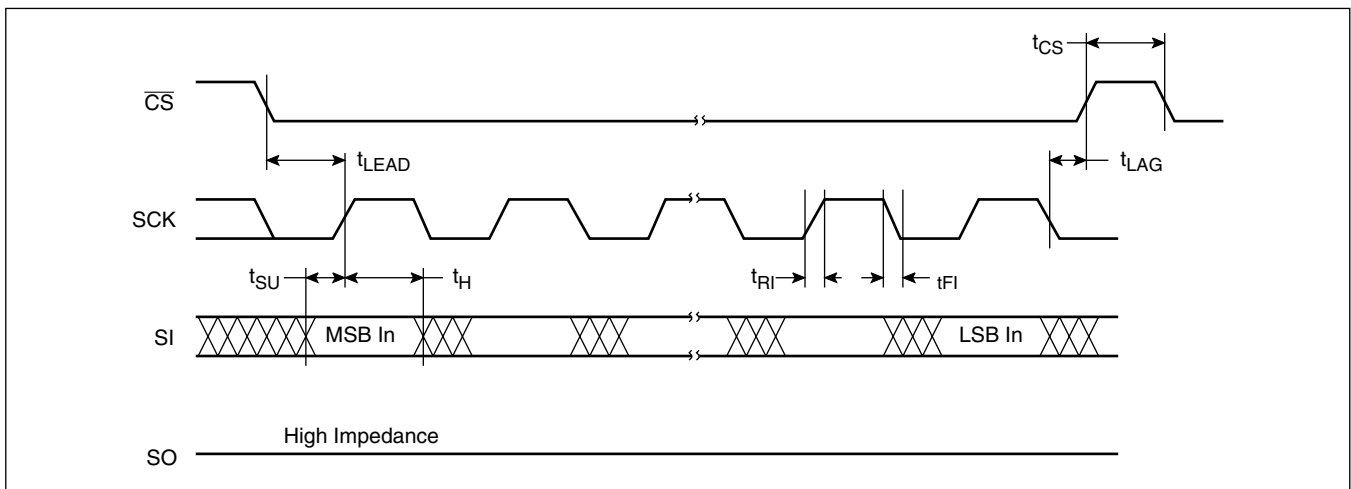
(4) t$_{WC}$ is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

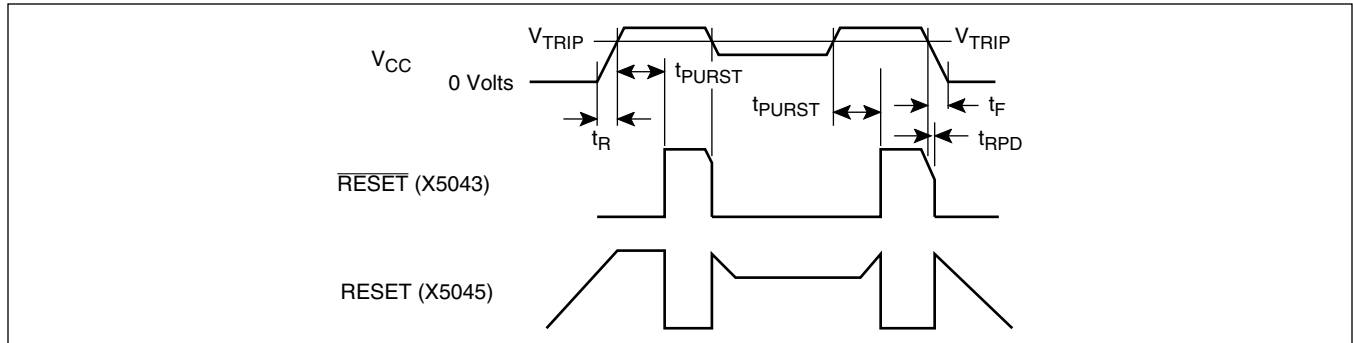# X5043/X5045

## Serial Output Timing
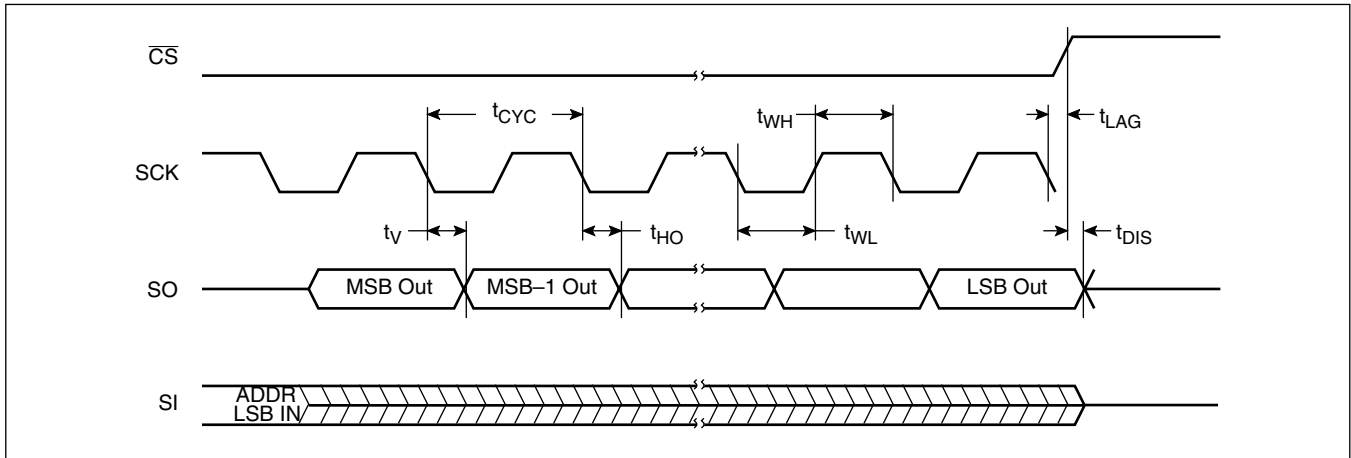


## Serial Input Timing



## SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
|  | Must be steady | Will be steady |
|  | May change from LOW to HIGH | Will change from LOW to HIGH |
|  | May change from HIGH to LOW | Will change from HIGH to LOW |
|  | Don't Care: Changes Allowed | Changing: State Not Known |
|  | N/A | Center Line is High Impedance |

## Power-Up and Power-Down Timing



## RESET Output Timing

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|-----------|------|------|------|------|
| $V_{TRIP}$ | Reset Trip Point Voltage, (-4.5A) | 4.5 | 4.62 | 4.75 | V |
| | Reset Trip Point Voltage, (Blank) | 4.25 | 4.38 | 4.5 | |
| | Reset Trip Point Voltage, (-2.7A) | 2.85 | 2.92 | 3.0 | |
| | Reset Trip Point Voltage, (-2.7) | 2.55 | 2.62 | 2.7 | |
| $t_{PURST}$ | Power-up Reset Time Out | 100 | 200 | 400 | ms |
| $t_{RPD}$[5] | $V_{CC}$ Detect to Reset/Output | | | 500 | ns |
| $t_F$[5] | $V_{CC}$ Fall Time | 10 | | | µs |
| $t_R$[5] | $V_{CC}$ Rise Time | 0.1 | | | ns |
| $V_{RVALID}$ | Reset Valid $V_{CC}$ | 1 | | | V |

**Note:** (5) This parameter is periodically sampled and not 100% tested.

## CS/WDI vs. RESET/RESET Timing
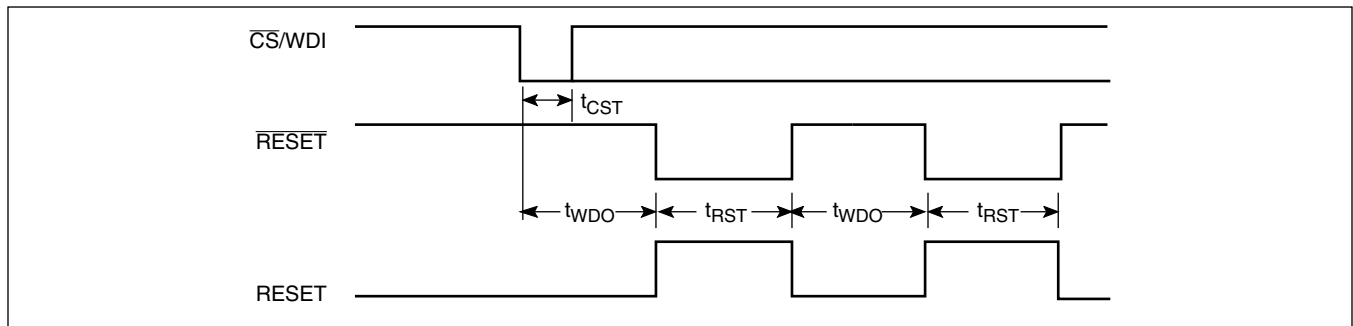


## RESET/RESET Output Timing

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|-----------|------|------|------|------|
| $t_{WDO}$ | Watchdog Time Out Period, | | | | |
| | WD1 = 1, WD0 = 0 | 100 | 200 | 300 | ms |
| | WD1 = 0, WD0 = 1 | 450 | 600 | 800 | ms |
| | WD1 = 0, WD0 = 0 | 1 | 1.4 | 2 | sec |
| $t_{CST}$ | CS Pulse Width to Reset the Watchdog | 400 | | | ns |
| $t_{RST}$ | Reset Time Out | 100 | 200 | 400 | ms |

# X5043/X5045

## V$_{TRIP}$ Programming Timing Diagram
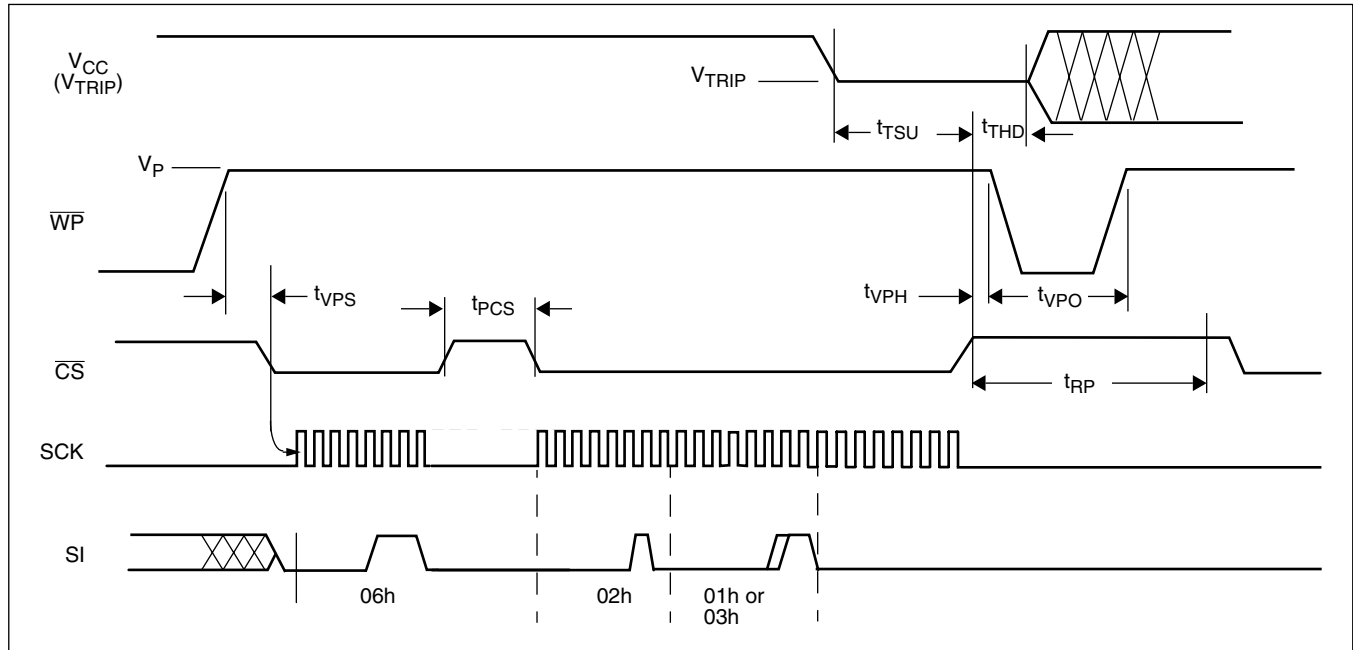


## V$_{TRIP}$ Programming Parameters

| Parameter | Description | Min | Max | Unit |
|-----------|-------------|-----|-----|------|
| t$_{VPS}$ | V$_{TRIP}$ Program Enable Voltage Setup time | 1 | | µs |
| t$_{VPH}$ | V$_{TRIP}$ Program Enable Voltage Hold time | 1 | | µs |
| t$_{PCS}$ | V$_{TRIP}$ Programming $\overline{CS}$ inactive time | 1 | | µs |
| t$_{TSU}$ | V$_{TRIP}$ Setup time | 1 | | µs |
| t$_{THD}$ | V$_{TRIP}$ Hold (stable) time | 10 | | ms |
| t$_{WC}$ | V$_{TRIP}$ Write Cycle Time | | 10 | ms |
| t$_{VPO}$ | V$_{TRIP}$ Program Enable Voltage Off time (Between successive adjustments) | 0 | | µs |
| t$_{RP}$ | V$_{TRIP}$ Program Recovery Period (Between successive adjustments) | 10 | | ms |
| V$_P$ | Programming Voltage | 15 | 18 | V |
| V$_{TRAN}$ | V$_{TRIP}$ Programmed Voltage Range | 1.7 | 5.0 | V |
| V$_{ta1}$ | Initial V$_{TRIP}$ Program Voltage accuracy (V$_{CC}$ applied–V$_{TRIP}$) (Programmed at 25°C.) | -0.1 | +0.4 | V |
| V$_{ta2}$ | Subsequent V$_{TRIP}$ Program Voltage accuracy [(V$_{CC}$ applied–V$_{ta1}$)–V$_{TRIP}$. Programmed at 25°C.) | -25 | +25 | mV |
| V$_{tr}$ | V$_{TRIP}$ Program Voltage repeatability (Successive program operations. Programmed at 25°C.) | -25 | +25 | mV |
| V$_{tv}$ | V$_{TRIP}$ Program variation after programming (0–75°C). (Programmed at 25°C.) | -25 | +25 | mV |

V$_{TRIP}$ programming parameters are periodically sampled and are not 100% tested.

## PACKAGING INFORMATION

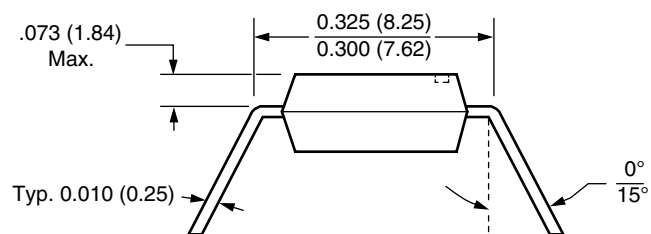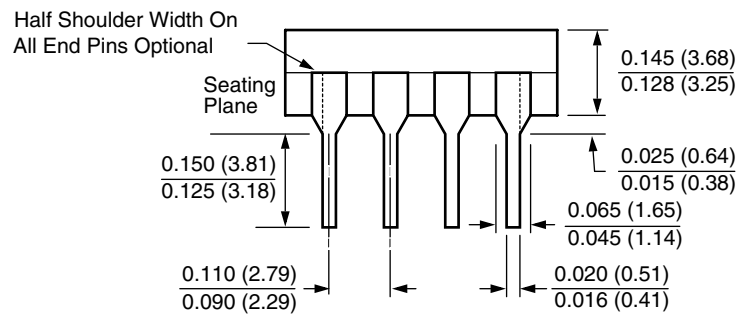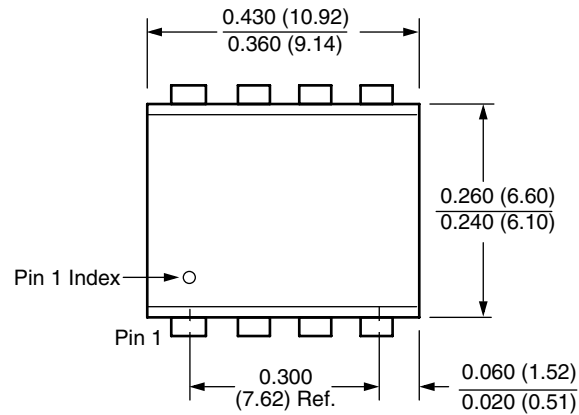### 8-Lead Miniature Small Outline Gull Wing Package Type M

0.118 ± 0.002
(3.00 ± 0.05)

0.012 + 0.006 / -0.002
(0.30 + 0.15 / -0.05)

0.0256 (0.65) Typ.

R 0.014 (0.36)

0.118 ± 0.002
(3.00 ± 0.05)

0.030 (0.76)

0.0216 (0.55)

0.036 (0.91)
0.032 (0.81)

7° Typ.

0.040 ± 0.002
(1.02 ± 0.05)

0.008 (0.20)
0.004 (0.10)

0.007 (0.18)
0.005 (0.13)

0.150 (3.81)
Ref.

0.193 (4.90)
Ref.

0.0256" Typical

0.025"
Typical

0.220"

0.020"
Typical
8 Places

**FOOTPRINT**
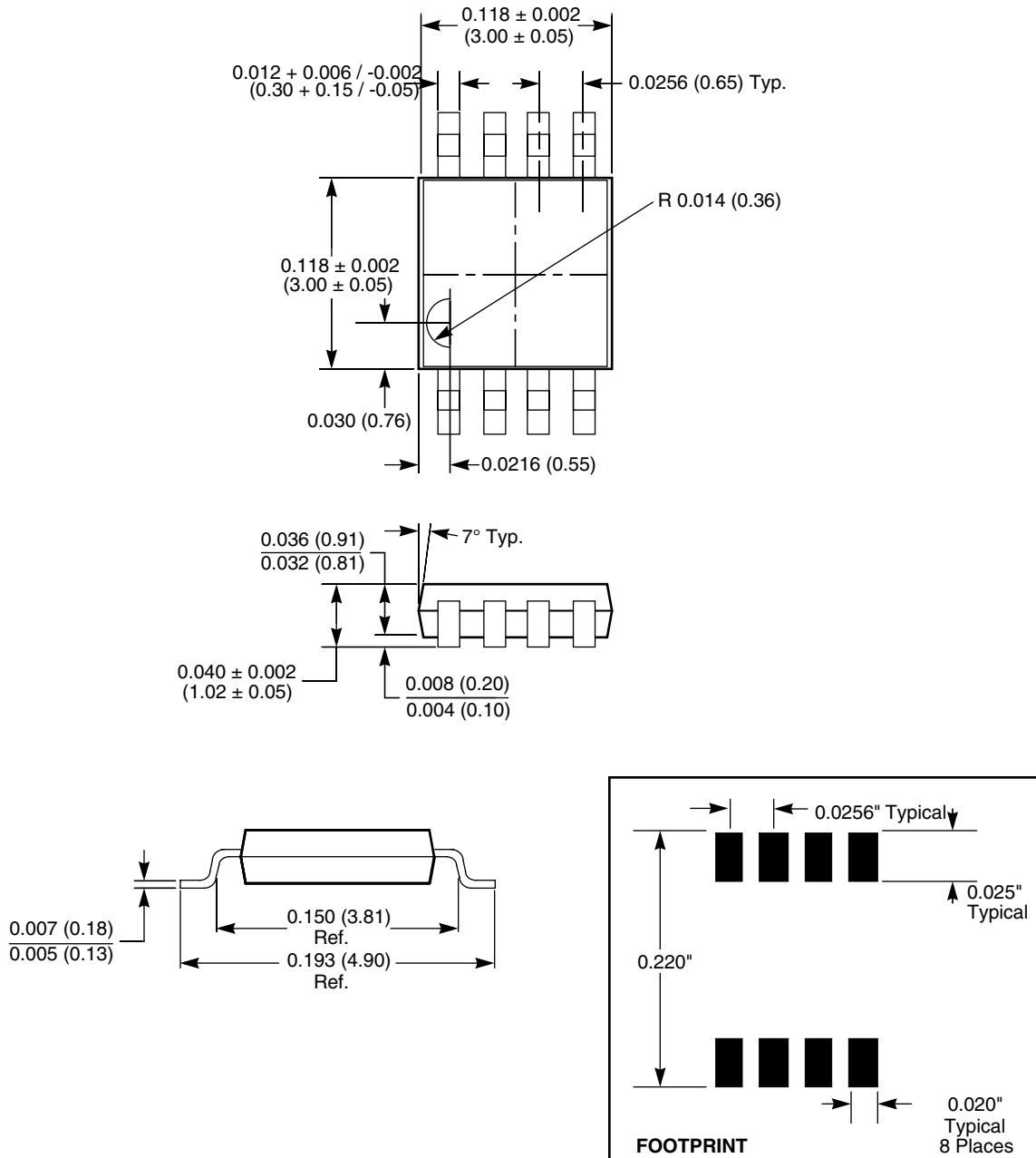
**NOTE:**
**1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)**

# X5043/X5045

## PACKAGING INFORMATION

### 8-Lead Plastic Dual In-Line Package Type P



Pin 1 Index

Pin 1

0.430 (10.92) / 0.360 (9.14)

0.260 (6.60) / 0.240 (6.10)

0.300 (7.62) Ref.

0.060 (1.52) / 0.020 (0.51)

Half Shoulder Width On All End Pins Optional

Seating Plane

0.145 (3.68) / 0.128 (3.25)

0.150 (3.81) / 0.125 (3.18)

0.025 (0.64) / 0.015 (0.38)

0.065 (1.65) / 0.045 (1.14)

0.110 (2.79) / 0.090 (2.29)

0.020 (0.51) / 0.016 (0.41)

.073 (1.84) Max.

0.325 (8.25) / 0.300 (7.62)

Typ. 0.010 (0.25)

0°/15°

**NOTE:**
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

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## PACKAGING INFORMATION

### 8-Lead Plastic Small Outline Gull Wing Package Type S



Pin 1 Index

Pin 1

$\dfrac{0.150\ (3.80)}{0.158\ (4.00)}$    $\dfrac{0.228\ (5.80)}{0.244\ (6.20)}$

$\dfrac{0.014\ (0.35)}{0.019\ (0.49)}$

$\dfrac{0.188\ (4.78)}{0.197\ (5.00)}$

(4X) 7°

$\dfrac{0.053\ (1.35)}{0.069\ (1.75)}$

0.050 (1.27)

$\dfrac{0.004\ (0.19)}{0.010\ (0.25)}$

$\dfrac{0.010\ (0.25)}{0.020\ (0.50)}$ X 45°

0° - 8°

$\dfrac{0.0075\ (0.19)}{0.010\ (0.25)}$

$\dfrac{0.016\ (0.410)}{0.037\ (0.937)}$

0.050"Typical

0.050" Typical

0.250"

0.030" Typical 8 Places

**FOOTPRINT**

**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

## PACKAGING INFORMATION

### 14-Lead Plastic, TSSOP, Package Type V

.025 (.65) BSC

.169 (4.3)
.177 (4.5)

.252 (6.4) BSC

.193 (4.9)
.200 (5.1)

.047 (1.20)

.0075 (.19)
.0118 (.30)

.002 (.05)
.006 (.15)

.010 (.25)

Gage Plane

Seating Plane

0° - 8°

.019 (.50)
.029 (.75)

Detail A (20X)

.031 (.80)
.041 (1.05)

See Detail "A"

**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

## Ordering Information

| V_CC Range | V_TRIP Range | Package | Operating Temperature Range | Part Number $\overline{\text{RESET}}$ (Active LOW) | Part Number RESET (Active HIGH) |
|---|---|---|---|---|---|
| 4.5-5.5V | 4.5-4.75 | 8-Pin PDIP | -40°C–85°C | X5043PI-4.5A | X5045PI-4.5A |
| | | 8L SOIC | -40°C–85°C | X5043S8I-4.5A | X5045S8I-4.5A |
| | | 8L MSOP | -40°C–85°C | X5043M8I-4.5A | X5045M8I-4.5A |
| | | 14L TSSOP | -40°C–85°C | X5043V14I-4.5A | X5045V14I-4.5A |
| | 4.25-4.5 | 8-Pin PDIP | -40°C–85°C | X5043PI | X5045PI |
| | | 8L SOIC | 0°C–70°C | X5043S8 | X5045S8 |
| | | | -40°C–85°C | X5043S8I | X5045S8I |
| | | 8L MSOP | -40°C–85°C | X5043M8I | X5045M8I |
| | | 14L TSSOP | -40°C–85°C | X5043V14I | X5045V14I |
| 2.7-5.5V | 2.85-3.0 | 8L PDIP | -40°C–85°C | X5043PI-2.7A | X5045PI-2.7A |
| | | 8L SOIC | -40°C–85°C | X5043S8I-2.7A | X5045S8I-2.7A |
| | | 8L MSOP | -40°C–85°C | X5043M8I-2.7A | X5045M8I-2.7A |
| | | 14L TSSOP | -40°C–85°C | X5043V14I-2.7A | X5045V14I-2.7A |
| | 2.55-2.7 | 8-Pin PDIP | -40°C–85°C | X5043PI-2.7 | X5045PI-2.7 |
| | | 8L SOIC | 0°C–70°C | X5043S8-2.7 | X5045S8-2.7 |
| | | | -40°C–85°C | X5043S8I-2.7 | X5045S8I-2.7 |
| | | 8L MSOP | -40°C–85°C | X5043M8I-2.7 | X5045M8I-2.7 |
| | | 14L TSSOP | -40°C–85°C | X5043V14I-2.7 | X5045V14I-2.7 |

## Part Mark Information

**PDIP/SOIC**

X5043/45 X
X

Blank = 8-Lead SOIC
P= 8 Pin Plastic DIP

Blank = No suffix, 0°C to +70°C
I = No Suffix; –40°C to +85°C
A = -4,5A; 0°C to +70°C,
IA = -4.5A; –40°C to +85°C
F = -2.7; 0°C to +70°C
G = -2.7; –40°C to +85°C
FA = -2.7A; 0°C to +70°C
GA = -2.7A; –40°C to +85°C

**MSOP**

YWW
XXX

AEP/AEY = No Suffix; –40°C to +85°C
AEN/AEW = -4.5A; –40°C to +85°C
AET/AFC = -2.7; –40°C to +85°C
AER/AFA = -2.7A; –40°C to +85°C

X5043/X5045

**TSSOP**

X5043/45 W
X

V = 14 Lead TSSOP

Blank = 5V ±10%, 0°C to +70°C, $V_{TRIP}$ = 4.25-4.5
AL = 5V±10%, 0°C to +70°C, $V_{TRIP}$ = 4.5-4.75
I = 5V ±10%, –40°C to +85°C, $V_{TRIP}$ = 4.25-4.5
AM = 5V ±10%, –40°C to +85°C, $V_{TRIP}$ = 4.5-4.75
F = 2.7V to 5.5V, 0°C to +70°C, $V_{TRIP}$ = 2.55-2.7
AN = 2.7V to 5.5V, 0°C to +70°C, $V_{TRIP}$ = 2.85-3.0
G = 2.7V to 5.5V, –40°C to +85°C, $V_{TRIP}$ = 2.55-2.7
AP = 2.7V to 5.5V, –40°C to +85°C, $V_{TRIP}$ = 2.85-3.0