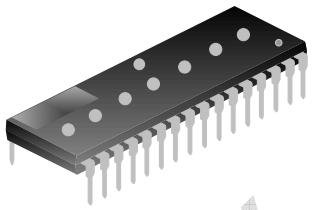
INTELLIGENT POWERMODULE，3 PHASE-BRIDGE 500V/5A

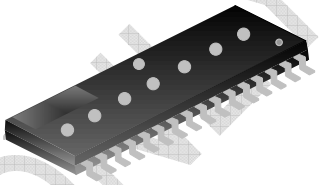
DESCRIPTION

SD05M50D/S is a robust, highly-integrated 3-phase BLDC motor driver IC, for small power motor drive applications such as fan motors and water suppliers. It incorporates 6 fast-recovery MOSFET(FRFET) and 3 half-bridge HVIC for FRFET gate driving.

The SD05M50D/S offers an extremely compact isolated package for very simple design. It integrated of under-voltage lockout function and dV/dt immune, deliver high level of protection and fail-safe operation. Each phase current of inverter can be monitored separately due to divided negative dc terminals. The package is optimized for the thermal performance and compacted for the use in the built-in motor application and any other application where the assembly space is concerned.



DIP-23



SOP-23

FEATURES

* 500V $R_{DS(on)}$=1.4Ω(max) 3-phase fast-recovery MOSFET inverter including high voltage integrated circuit(HVIC)
* 3 divided negative dc-link terminals for inverter current sensing applications
* HVIC for gate driving and under-voltage protection
* 3/5V CMOS/TTL compatible, active-high interface
* Optimized for low electromagnetic interference
* Isolation voltage rating of 1500Vrms for 1min.

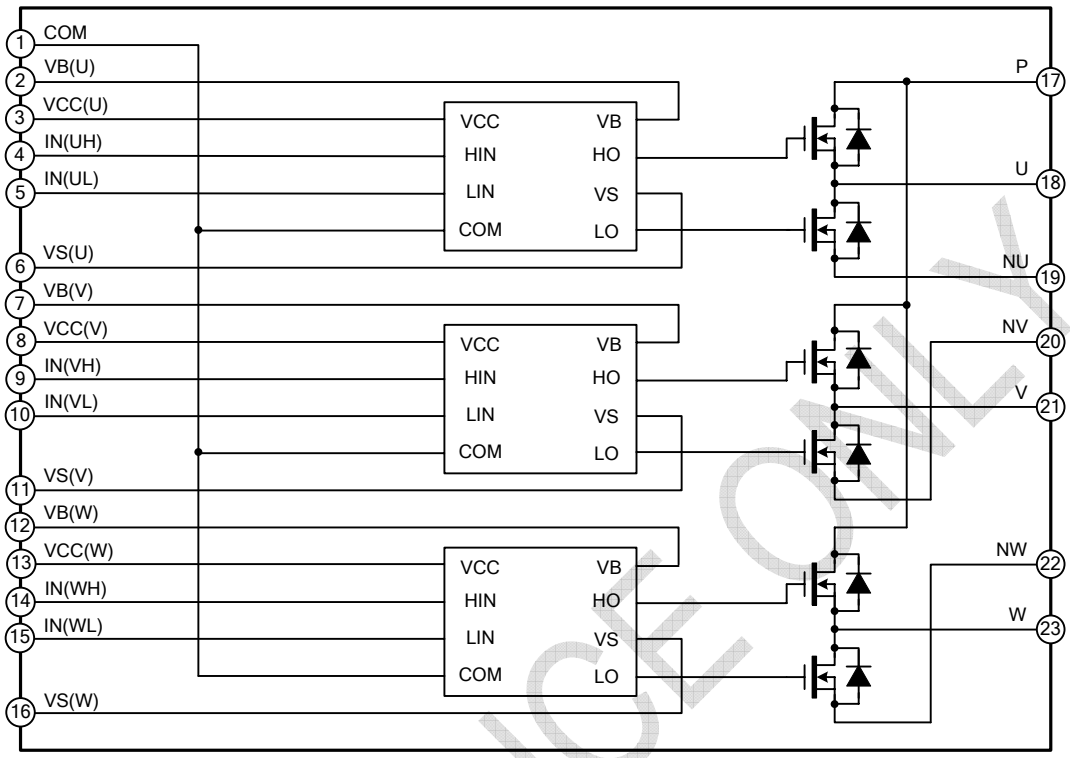
APPLICATIONS

* Air conditioner fan
* Refrigerator compressor
* Dishwasher pump

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SD05M50D	DIP-23	SD05M50D	Pb free	Tube
SD05M50S	SOP-23	SD05M50S	Pb free	Tube

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Ratings	Unit
DC Link Input Voltage, Drain-source Voltage of FRFET	V_{PN}	500	V
Each FRFET Drain Current, Continuous, T_C=25°C	I_{D25}	2.0	A
Each FRFET Drain Current, Continuous, T_C=80°C	I_{D80}	1.5	A
Each FRFET Drain Current, Peak, T_C=25°C, PW<100μs	I_{DP}	5	A
Maximum Power Dissipation, T_C=25°C	P_D	14.5	W
Control Supply Voltage	V_{CC}	20	V
High-side Bias Voltage	V_{BS}	20	V
Input Signal Voltage	V_{IN}	-0.3~V_{CC}+0.3	V
Operating Junction Temperature	T_J	-40~150	°C
Storage Temperature Range	T_{STG}	-50~150	°C
Junction to Case Thermal Resistance	$R_{\theta JC}$	8.6	°C/W
Isolation Voltage 60Hz, Sinusoidal, 1 minute, Connection pins to heatsink	V_{ISO}	1500	V_{rms}

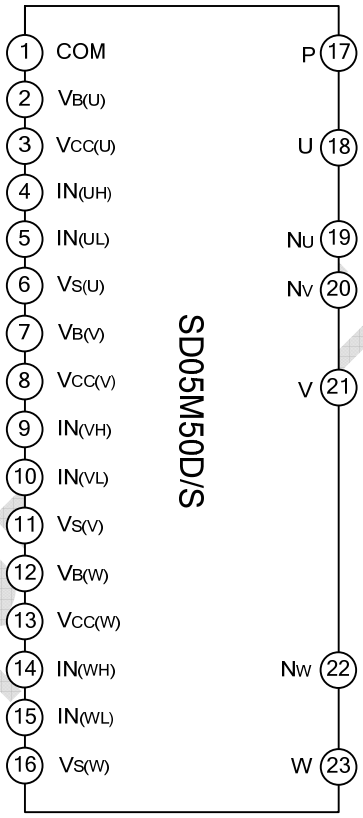
RECOMMENDED OPRATING CONDITIONS

Characteristics	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{PN}		300	400	V
Control Supply Voltage	V_{CC}	13.5	15	16.5	V
High-side Bias Voltage	V_{BS}	13.5	15	16.5	V
Input ON Threshold Voltage	$V_{IN(ON)}$	3.0	-	VCC	V
Input OFF Threshold Voltage	$V_{IN(OFF)}$	0	-	0.6	V
Blanking Time for Preventing Arm-short V_{CC}=V_{BS}=13.5~16.5V, T_J≤25°C	T_{dead}	1.0	-	-	μs
PWM Switching Frequency	f_{PWM}	-	15	-	KHz

ELECTRICAL CHARACTERISTICS (Unless specified particularly T_{amb}=25°C, V_{CC}=V_{BS}=15V)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{CC}=V_{BS}=15V,V_{IN}=5V,I_D=1.2A	-	1.0	1.4	Ω
Drain-Source Diode Forward voltage	V_{SD}	V_{CC}=V_{BS}=15V,V_{IN}=0V,I_D=-1.2A	-	-	1.2	V

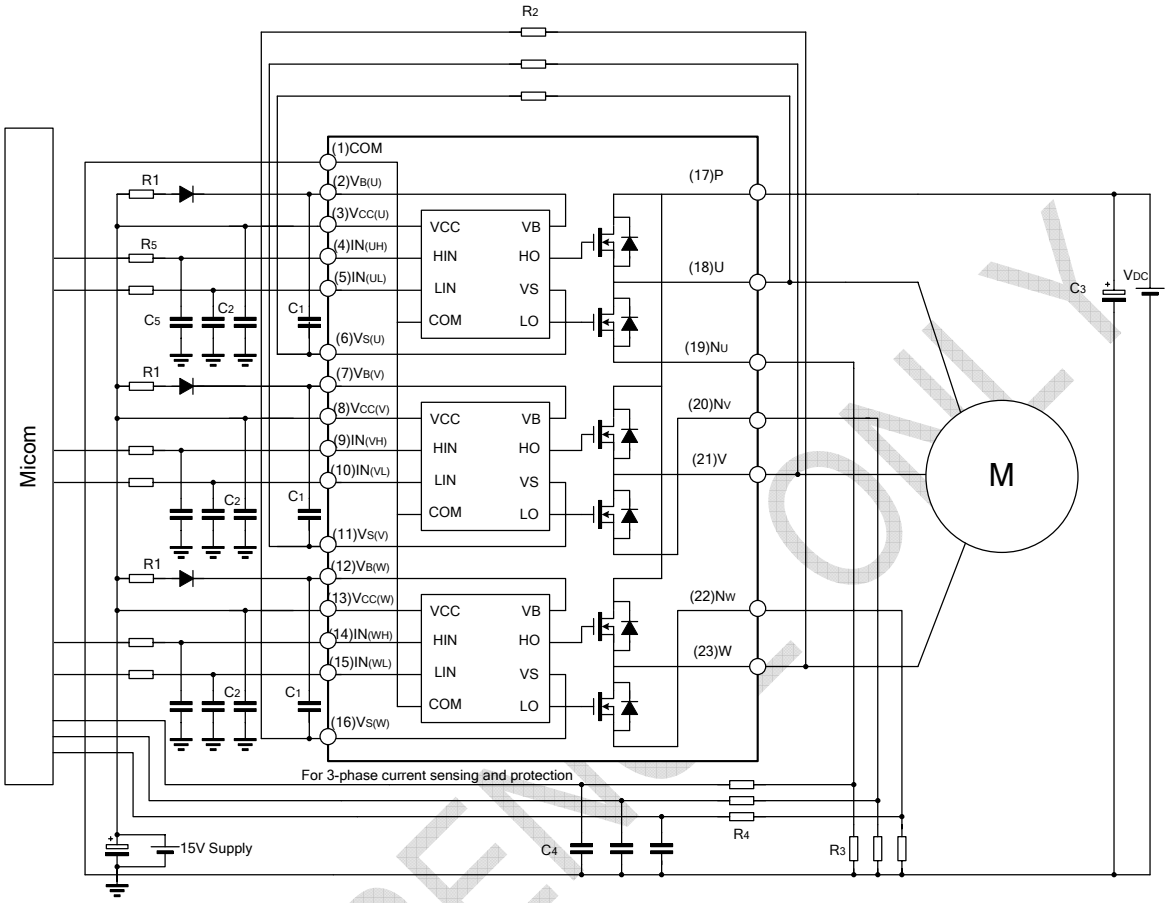
PIN CONFIGURATIONS



PIN DESCRIPTIONS

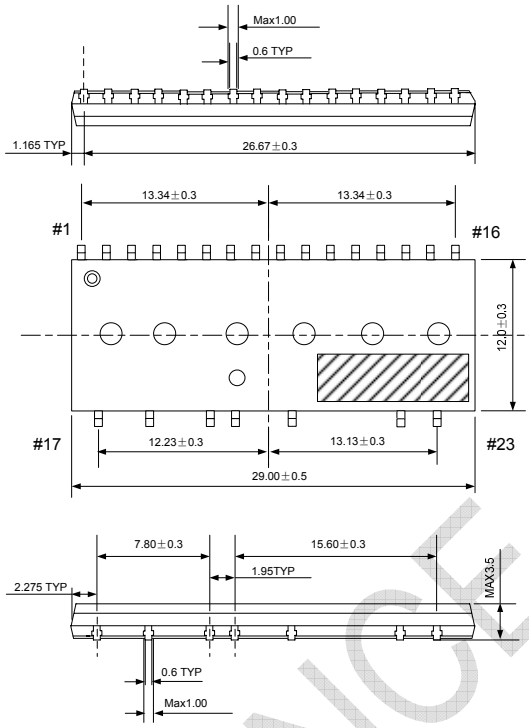
Pin No.	Pin Name	I/O	Description
1	COM	I/O	IC Common Supply Ground
2	$V_{B(U)}$	I/O	Bias Voltage for U Phase High Side FRFET Driving
3	$V_{CC(U)}$	I/O	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	$IN_{(UH)}$	I	Signal Input for U Phase High-side
5	$IN_{(UL)}$	I	Signal Input for U Phase Low-side
6	$V_{S(U)}$	I/O	Bias Voltage Ground for U Phase High Side FRFET Driving
7	$V_{B(V)}$	I/O	Bias Voltage for V Phase High Side FRFET Driving
8	$V_{CC(V)}$	I/O	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	$IN_{(VH)}$	I	Signal Input for V Phase High-side
10	$IN_{(VL)}$	I	Signal Input for V Phase Low-side
11	$V_{S(V)}$	I/O	Bias Voltage Ground for V Phase High Side FRFET Driving
12	$V_{B(W)}$	I/O	Bias Voltage for W Phase High Side FRFET Driving
13	$V_{CC(W)}$	I/O	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	$IN_{(WH)}$	I	Signal Input for W Phase High-side
15	$IN_{(WL)}$	I	Signal Input for W Phase Low-side
16	$V_{S(W)}$	I/O	Bias Voltage Ground for W Phase High Side FRFET Driving
17	P	I/O	Positive DC–Link Input
18	U	O	Output for U Phase
19	NU	I/O	Negative DC–Link Input for U Phase
20	NV	I/O	Negative DC–Link Input for V Phase
21	V	O	Output for V Phase
22	NW	I/O	Negative DC–Link Input for W Phase
23	W	O	Output for W Phase

TYPICAL APPLICATION CIRCUIT

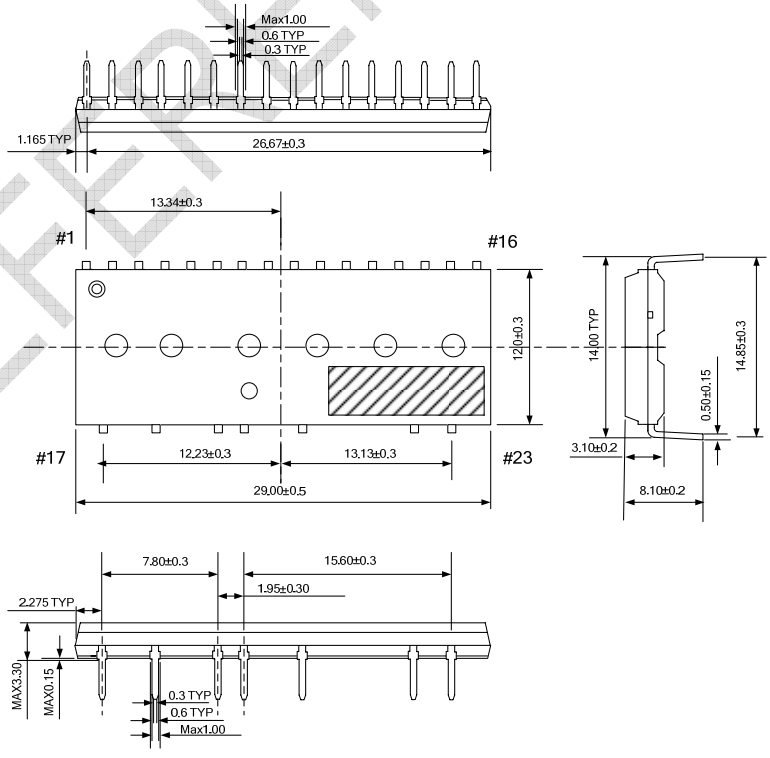


PACKAGE OUTLINE

SOP-23 UNIT: mm



DIP-23 UNIT: mm



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Disclaimer :

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!