

# Preliminary

## MOS Memories



### ■ MB8464A-10-W, MB8464A-15-W CMOS 65,536-Bit Static Random Access Memory with Data Retention Mode

#### Description

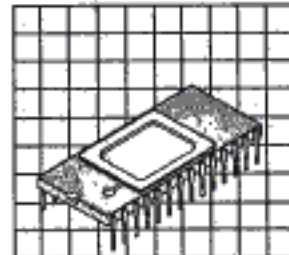
The Fujitsu MB8464A-W is a 8,192-word by 8-bit static random access memory fabricated with a CMOS silicon gate process.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volt power supply is required.

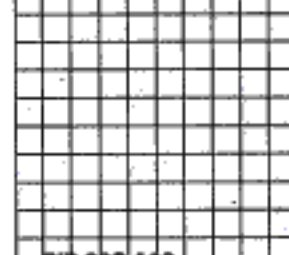
The MB8464A-W is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

#### Features

- Organization: 8,192 words x 8-bits
- Fast access times:  
 TAVQV = TELQV = 100 ns max. (MB8464A-10-W)  
 TAVQV = TELQV = 150 ns max. (MB8464A-15-W)
- Completely static operation:  
 No clock required
- TTL compatible input/output
- Three-state output
- Common data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby:  
 11 mW max.
- Data retention: 2.0V min.
- 28-pin ceramic package (300 mil width)
- 32-pad leadless chip carrier (500 mil width)
- Pin compatible with MB8464-W



DIP-28C-A07



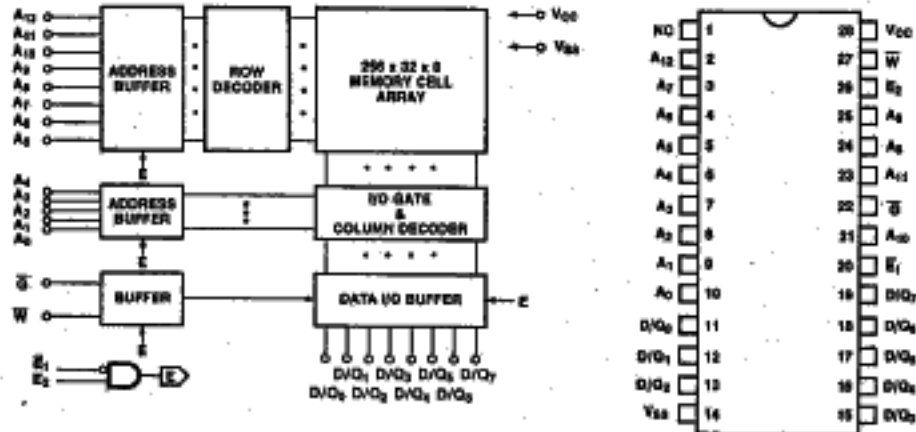
DIP-28C-A08



LCD-32C-A02

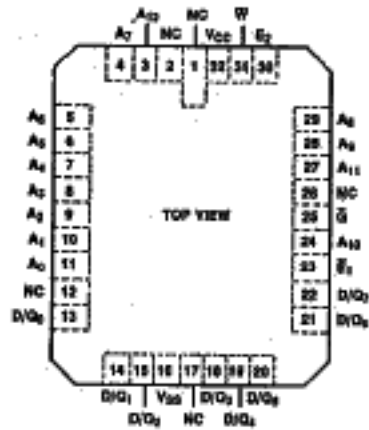
MB8464A-10-W  
MB8464A-16-W

MB8464A-W Block Diagram and Pin Assignment



TRUTH TABLE

E <sub>1</sub>	E <sub>2</sub>	G	W	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	NOT SELECTED	I <sub>SB</sub>	HIGH-Z
X	L	X	X	NOT SELECTED	I <sub>SB</sub>	HIGH-Z
L	H	H	H	OUT DISABLE	I <sub>CC</sub>	HIGH-Z
L	H	L	H	READ	I <sub>CC</sub>	Q <sub>OUT</sub>
L	H	X	L	WRITE	I <sub>CC</sub>	W



**Absolute Maximum Ratings**  
(See note)

Rating	Symbol	Value	Unit
Storage temperature range	T <sub>STG</sub>	-65 to +150	°C
Temperature under bias	T <sub>BVS</sub>	-55 to +125	°C
Supply voltage	V <sub>CC</sub>	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
Output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUJITSU

MB8464A-10-W  
MB8464A-15-W

**Recommended Operating Conditions**  
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input low voltage	$V_{IL}$	-0.3		0.6	V
Input high voltage	$V_{IH}$	2.4		$V_{CC} + 0.3$	V
Ambient temperature	$T_A$	-55		+125	°C

**Capacitance**  
( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit
I/O capacitance ( $V_{IO} = 0\text{V}$ )	$C_{IO}$			6	pF
Input capacitance ( $V_{IN} = 0\text{V}$ )	$C_{IN}$			6	pF

**DC Characteristics**  
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8464A-10-W MB8464A-15-W		Unit	Test Condition
		Min	Max		
Standby supply current	$I_{SB1}$	2		mA	$E_2 = 0.2\text{V}$ , $E_1 > V_{CC} - 0.2\text{V}$ ( $E_2 = 0.2\text{V}$ or $E_2 > V_{CC} - 0.2\text{V}$ )
	$I_{SB2}$	6		mA	$E_1 = V_{IH}$ or $E_2 = V_L$
Active supply current	$I_{CC1}$	70		mA	$E_1 = V_L$ , $E_2 = V_{IH}$ $V_{IN} = V_{IH}$ or $V_L$ , $I_{OUT} = 0\text{ mA}$
Operating supply current	$I_{CC2}$	90		mA	Cycle = min., duty = 100%, $I_{OUT} = 0\text{ mA}$
Input leakage current	$I_{LI}$	-10	10	$\mu\text{A}$	$V_{IN} = 0\text{V}$ to $V_{CC}$
Output leakage current	$I_{LZO}$	-50	50	$\mu\text{A}$	$V_{IO} = 0\text{V}$ to $V_{CC}$ $E_1 = V_{IH}$ or $E_2 = V_L$ or $G = V_{IH}$ or $W = V_L$
Output high voltage	$V_{OH}$	2.4		V	$I_{OH} = -1.0\text{ mA}$
Output low voltage	$V_{OL}$		0.4	V	$I_{OL} = 2.1\text{ mA}$

Note: All voltages are referenced to  $V_{SS}$ .

**AC Characteristics**  
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8464A-10-W		MB8464A-15-W		Unit
		Min	Max	Min	Max	
Read cycle time	TAXX	100		150		ns
Address access time	TAVQV		100		150	ns
$E_1$ access time	TE1LQV		100		150	ns
$E_2$ access time	TE2HQV		100		150	ns
Output enable to output valid	TGLOV		45		60	ns
Output hold from address change	TAXQX	10		10		ns
Chip enable to output low-Z*	TE1LOX TE2HOX	10		10		ns
Output enable to output low-Z*	TGLQZ	5		5		ns
Chip enable to output high-Z*	TE1HOZ TE2LOZ		40		50	ns
Output enable to output high-Z*	TGHOZ		40		50	ns

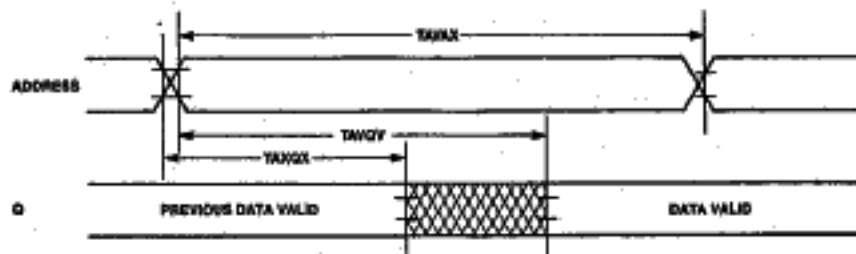
Note: \* Transition is measured at the point of +500 mV from steady state voltage.

MB9464A-10-W  
MB9464A-15-W

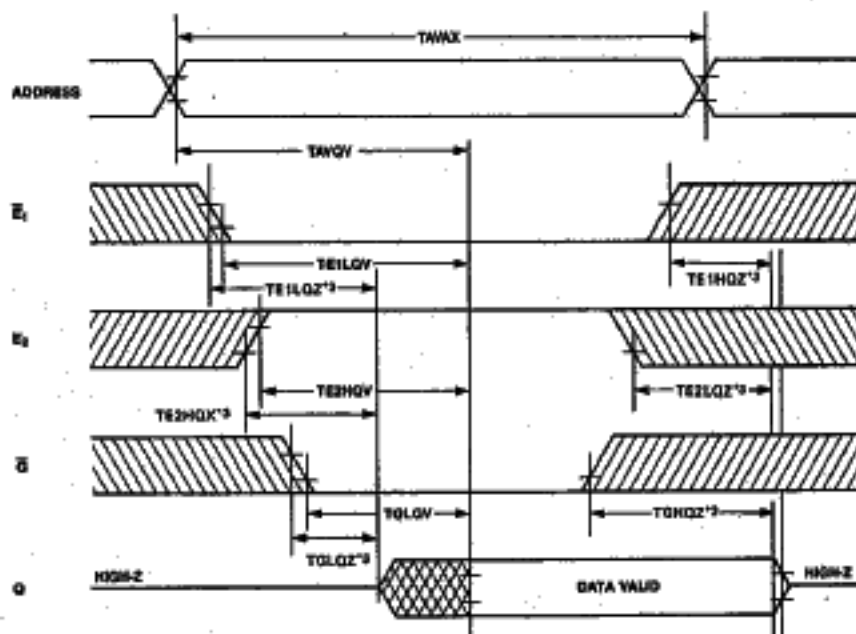
**AC Characteristics**  
(Continued)  
(Recommended operating  
conditions unless otherwise  
noted)

**Read Cycle Timing Diagrams**

**Read Cycle I<sup>1,2</sup>**



**Read Cycle II<sup>1</sup>**



NOTES: <sup>1</sup> W IS HIGH FOR READ CYCLE.  
<sup>2</sup> DEVICE IS CONTINUOUSLY SELECTED,  $E_1 = \bar{O} = V_{OL}$ ,  $E_2 = V_{OH}$ .  
<sup>3</sup> TRANSITION IS MEASURED AT THE POINT OF 500-mV STEADY STATE VOLTAGE.

▨ DON'T CARE  
▩ UNDEFINED

MB8464A-10-W  
MB8464A-15-W

**AC Characteristics**  
(Continued)  
(Recommended operating  
conditions unless otherwise  
noted)

**Write Cycle**

Parameter	Symbol	MB8464A-10-W		MB8464A-15-W		Unit
		Min	Max	Min	Max	
Write cycle time	TAVAX	100		150		ns
Address valid to end of write	TAVWH, TAVE1L, TAVE2H	80		100		ns
Chip enable to end of write	TE1LE1H, TE2H2EL	80		100		ns
Data valid to end of write	TDVWH, TDVE1L, TDVE2H	40		50		ns
Data hold time	TWHDX, TE1HDX, TE2LDX	5		5		ns
Write pulse width	TWLWH	60		70		ns
Address setup time	TAVWL, TAVE1L, TAVE2H	0		10		ns
Write recovery time	TWHAX, TE1HAX, TE2LAX	10		10		ns
Write enable to output low-Z*	TWHQX	5		5		ns
Write enable to output high-Z*	TWLQZ		40		50	ns

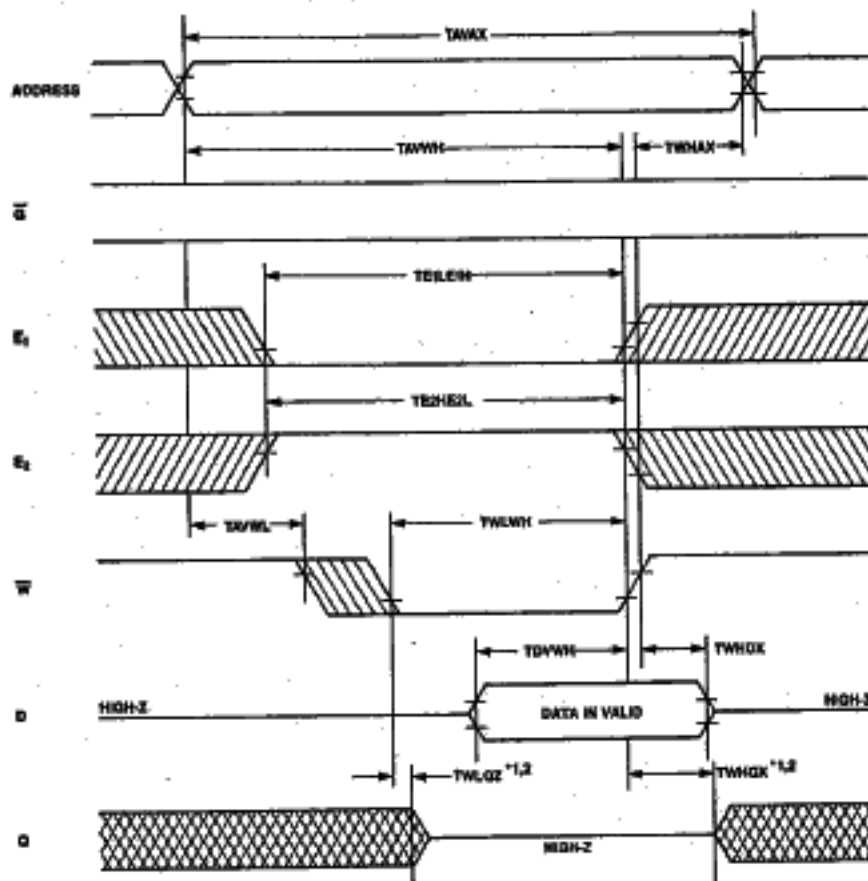
\*TRANSITION IS MEASURED AT THE POINT OF ±500 mV STEADY STATE VOLTAGE.

MB8464A-16-W  
MB8464A-16-W

**AC Characteristics**  
(Continued)  
(Recommended operating conditions unless otherwise noted)

**Write Cycle Timing Diagrams**

**Write Cycle 1 ( $\bar{W}$  Controlled)**



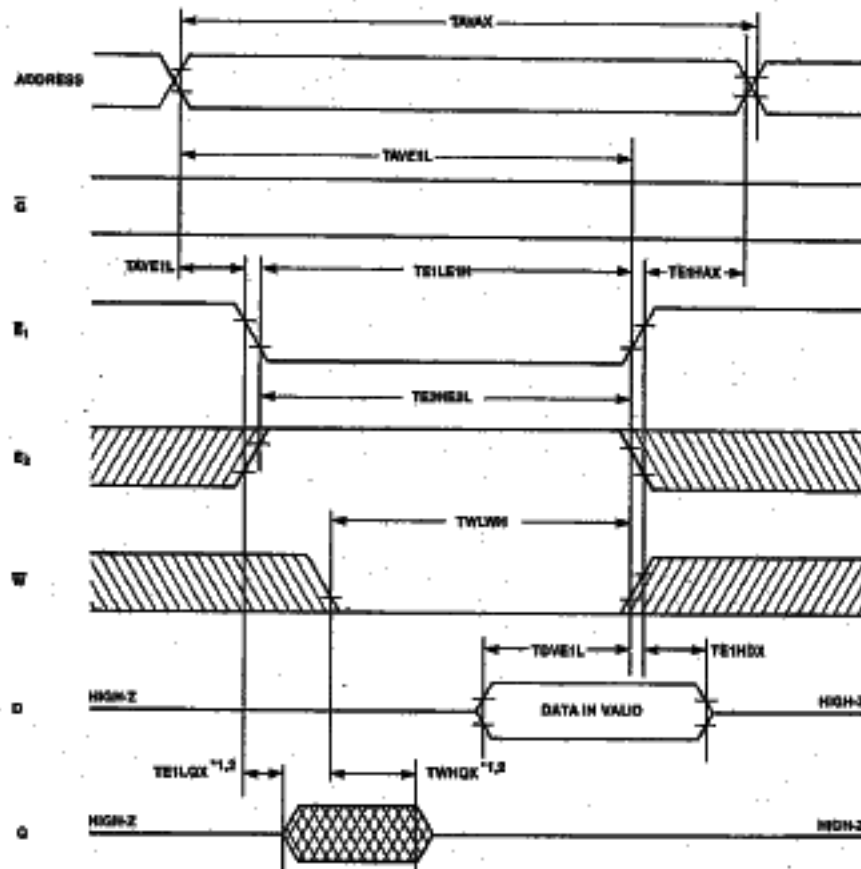
NOTE: \*1 IF  $\bar{CS}$ ,  $E_1$ , AND  $E_2$  ARE IN THE READ MODE DURING THIS PERIOD,  $DQ$  PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.  
\*2 TRANSITION IS MEASURED AT THE POINT OF  $\pm 500$  mV FROM STEADY STATE VOLTAGE.

▨ DONT CARE  
▩ UNSPINED

MB8464A-10-W  
MB8464A-15-W

**AC Characteristics**  
(Continued)  
(Recommended operating  
conditions unless otherwise  
noted)

**Write Cycle II (E<sub>1</sub> Controlled)**



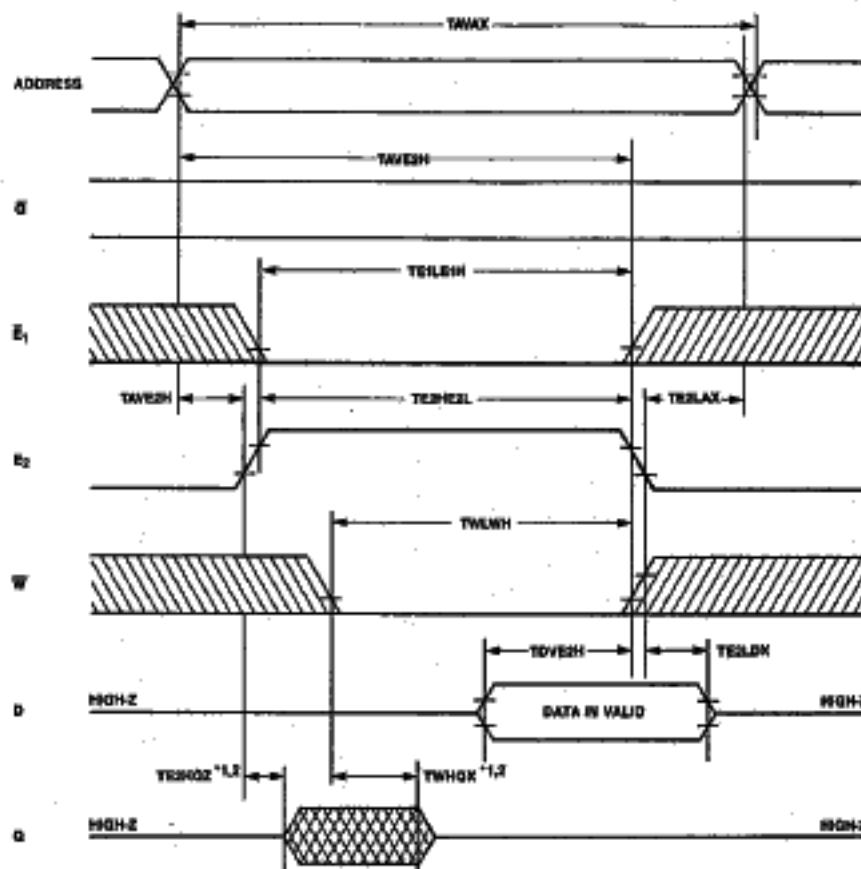
NOTE: \*1. IF G, E<sub>2</sub> AND W ARE IN THE READ MODE DURING THIS PERIOD, D,Q PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.  
\*2. TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

▨ DONT CARE  
▩ UNDERNEE

MB8464A-10-W  
MB8464A-16-W

**AC Characteristics**  
(Continued)  
(Recommended operating conditions unless otherwise noted)

**Write Cycle III (E<sub>2</sub> Controlled)**



NOTE: \*1 IF  $\bar{D}$ ,  $E_2$ , AND  $\bar{W}$  ARE IN THE READ MODE DURING THIS PERIOD,  $\bar{D}$  PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.  
\*2 TRANSITION IS MEASURED AT THE POINT OF  $\pm 500$  mV FROM STEADY STATE VOLTAGE.

▨ DONT CARE  
▩ UNDEFINED

**Data Retention Characteristics**  
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Data retention supply voltage*1	$V_{DR}$	2.0	5.5	V
Data retention supply current*2	Standard $I_{DR}$		0.5	mA
Data retention setup time	TE1HVL, TE2LVL	0		ns
Operation recovery time	TVHE1L, TVHE2H	TAVAX		

Notes: \*1 E<sub>2</sub> controlled: E<sub>2</sub> = 0.2V  
E<sub>1</sub> controlled: E<sub>1</sub> = V<sub>DR</sub> - 0.2V (E<sub>2</sub> = 0.2V or E<sub>2</sub> > V<sub>DR</sub> - 0.2V)  
\*2 E<sub>2</sub> controlled: V<sub>DR</sub> = 3.0V, E<sub>2</sub> = 0.2V  
E<sub>1</sub> controlled: V<sub>DR</sub> = 3.0V, E<sub>1</sub> = V<sub>DR</sub> - 0.3V (E<sub>2</sub> = 0.2V or E<sub>2</sub> > V<sub>DR</sub> - 0.3V)

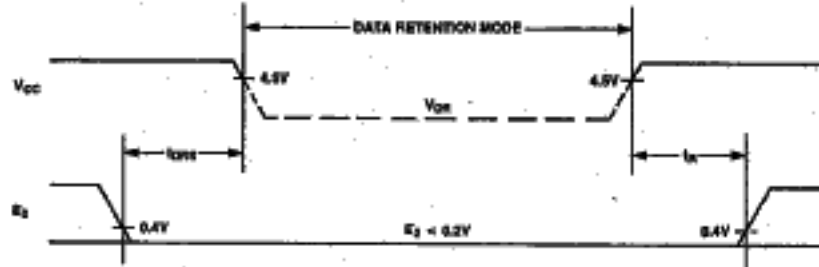


MB8464A-10-W  
MB8464A-15-W

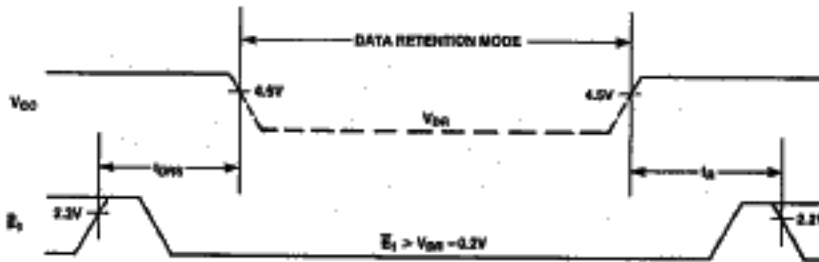
**Data Retention Characteristics**  
(Continued)  
(Recommended operating conditions unless otherwise noted)

**Data Retention Timing**

**Data Retention I ( $E_2$  Controlled)**



**Data Retention II ( $E_1$  Controlled)**

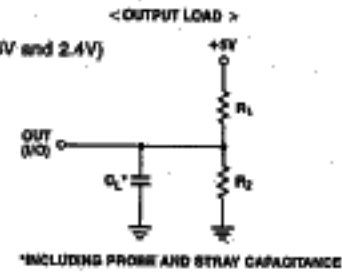


**AC Test Conditions**

Input Pulse Levels: 0.4V to 2.6V  
Input Pulse Rise and Fall Times: 5 ns (Transition time between 0.6V and 2.4V)  
Timing Reference Levels: Input:  $V_{IL} = 0.6V$ ,  $V_{IH} = 2.4V$   
Output:  $V_{OL} = 0.8V$ ,  $V_{OH} = 2.0V$

Output Load:

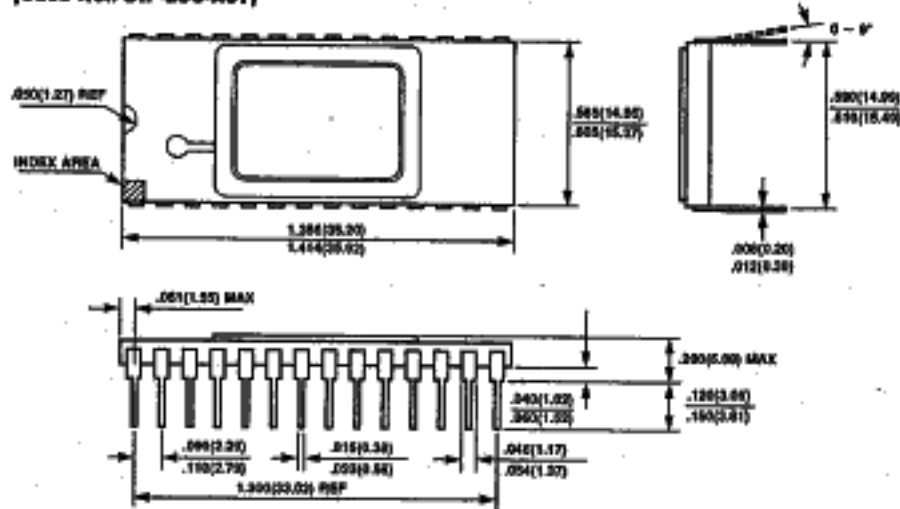
	$R_1$	$R_2$	$C_L$	PARAMETERS MEASURED
LOAD I	1.8 k $\Omega$	890 $\Omega$	100 pF	EXCEPT TEHQX, TBLGZ, TEHQZ, TQHQZ, TWHQX AND TWLQZ
LOAD II	1.8 k $\Omega$	990 $\Omega$	5 pF	TEHLQX, TOLGZ, TEHQZ, TQHQZ, TWHQX AND TWLQZ



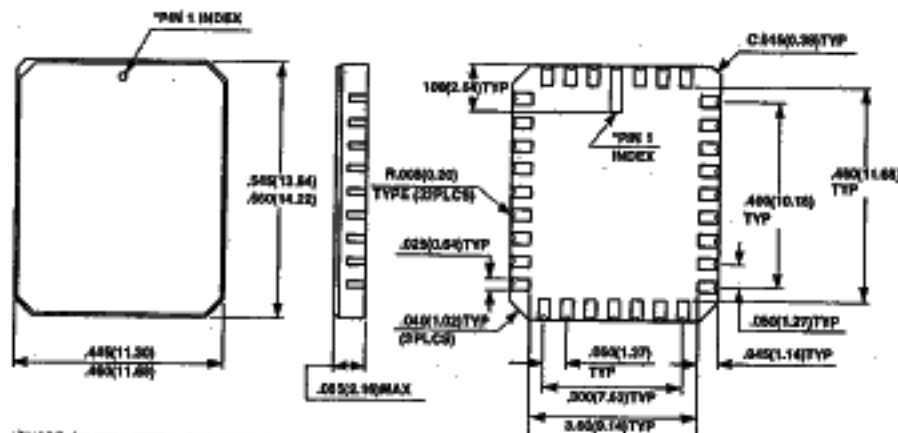
MB8464A-10-W  
MB8464A-15-W

**Package Dimensions**  
Dimensions in inches  
(millimeters)

**28-Lead Ceramic Dual-In-Line Package**  
(Case No.: DIP-28C-A07)



**32-PAD Ceramic (Metal Seal) Leadless Chip Carrier**  
(Case No. LCC-32C-A02)



MB8464A-10-W  
 MB8464A-15-W

**Package Dimensions**  
 (Continued)  
 Dimensions in inches  
 (millimeter)

**20-Lead Ceramic (Metal Seal) Dual In-Line Package  
 (Case No.: DIP-20C-A08)**

