

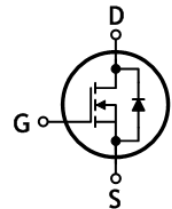
## SWITCHING REGULATOR APPLICATION

### Features

- Drain-Source breakdown voltage:  $BV_{DSS} = 500V$
- Low gate charge:  $Q_g = 46nC$  (Typ.)
- Low drain-source On resistance:  $R_{DS(on)} = 0.3\Omega$  (Max.)
- 100% avalanche tested
- RoHS compliant device

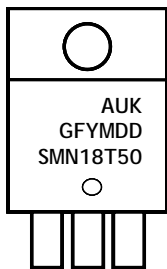
### Ordering Information

Part Number	Marking	Package
SMN18T50FD	SMN18T50	TO-220F-3L



TO-220F-3L

### Marking Information



Column 1: Manufacturer  
 Column 2: Production Information  
 e.g.) GFYMDD  
 -. G: Option Code (H: Halogen Free)  
 -. F: Factory Management Code  
 -. YMDD: Date Code (Year, Month, Date)  
 Column 3: Device Code

### Absolute maximum ratings ( $T_c = 25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	500	V	
Gate-source voltage	$V_{GSS}$	$\pm 30$	V	
Drain current (DC) *	$I_D$	$T_c = 25^\circ C$	18	A
		$T_c = 100^\circ C$	11.4	A
Drain current (Pulsed) *	$I_{DM}$	72	A	
Single pulsed avalanche energy <sup>(Note 2)</sup>	$E_{AS}$	954	mJ	
Repetitive avalanche current <sup>(Note 1)</sup>	$I_{AR}$	18	A	
Repetitive avalanche energy <sup>(Note 1)</sup>	$E_{AR}$	4.8	mJ	
Power dissipation	$P_D$	48	W	
Peak diode recovery dv/dt <sup>(Note 3)</sup>	dv/dt	4.5	V/ns	
Junction temperature	$T_J$	150	$^\circ C$	
Storage temperature range	$T_{stg}$	-55~150	$^\circ C$	

\* Drain current limited by maximum junction temperature

## Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.6	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

## Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$BV_{DSS}$	$I_D=250\mu\text{A}, V_{GS}=0$	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}, V_{DS}=V_{GS}$	2	-	4	V
Drain-source cut-off current	$I_{DSS}$	$V_{DS}=500\text{V}, V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS}=400\text{V}, T_c=125^\circ\text{C}$	-	-	10	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$	-	-	$\pm 100$	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=9\text{A}$	-	0.25	0.3	$\Omega$
Forward transfer conductance (Note 4)	$g_{fs}$	$V_{DS}=10\text{V}, I_D=9\text{A}$	-	11	-	S
Input capacitance	$C_{iss}$	$V_{DS}=25\text{V}, V_{GS}=0\text{V}, f=1.0\text{MHz}$	-	3405	4643	pF
Output capacitance	$C_{oss}$		-	283	386	
Reverse transfer capacitance	$C_{rss}$		-	10.6	17	
Turn-on delay time (Note 4,5)	$t_{d(on)}$	$V_{DD}=250\text{V}, I_D=18\text{A}, R_G=25\Omega$	-	78	-	ns
Rise time (Note 4,5)	$t_r$		-	72	-	
Turn-off delay time (Note 4,5)	$t_{d(off)}$		-	184	-	
Fall time (Note 4,5)	$t_f$		-	68	-	
Total gate charge (Note 4,5)	$Q_g$	$V_{DS}=400\text{V}, V_{GS}=10\text{V}, I_D=18\text{A}$	-	46	62	nC
Gate-source charge (Note 4,5)	$Q_{gs}$		-	14	-	
Gate-drain charge (Note 4,5)	$Q_{gd}$		-	8.5	-	

## Source-Drain Diode Ratings and Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

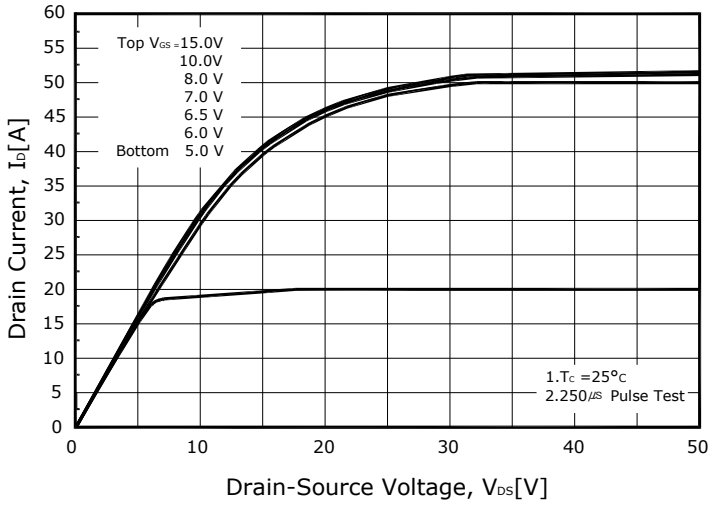
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_S$	Integral reverse diode in the MOSFET	-	-	18	A
Source current (Pulsed)	$I_{SM}$		-	-	72	A
Forward voltage	$V_{SD}$	$V_{GS}=0\text{V}, I_S=18\text{A}$	-	-	1.5	V
Reverse recovery time (Note 4,5)	$t_{rr}$	$I_S=18\text{A}, V_{GS}=0\text{V}, di_f/dt=100\text{A}/\mu\text{s}$	-	360	-	ns
Reverse recovery charge (Note 4,5)	$Q_{rr}$		-	4.1	-	$\mu\text{C}$

Note:

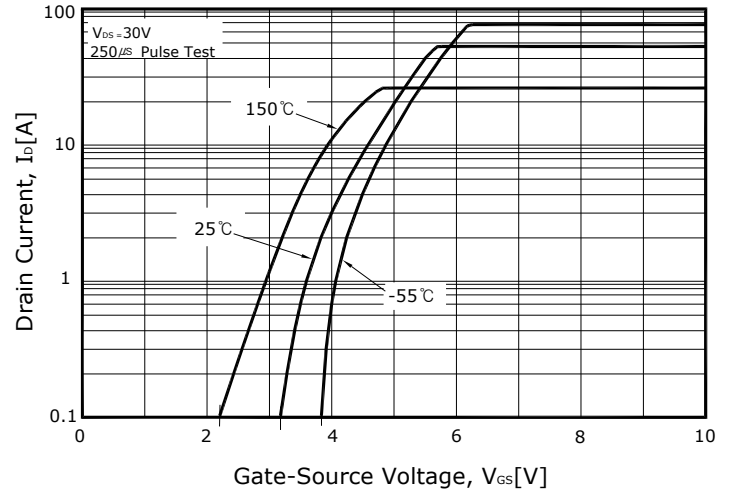
1. Repeated rating: Pulse width limited by safe operating area
2.  $L=5.3\text{mH}, I_{AS}=18\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
3.  $I_S \leq 18\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J=25^\circ\text{C}$
4. Pulse test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature typical characteristics

## Electrical Characteristics Curve

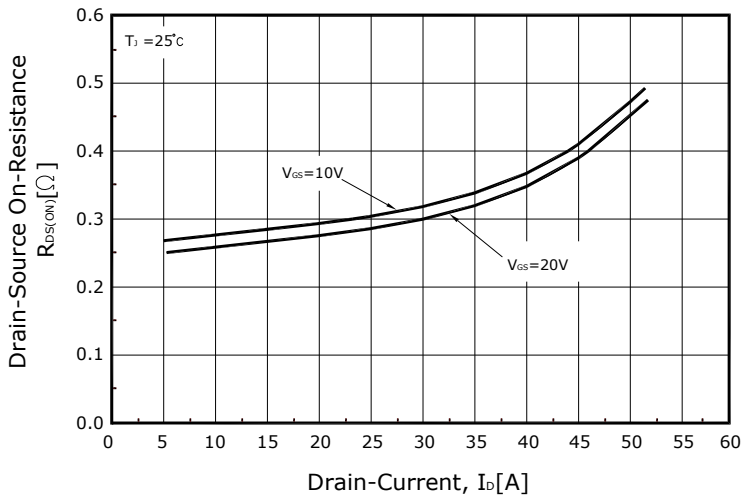
**Fig. 1  $I_D - V_{DS}$**



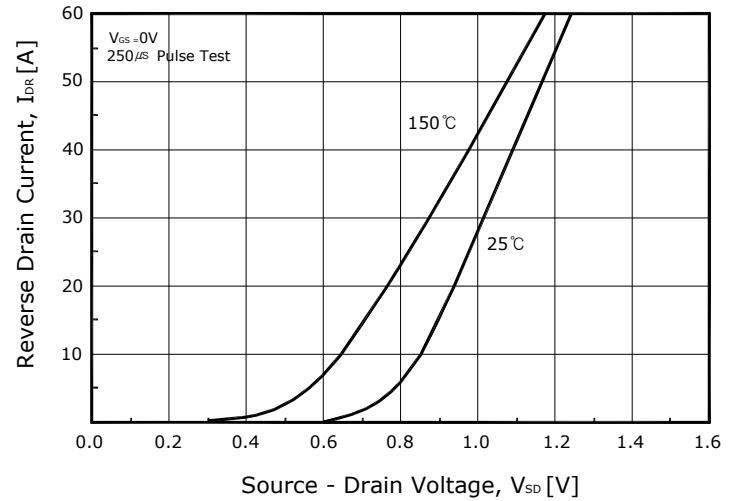
**Fig. 2  $I_D - V_{GS}$**



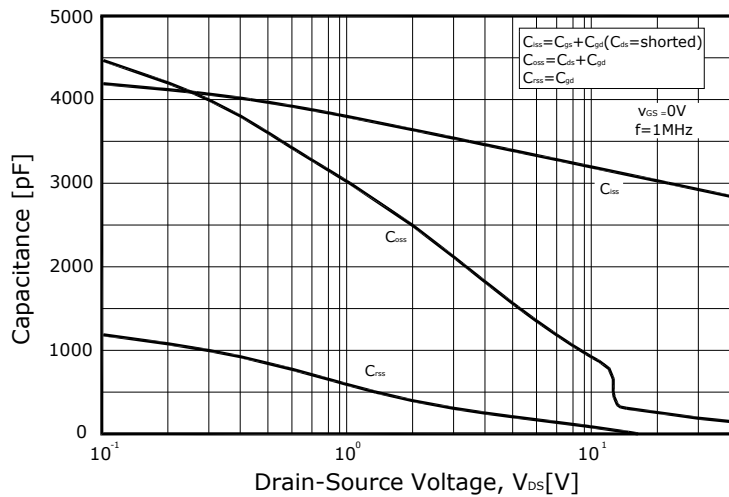
**Fig. 3  $R_{DS(ON)} - I_D$**



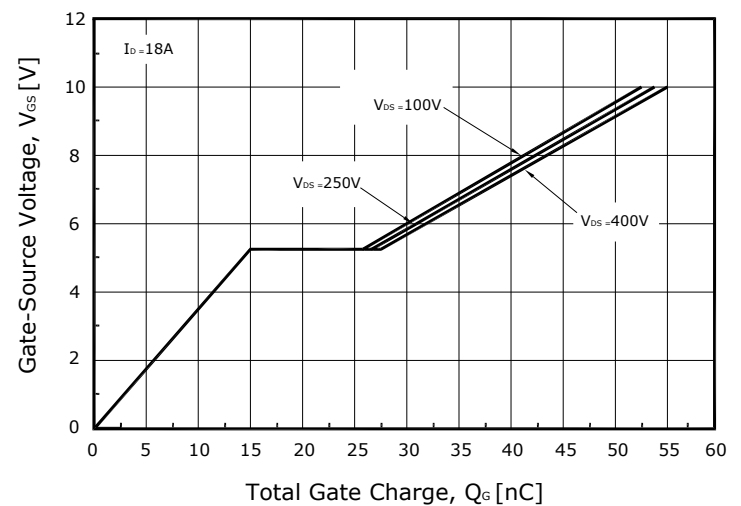
**Fig. 4  $I_{DR} - V_{SD}$**



**Fig. 5 Capacitance -  $V_{DS}$**



**Fig. 6  $V_{GS} - Q_G$**



## Electrical Characteristics Curve (Continue)

Fig. 7  $BV_{DSS} - T_J$

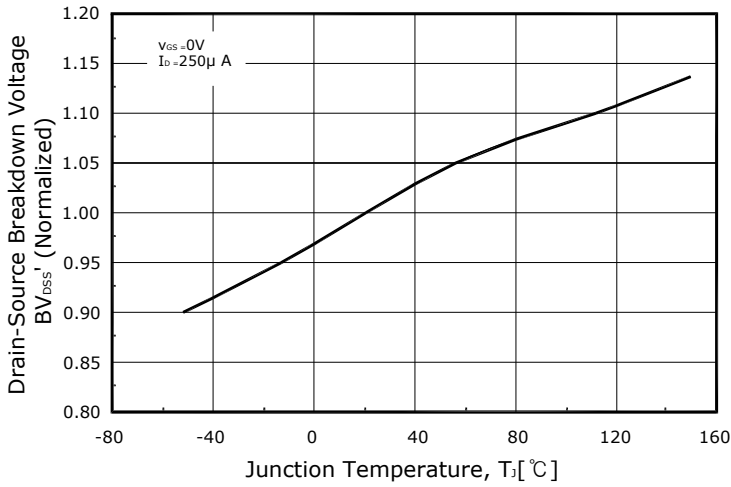


Fig. 8  $R_{DS(ON)} - T_J$

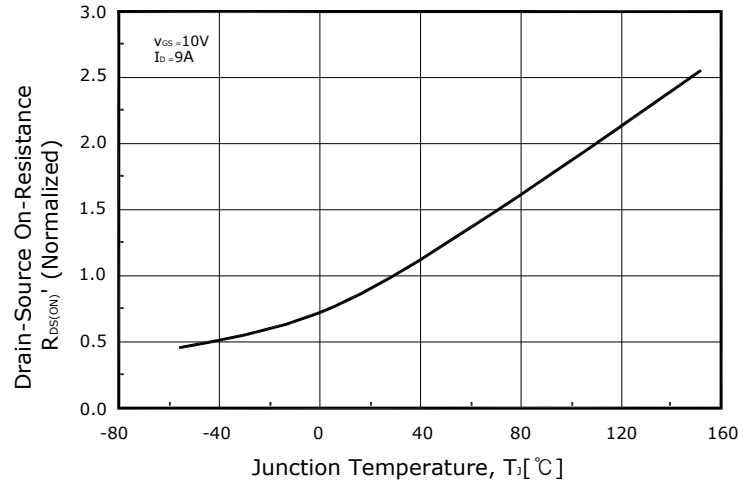


Fig. 9  $I_D - T_C$

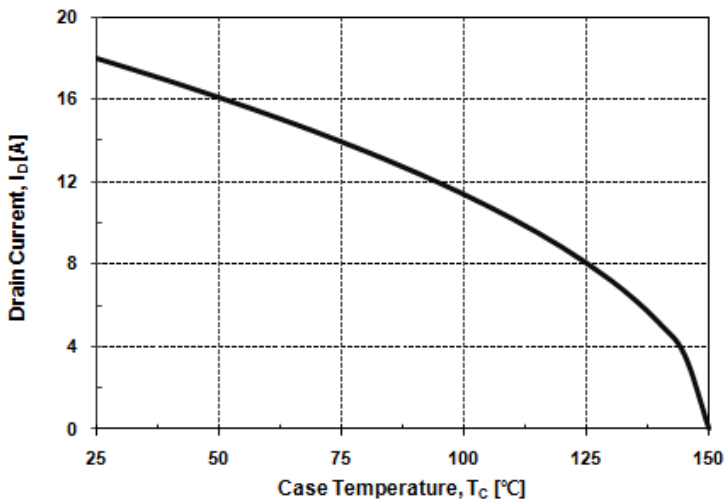


Fig. 10 Safe Operating Area

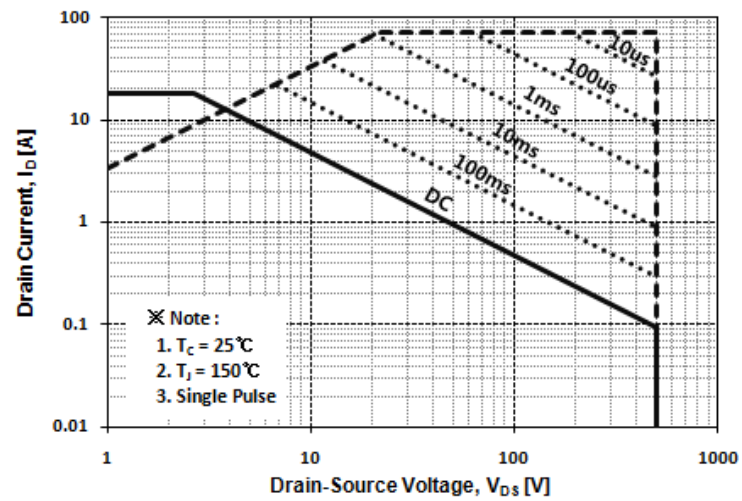
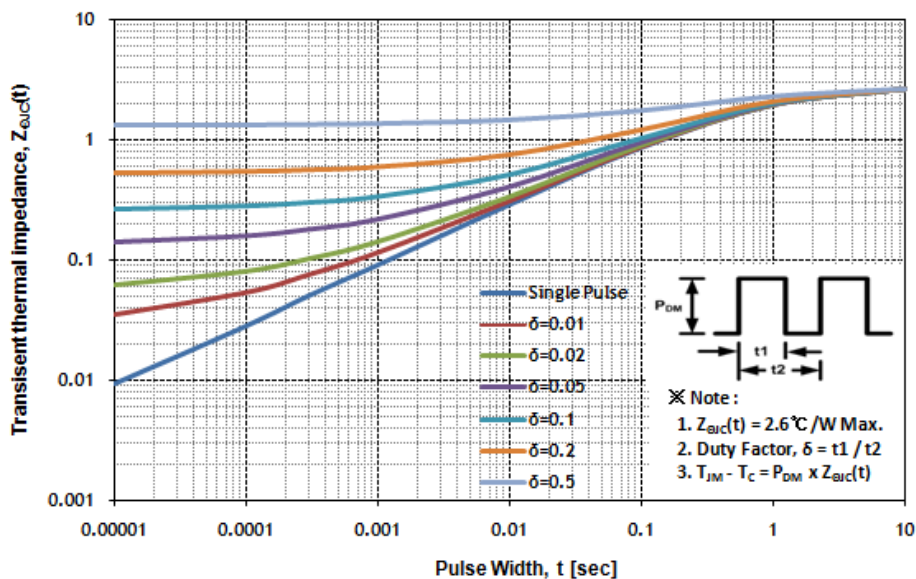
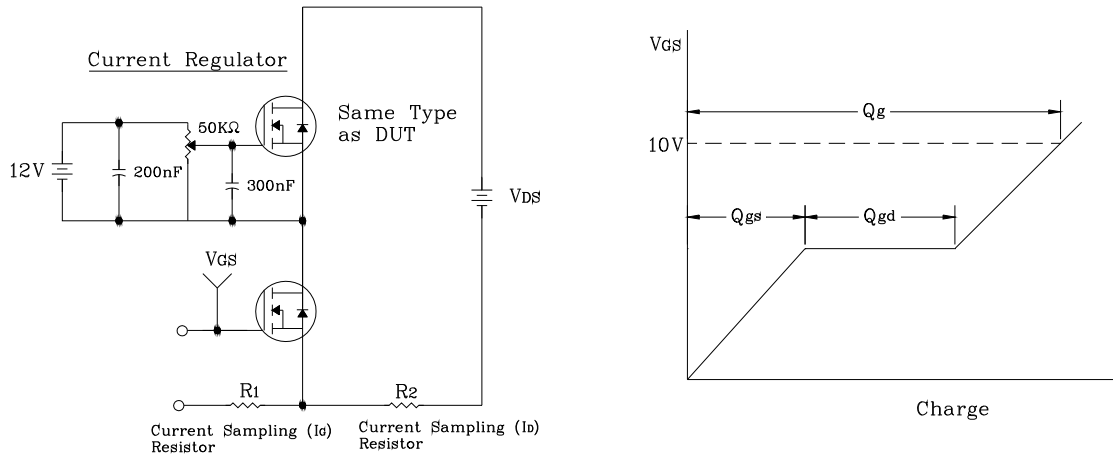


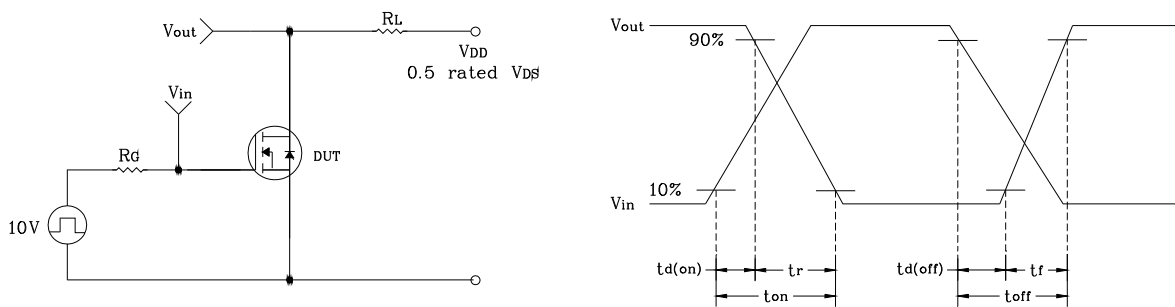
Fig. 11 Transient Thermal Impedance



**Fig. 12 Gate Charge Test Circuit & Waveform**



**Fig. 13 Resistive Switching Test Circuit & Waveform**



**Fig. 14 E<sub>AS</sub> Test Circuit & Waveform**

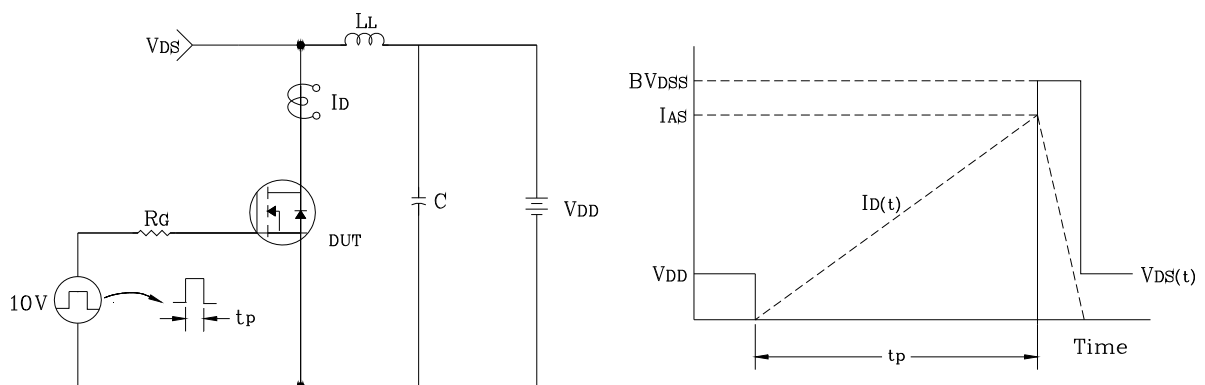
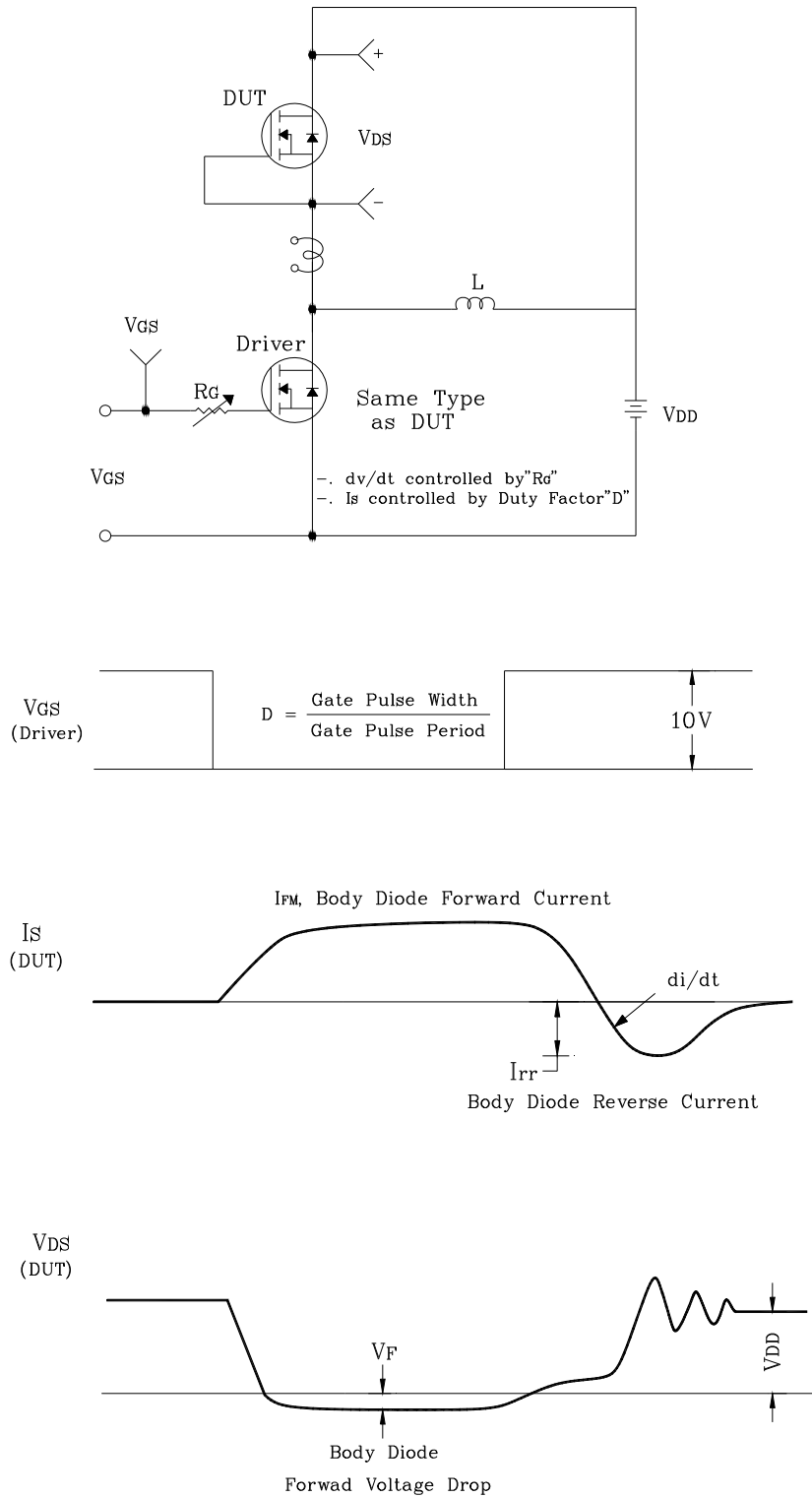
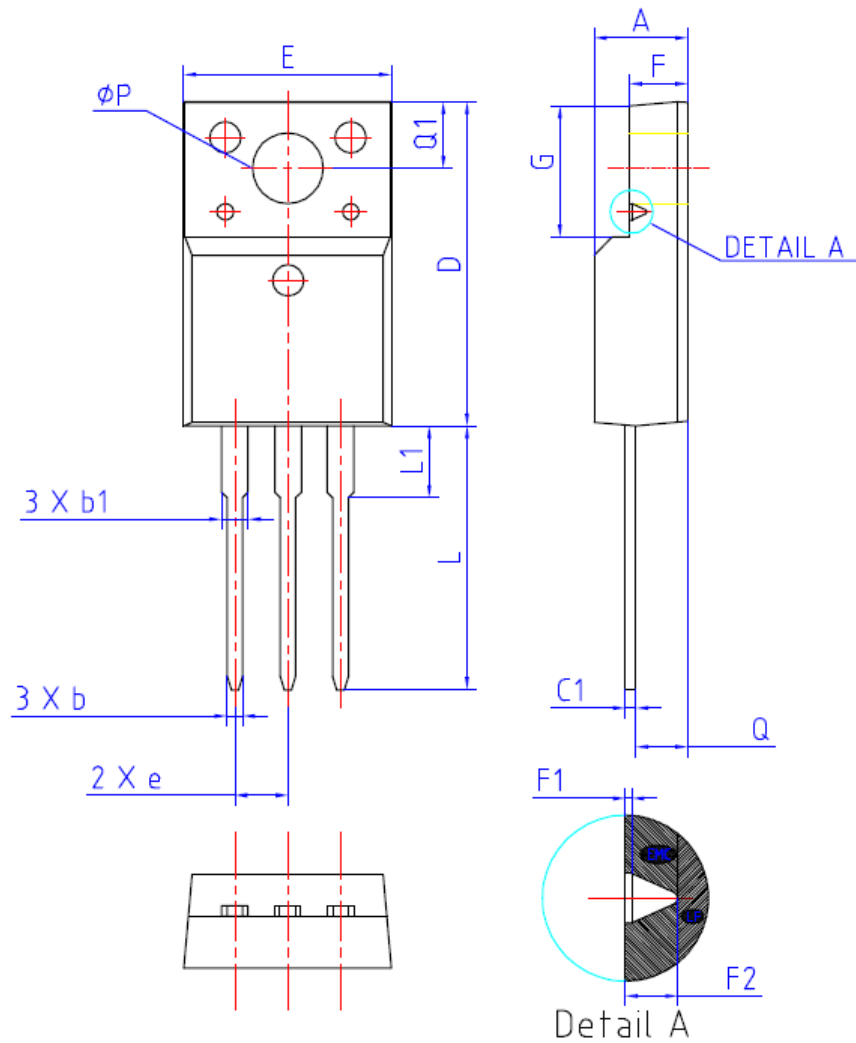


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



## Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	4.50	4.70	4.90	
b	0.70	0.80	0.90	
b1	1.33	1.40	1.47	
C1	0.45	0.50	0.60	
D	15.67	15.87	16.07	
E	9.96	10.16	10.36	
e	2.54BSC			
F	2.34	2.54	2.74	
F1	(0.10 REF)			
F2	(0.84 REF)			
G	6.48	6.68	6.88	
L	12.78	12.98	13.18	
L1	3.03	3.23	3.43	
Q	2.56	2.76	2.96	
Q1	3.10	3.30	3.50	
$\phi P$	3.08	3.18	3.28	

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