

### RLSD92A031~121V/C Series

LOW CAPACITANCE TVS/ESD ARRAY

# **Description**

The RLSD92AXX1X is designed to protect voltage sensitive components from ESD and transient voltage events. Excellent clamping capability, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its small size, it is suited for use in cellular phones, MP3 players, digital cameras and many other portable applications where board space is at a premium.

### **Features**

- Transient protection for data lines to IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact) IEC 61000-4-4 (EFT) 40A (tp = 5/50ns)
   Cable Discharge Event (CDE)
- Ultra-small package (1.0 x 0.6 x 0.5mm)
- Protects one data or I/O line
- · Low capacitance:
- · Low clamping voltage
- Solid-state silicon-avalanche technology

# **Applications**

- Cellular phones audio
- MP3 players
- · Digital cameras
- Portable applicationss
- obile telephone

### **Mechanical Characteristics**

- Molding compound flammability rating: UL 94V-0
- Marking: Marking code
- · Packaging : Tape and Reel
- · Lead Finish: NiPdAu
- RoHS/WEEE Compliant

# Pin Configuration 1 2 C Series V Series

# **Maximum Ratings**

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P <sub>PK</sub>	100	Watts
Peak Pulse Current (tp = 8/20µs)	Ірр	4	Α
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V <sub>ESD</sub>	±15 ±8	kV
Operating Temperature	TJ	-55 to +125	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

# **Electrical Characteristics (T=25°C)**

### RLSD92A031C/RLSD92A031V

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>	-	-	-	3.3	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> =1mA	5.0	-	-	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 3.3V, T=25°C	-	-	1	μΑ
Total Capacitance	CJ	V <sub>R</sub> = 0V, f = 1MHz	-	-	40/80	pF
Max Reverse Peak Pulse Current	Ірр	-	-	-	9.8	Α
Clamping Voltage @lpp	Vc	-	-	-	10.4	V

### RLSD92A051C/RLSD92A051V

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>	-	-	-	5	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> =1mA	6.2	-	-	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 5V, T=25°C	-	-	1	μΑ
Total Capacitance	CJ	V <sub>R</sub> = 0V, f = 1MHz	-	-	30/65	pF
Max Reverse Peak Pulse Current	Ірр	-	-	-	8.7	Α
Clamping Voltage @lpp	Vc	-	-	-	12.3	V

# RLSD92A071C/RLSD92A071V

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>	-	-	-	7	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> =1mA	9.5	-	-	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 7V, T=25°C	-	-	1	μΑ
Junction Capacitance	CJ	V <sub>R</sub> = 0V, f = 1MHz	-	-	25/50	pF
Max Reverse Peak Pulse Current	Ірр	-	-	-	8.2	Α
Clamping Voltage @lpp	Vc	-	-	-	12.2	V

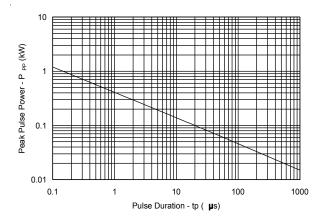
### RLSD92A121C/RLSD92A121V

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>	-	-	-	12	V
Reverse Breakdown Voltage	V <sub>BR</sub>	I <sub>t</sub> =1mA	13.3	-	-	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 12V, T=25°C	-	-	1	μΑ
Junction Capacitance	CJ	V <sub>R</sub> = 0V, f = 1MHz	-	-	15/30	pF
Max Reverse Peak Pulse Current	Ірр	-	-	-	5.9	Α
Clamping Voltage @lpp	Vc	-	-	-	23.7	V

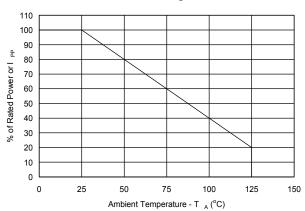
# **Protection Products**

# **Typical Characteristics**

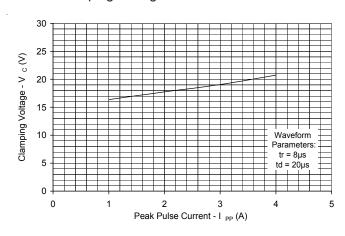
Non-Repetitive Peak Pulse Power vs. Pulse Time



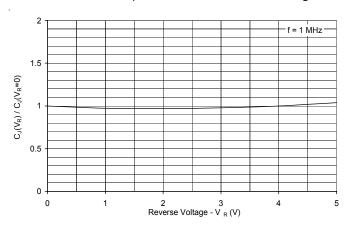
Power Derating Curve



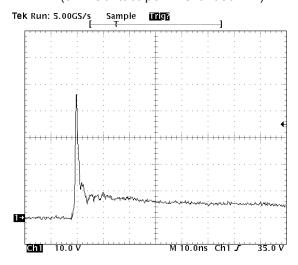
Clamping Voltage vs. Peak Pulse Current



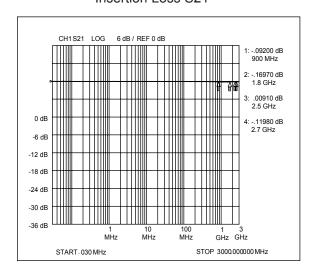
Normalized Capacitance vs. Reverse Voltage



ESD Clamping (8kV Contact per IEC 61000-4-2)



Insertion Loss S21



# **Protection Products**

# **Applications Information**

**Device Connection Options** 

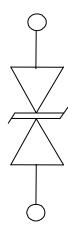
These low capacitance TVS diodes are designed to provide common mode protection for one high-speed line or differential protection for one line pair. The device is bidirectional and may be used on lines where the signal polarity is positive and negative.

Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible. Equivalent Circuit Diagram

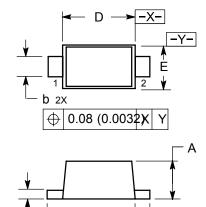
### **Equivalent Circuit Diagram**



# PROTECTION PRODUCTS

# **Outline Drawing**

SOD-923



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### NOTES:

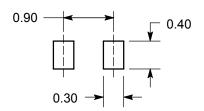
- 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETERS.

  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MIL	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.34	0.37	0.40	0.013	0.015	0.016	
b	0.15	0.20	0.25	0.006	0.008	0.010	
С	0.07	0.12	0.17	0.003	0.005	0.007	
D	0.75	0.80	0.85	0.030	0.031	0.033	
Е	0.55	0.60	0.65	0.022	0.024	0.026	
HE	0.95	1.00	1.05	0.037	0.039	0.041	
L	0.05	0.10	0.15	0.002	0.004	0.006	

### **SOLDERING FOOTPRINT\***



**DIMENSIONS: MILLIMETERS** 

# **Protection Products**

# **Ordering Information**

Part Number	Qty per Reel	Reel Size
RLSD92AXX1X	8,000	

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