DOCUMENT NUMBER AND REVISION

FS-TJ028A02-03 REV. A

(240320W2HEG12SP)

DOCUMENT TITLE:

SPECIFICATION

OF

LCD MODULE TYPE

CUSTOMER	
MODEL NUMBER	**TJ028A02-03**
CUSTOMER APPROVAL	
DATE	

DEPARTMENT	NAME	SIGNATURE	DATE
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DOCUMENT REVISION HISTORY 1:

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A	2007.11.19	First Release.	LIANG YUN	JIANG WEN RONG

CONTENTS

Specification of LCD Module Type
Item No.: TJ028A02-03

1. General Description

- 240(RGB) x 320 2.83'' TFT Transmissive normal black Matrix LCD Module.
- Viewing Angle: 12 O'clock direction.
- 'Sunplus' SPFD5408 LCD Controller &Driver or equivalent (COG type)
- Power Supply: +2.8V.
- Interface type: FPC
- White backlight. (Side LED)

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	49.6(L) ×69.15 (W) × 3.45 (H) (Exclude FPC) 49.6(L) ×98.37 (W) × 3.45 (H) (Include FPC)	mm
Active area	43.2(L) ×57.6(W)	mm
Display format	240(RGB) × 320	dots
Pixel pitch	0.18(V) × 0.18(H)	mm

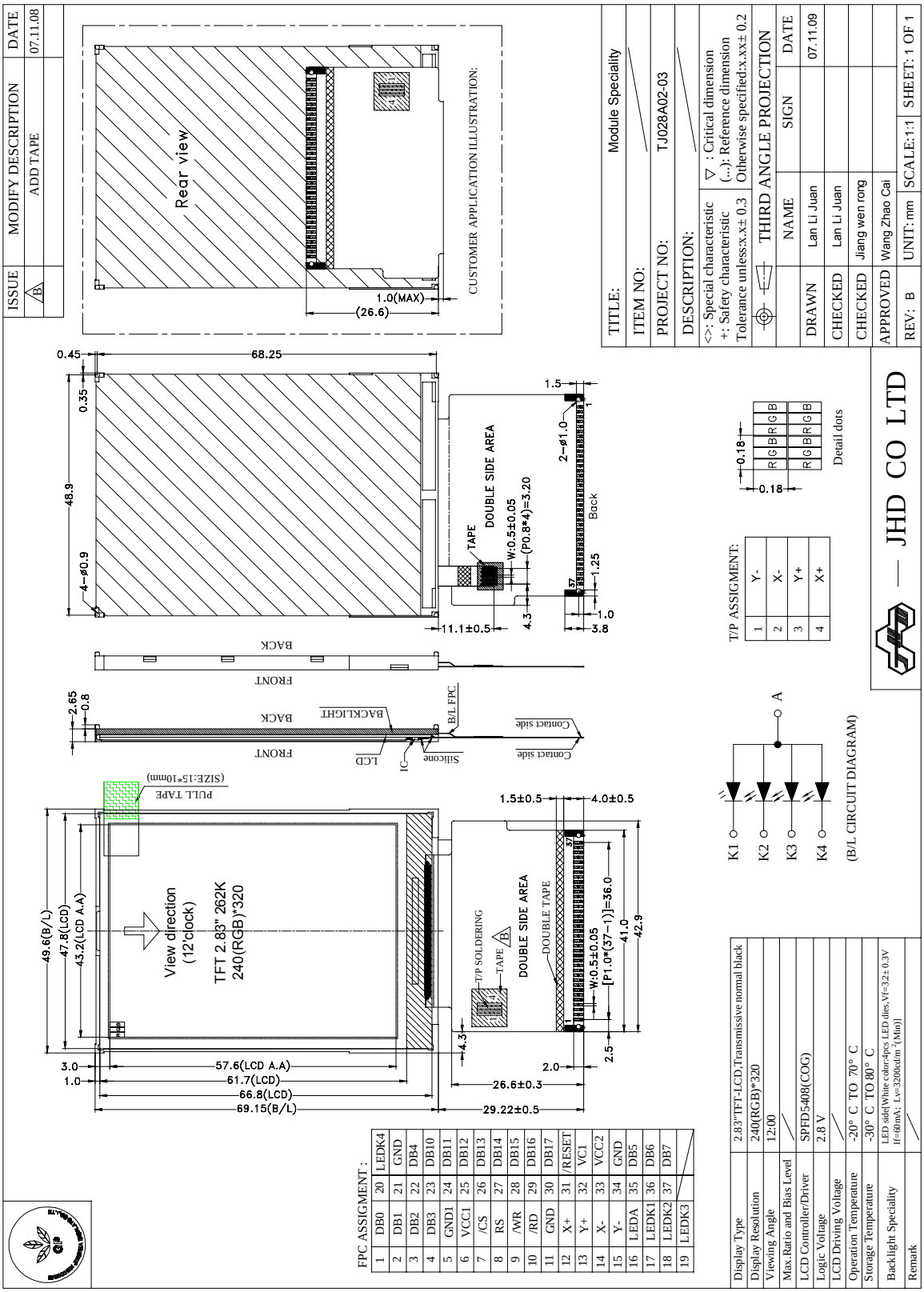

Figure 1: Module Specification

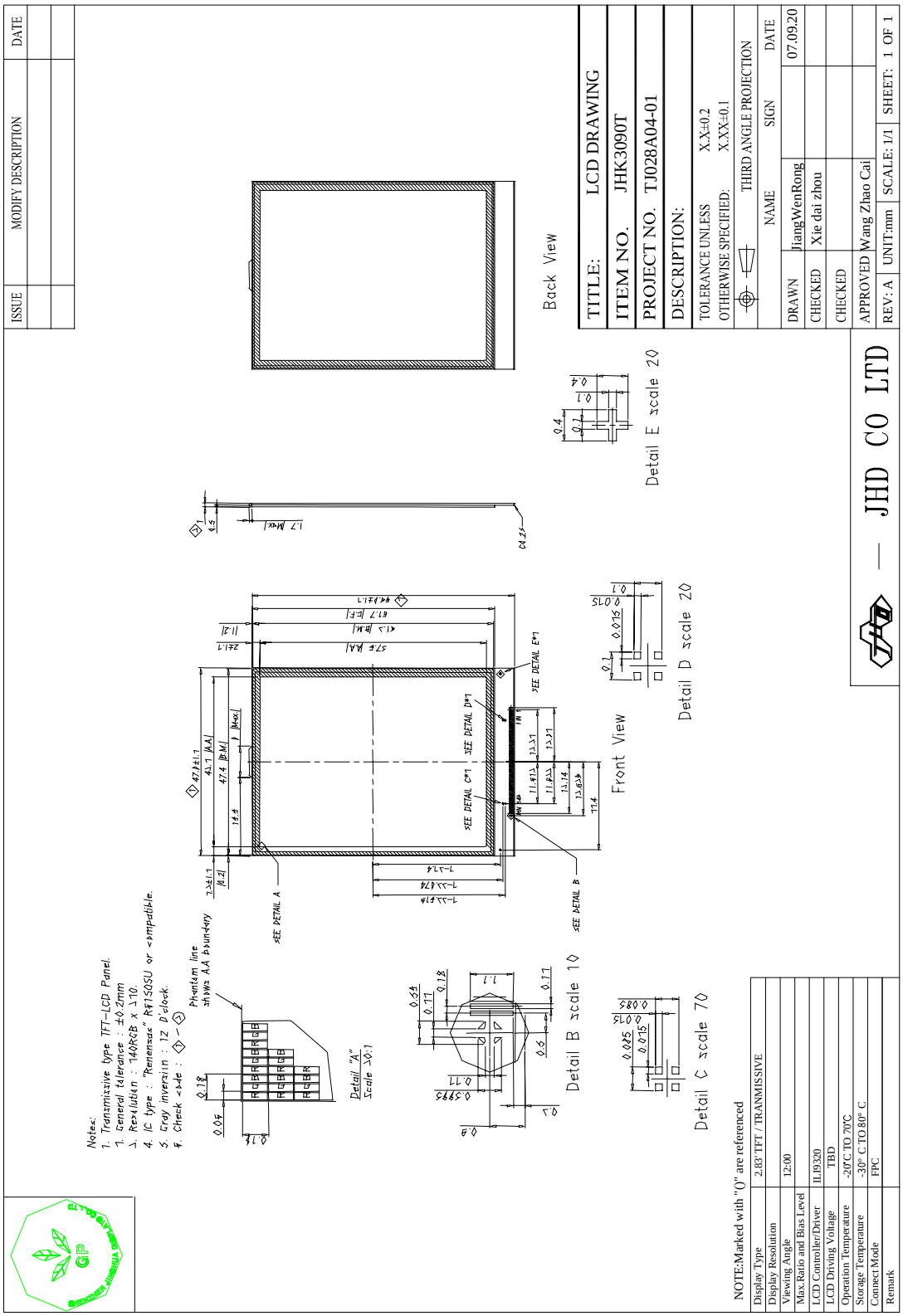

Figure 2: LCD Specification

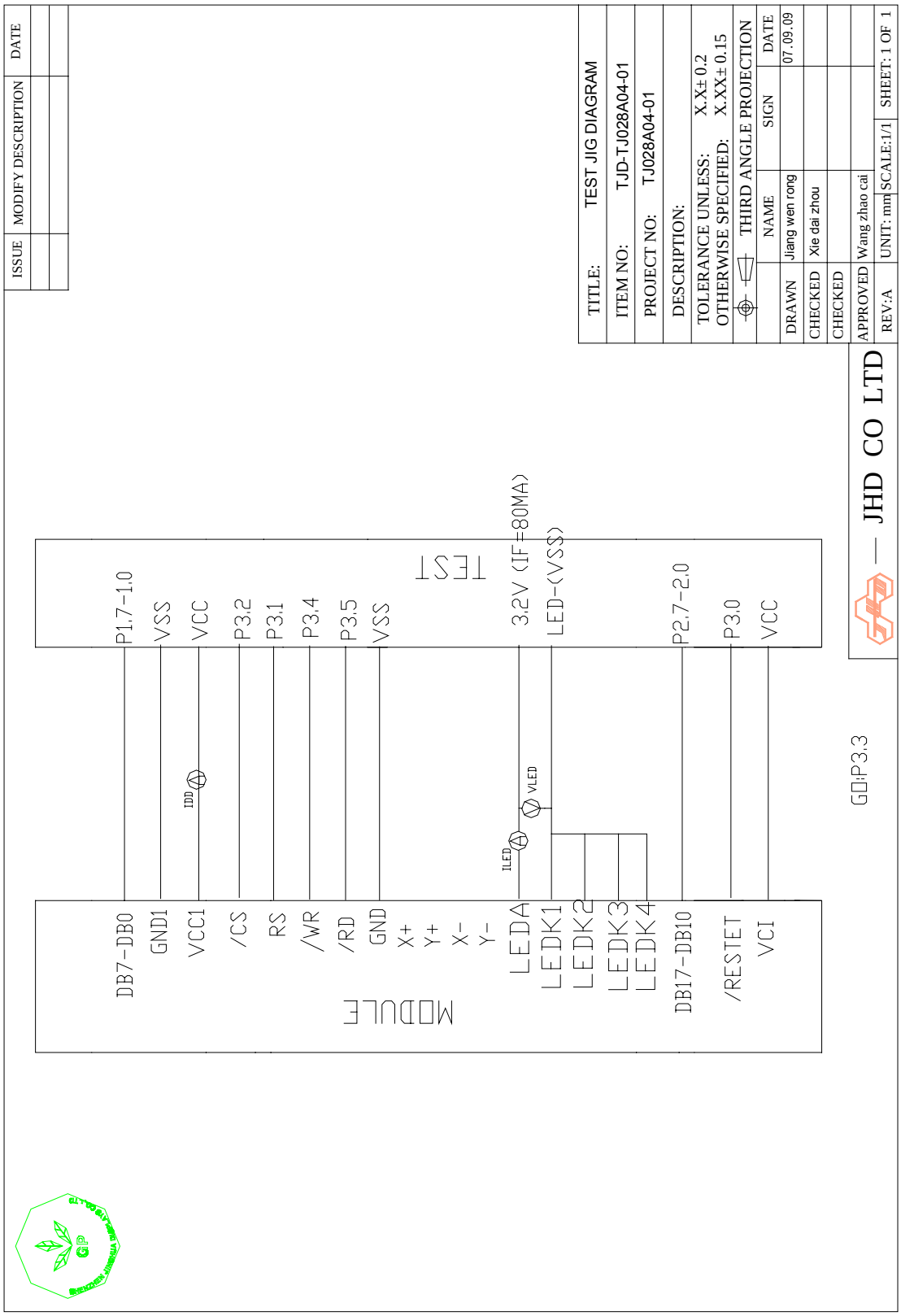

Figure 3: Recommend the power supply for circuit

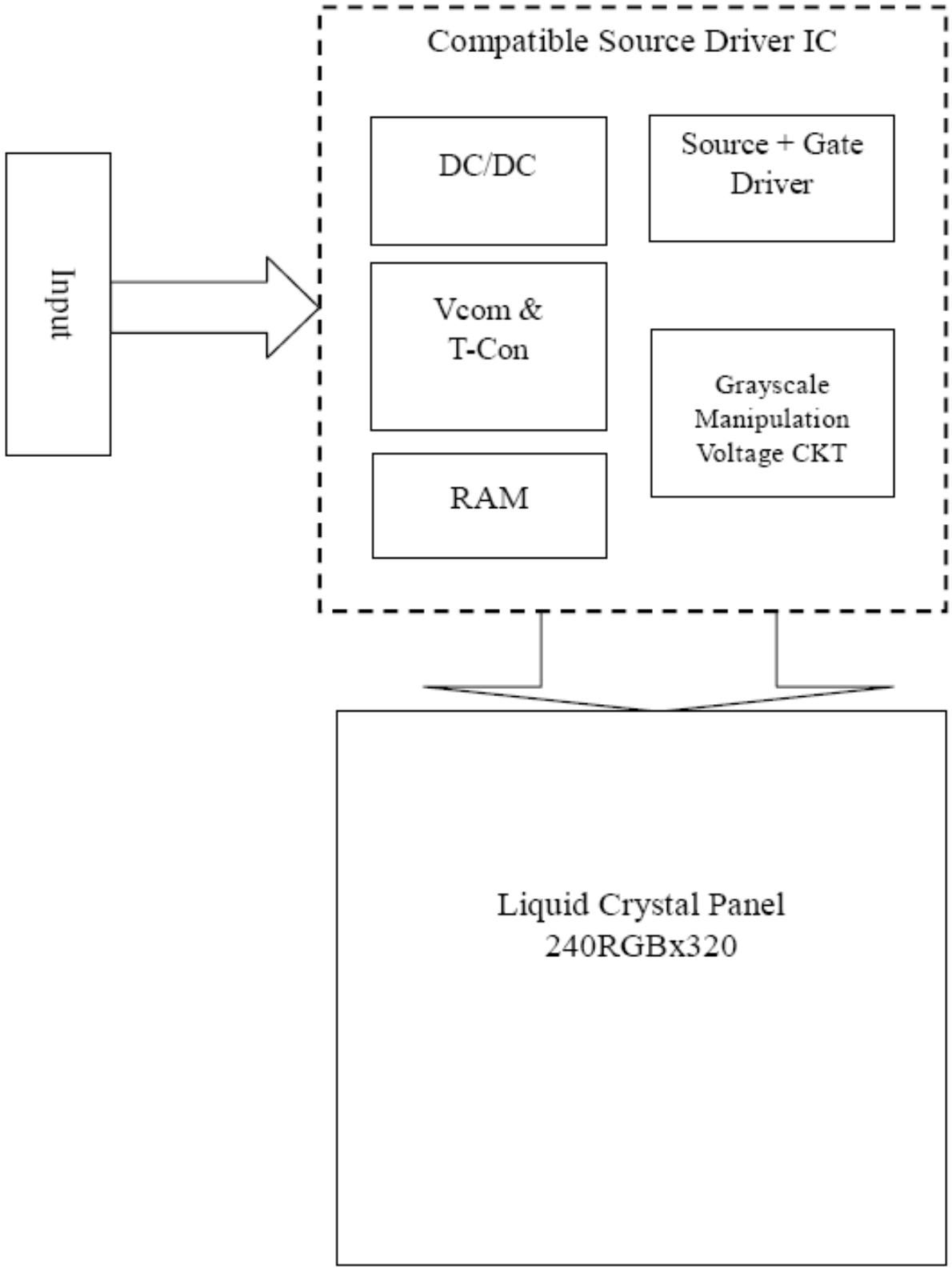

Figure 4: Block diagram

3. Interface signals

Table 2(a) for FPC

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>DB0</td><td rowspan="4">Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
<table>
<tr><th>Mode</th><th>Pin Assignment</th></tr>
<tr><td>8-bit system interface</td><td>DB17-DB10</td></tr>
<tr><td>9-bit system interface</td><td>DB17-DB9</td></tr>
<tr><td>16-bit system interface</td><td>DB17-DB10, DB8-DB1</td></tr>
<tr><td>18-bit system interface</td><td>DB17-DB0</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB12</td></tr>
<tr><td>16-bit External (RGB) interface</td><td>DB17-10, DB8-DB1</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB0</td></tr>
</table>
Must connect to the GND or IOVCC level when not in use.
These pins have weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.</td></tr>
<tr><td>2</td><td>DB1</td></tr>
<tr><td>3</td><td>DB2</td></tr>
<tr><td>4</td><td>DB3</td></tr>
<tr><td>5</td><td>GND1</td><td>Ground.</td></tr>
<tr><td>6</td><td>VCC1</td><td>Internal logic power.</td></tr>
<tr><td>7</td><td>/CS</td><td>Chip select signal.
Low: the SPFD5408A is accessible
High: the SPFD5408A is not accessible Must connect to the GND or IOVCC level when not used.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.</td></tr>
<tr><td>8</td><td>RS</td><td>Used as register selection input.
When RS = "High", Data register is selected.
When RS = "Low", Instruction register is selected.</td></tr>
<tr><td>9</td><td>/WR</td><td>(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low.
(B) In SPI mode, served as a synchronizing clock signal.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.</td></tr>
<tr><td>10</td><td>/RD</td><td>In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low.
Must connect to the GND or IOVCC level when not in use.
This pin has weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.</td></tr>
<tr><td>11</td><td>GND</td><td>Ground.</td></tr>
<tr><td>12</td><td>X+</td><td>Connect to the right of Touch Panel.</td></tr>
<tr><td>13</td><td>Y+</td><td>Connect to the top of Touch Panel.</td></tr>
<tr><td>14</td><td>X-</td><td>Connect to the left of Touch Panel.</td></tr>
<tr><td>15</td><td>Y-</td><td>Connect to the bottom of Touch Panel.</td></tr>
</table>

Table 2(a) for FPC

<table>
<tr><td>16</td><td>LEDA</td><td>Anode of the backlight.</td></tr>
<tr><td>17</td><td>LEDK1</td><td rowspan="4">Cathode of the backlight.</td></tr>
<tr><td>18</td><td>LEDK2</td></tr>
<tr><td>19</td><td>LEDK3</td></tr>
<tr><td>20</td><td>LEDK4</td></tr>
<tr><td>21</td><td>GND</td><td>Ground.</td></tr>
<tr><td>22</td><td>DB4</td><td rowspan="9">Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
<table>
<tr><th>Mode</th><th>Pin Assignment</th></tr>
<tr><td>8-bit system interface</td><td>DB17-DB10</td></tr>
<tr><td>9-bit system interface</td><td>DB17-DB9</td></tr>
<tr><td>16-bit system interface</td><td>DB17-DB10, DB8-DB1</td></tr>
<tr><td>18-bit system interface</td><td>DB17-DB0</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB12</td></tr>
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<tr><td>18-bit External (RGB) interface</td><td>DB17-DB0</td></tr>
</table>
Must connect to the GND or IOVCC level when not in use.
These pins have weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.</td></tr>
<tr><td>23</td><td>DB10</td></tr>
<tr><td>24</td><td>DB11</td></tr>
<tr><td>25</td><td>DB12</td></tr>
<tr><td>26</td><td>DB13</td></tr>
<tr><td>27</td><td>DB14</td></tr>
<tr><td>28</td><td>DB15</td></tr>
<tr><td>29</td><td>DB16</td></tr>
<tr><td>30</td><td>DB17</td></tr>
<tr><td>31</td><td>/RESET</td><td>RESET pin. This is an active low signal.</td></tr>
<tr><td>32</td><td>VC1</td><td>Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.</td></tr>
<tr><td>33</td><td>VCC2</td><td>Internal logic power.</td></tr>
<tr><td>34</td><td>GND</td><td>Ground.</td></tr>
<tr><td>35</td><td>DB5</td><td rowspan="3">Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
<table>
<tr><th>Mode</th><th>Pin Assignment</th></tr>
<tr><td>8-bit system interface</td><td>DB17-DB10</td></tr>
<tr><td>9-bit system interface</td><td>DB17-DB9</td></tr>
<tr><td>16-bit system interface</td><td>DB17-DB10, DB8-DB1</td></tr>
<tr><td>18-bit system interface</td><td>DB17-DB0</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB12</td></tr>
<tr><td>16-bit External (RGB) interface</td><td>DB17-10, DB8-DB1</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB0</td></tr>
</table>
Must connect to the GND or IOVCC level when not in use.
These pins have weak pull high/low resistors and can be modified to high / low by metal layer change for customer's request.</td></tr>
<tr><td>36</td><td>DB6</td></tr>
<tr><td>37</td><td>DB7</td></tr>
</table>

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings (Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	V_{DD}, V_{CC}, IOVCC,	-0.3	+4.6	V
Power Supply voltage (Logic)	VCI-AGND	-0.3	+4.6	V
Power Supply voltage	DDVDH-AGND	-0.3	+6.5	V
Power Supply voltage	DDVDH-VCL	-0.3	+9.0	V
Power Supply voltage	AGND-VGL	-0.3	+14.0	V
Power Supply voltage	V_{GH}-V_{GL}	-0.3	+30.0	V
Input Voltage	V_{IN}	-0.3	IOVCC+0.3	V

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry

5. Electrical Specifications

5.1 Typical Electrical Characteristics

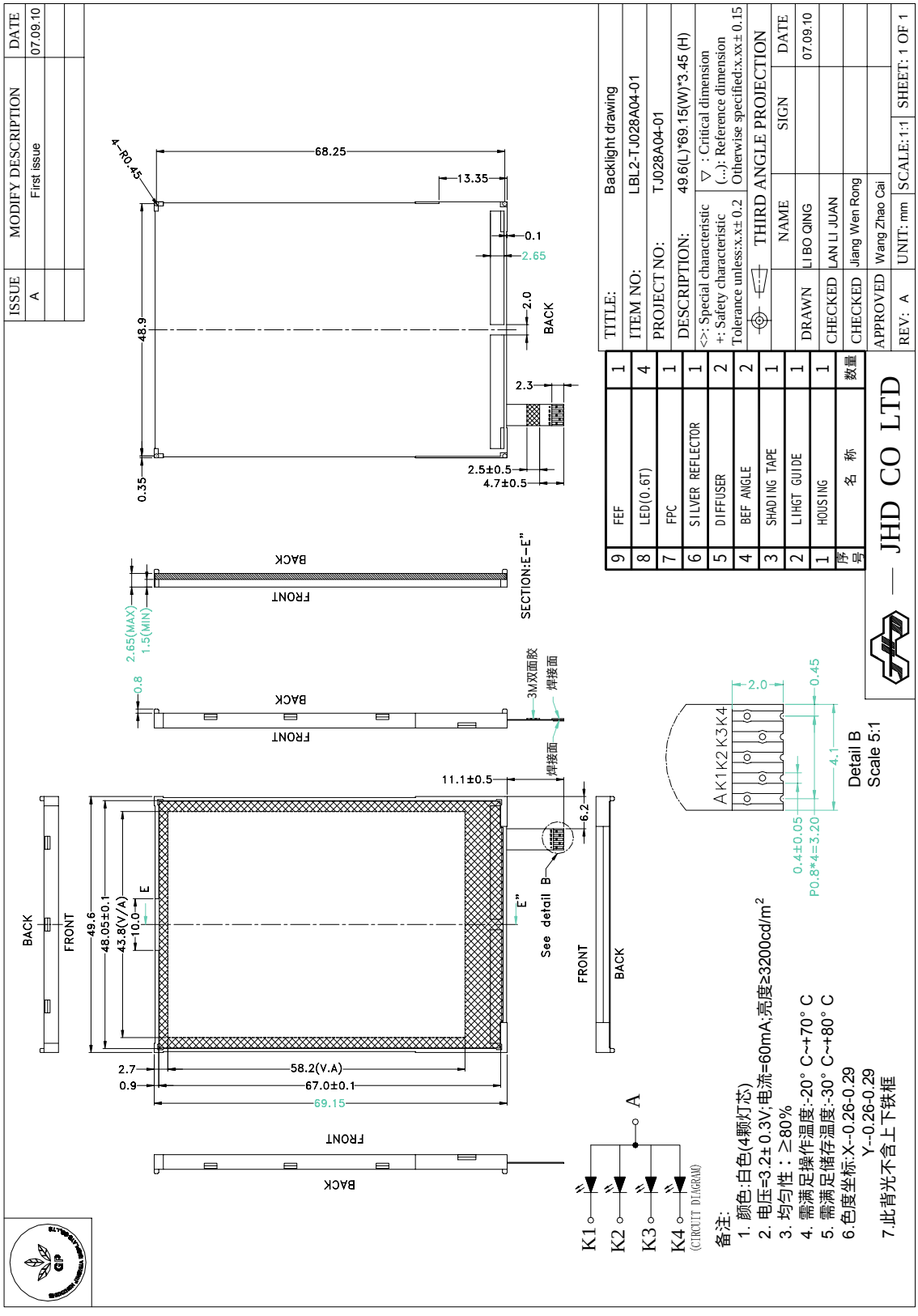
At Ta = 25 °C, V_{DD} = 2.8±0.1V, V_{SS}=0V,Vcc=2.50V~3.30V, IOVCC=1.65V~3.30V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}	-	2.7	2.8	2.9	V
Supply voltage (LCD)	V_{LCD}=V_{EE}-V_{SS}	V_{DD}=+2.8V, Note 1	-	-	-	V
Input Level voltage	V_{IH}	IOVCC＝ 1.65V~3.30V	0.8xIOVCC	-	IOVCC	V
	V_{IL}	IOVCC＝ 1.65V~3.30V	-0.3	-	0.2xIOVCC	V
Input Level voltage	V_{OH}	IOVCC＝ 1.65V~3.30V I_{OH}=-0.1mA	0.8xIOVCC	-	-	V
	V_{OL}	IOVCC＝ 1.65V~3.30V I_{OL}=0.1mA	-	-	0.2xIOVCC	V
Supply Current (Logic)	I_{DD}	Note 1	-	7.5	11.25	mA
Supply voltage for Backlight	V_{LED}	Forward current-60mA	2.9	3.2	3.5	V

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 LED Specifications



5.3 Timing Specifications

At Ta = -20 °C To +70 °C, V_{DD} = 2.8±0.1V, V_{SS} = 0V.

Refer to Fig. 5 to Fig.7 the bus-timing diagram for Read/Write Characteristics

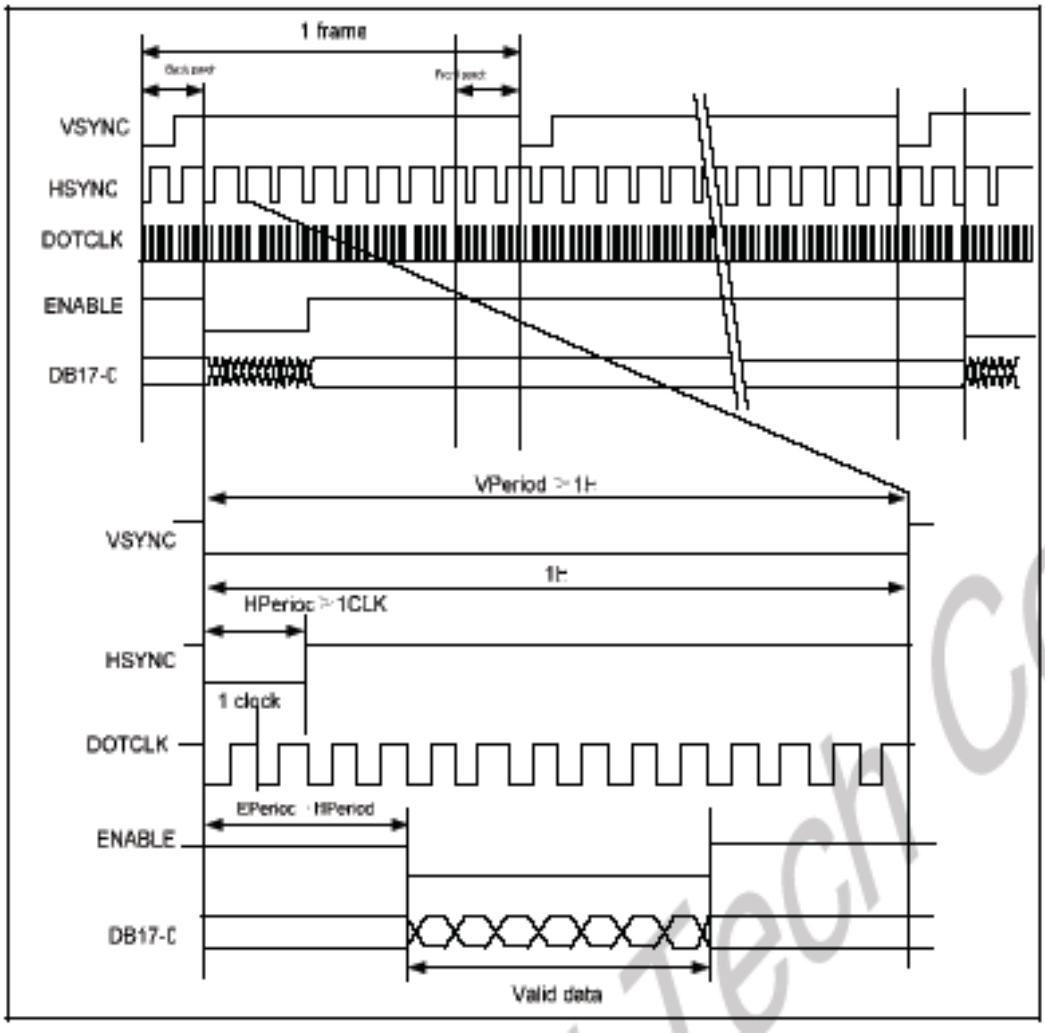


Figure 5: The detail-timing diagram for 18-bit and 16-bit

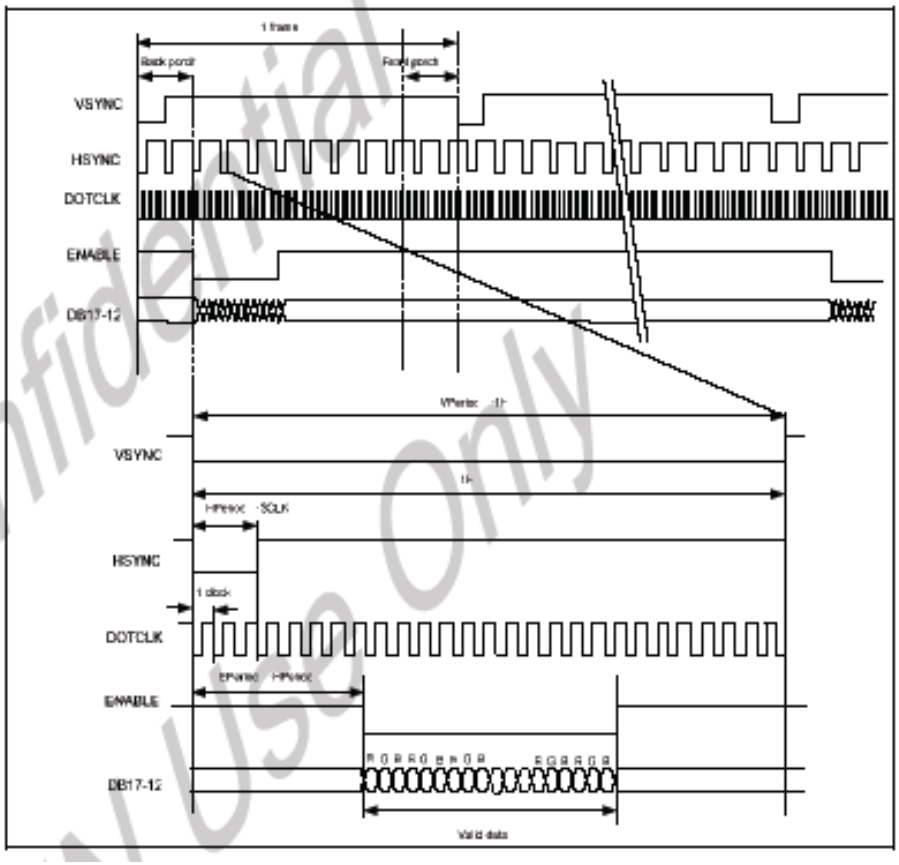


Figure 6: The detail timing diagram for 6-bit

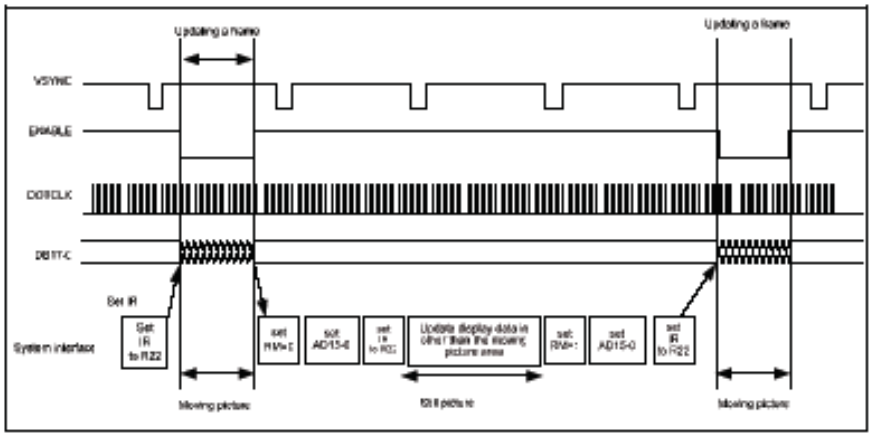


Figure 7: Illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

5.4 Instruction Table

Table 6

Category	Register No	Register	Upper 8-bit								Lower 8-bit							
			CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
	00h	ID Read	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1
	01h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
	02h	LCD AC Drive Control	0	0	0	0	0	1	B/C (0)	EOR (0)	0	0	0	0	0	0	0	NW0 (0)
	03h	Entry Mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	0	0
	04h	Resizing Control	0	0	0	0	0	0	RCV1 (0)	RCV0 (0)	0	0	RCH1 (0)	RCH0 (0)	0	0	RSZ1 (0)	RSZ0 (0)
	07h	Display control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	VON (0)	GON (0)	DTE (0)	COL (0)	0	D1 (0)	D0 (0)
	08h	Display control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
	09h	Display control (3)	0	0	0	0	0	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)
	0Ah	Display control (4)	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)
	0Ch	External interface control (1)	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
	0Dh	Frame Maker Position	0	0	0	0	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)
	0Fh	External interface control (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
	10h	Power Control (1)	0	0	0	SAP (0)	BT3 (0)	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	0	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0
	11h	Power Control (2)	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)
	12h	Power Control (3)	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
	13h	Power Control (4)	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0
	17h	Power Control (5)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE (0)
	20h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
	21h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
	22h	GRAM data																
	28h	NVM read data (1)	0	0	0	0	0	0	0	0	0	0	0	0	UID3 (0)	UID2 (0)	UID1 (0)	UID0 (0)
	29h	NVM read data (2)	0	0	0	0	0	0	0	0	0	0	0	VCM14 (0)	VCM13 (0)	VCM12 (0)	VCM11 (0)	VCM10 (0)
	2Ah	NVM read data (3)	0	0	0	0	0	0	0	0	VCMSEL(0)	0	0	VCM24 (0)	VCM23 (0)	VCM22 (0)	VCM21 (0)	VCM20 (0)
	30h	γ Control (1)	0	0	0	0	0	POKP12 (0)	POKP11 (0)	POKP10 (0)	0	0	0	0	0	POKP02 (0)	POKP01 (0)	POKP00 (0)
	31h	γ Control (2)	0	0	0	0	0	POKP32 (0)	POKP31 (0)	POKP30 (0)	0	0	0	0	0	POKP22 (0)	POKP21 (0)	POKP20 (0)
	32h	γ Control (3)	0	0	0	0	0	POKP52 (0)	POKP51 (0)	POKP50 (0)	0	0	0	0	0	POKP42 (0)	POKP41 (0)	POKP40 (0)
	33h	γ Control (4)	0	0	0	0	0	0	POFP11 (0)	POFP10 (0)	0	0	0	0	0	0	POFP01 (0)	POFP00 (0)
	34h	γ Control (5)	0	0	0	0	0	0	POFP31 (0)	POFP30 (0)	0	0	0	0	0	0	POFP21 (0)	POFP20 (0)
	35h	γ Control (6)	0	0	0	0	0	PORP12 (0)	PORP11 (0)	PORP10 (0)	0	0	0	0	0	PORP02 (0)	PORP01 (0)	PORP00 (0)
	36h	γ Control (7)	0	0	0	VORP14 (0)	VORP13 (0)	VORP12 (0)	VORP11 (0)	VORP10 (0)	0	0	0	VORP04 (0)	VORP03 (0)	VORP02 (0)	VORP01 (0)	VORP00 (0)
	37h	γ Control (8)	0	0	0	0	0	PONK12 (0)	PONK11 (0)	PONK10 (0)	0	0	0	0	0	PONK02 (0)	PONK01 (0)	PONK00 (0)
	38h	γ Control (9)	0	0	0	0	0	PONK32 (0)	PONK31 (0)	PONK30 (0)	0	0	0	0	0	PONK22 (0)	PONK21 (0)	PONK20 (0)
	39h	γ Control (10)	0	0	0	0	0	PONK52 (0)	PONK51 (0)	PONK50 (0)	0	0	0	0	0	PONK42 (0)	PONK41 (0)	PONK40 (0)
	3Ah	γ Control (11)	0	0	0	0	0	0	POFN11 (0)	POFN10 (0)	0	0	0	0	0	0	POFN01 (0)	POFN00 (0)
	3Bh	γ Control (12)	0	0	0	0	0	0	POFN31 (0)	POFN30 (0)	0	0	0	0	0	0	POFN21 (0)	POFN20 (0)
	3Ch	γ Control (13)	0	0	0	0	0	PORN12 (0)	PORN11 (0)	PORN10 (0)	0	0	0	0	0	PORN02 (0)	PORN01 (0)	PORN00 (0)
	3Dh	γ Control (14)	0	0	0	VORN14 (0)	VORN13 (0)	VORN12 (0)	VORN11 (0)	VORN10 (0)	0	0	0	VORN04 (0)	VORN03 (0)	VORN02 (0)	VORN01 (0)	VORN00 (0)
	50h	Window Horizontal RAM address start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
	51h	Window Horizontal RAM address start	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
	52h	Window Vertical RAM address start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
	53h	Window Vertical RAM address start	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
	60h	Driver Output Control	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
	61h	Image Display Control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)

	6Ah	Vertical Scoll ing Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
	80h	Display Position 1	0	0	0	0	0	0	0	PTDP 08 (0)	PTDP 07 (0)	PTDP 06 (0)	PTDP 05 (0)	PTDP 04 (0)	PTDP 03 (0)	PTDP 02 (0)	PTDP 01 (0)	PTDP 00 (0)
	81h	GRAM start line address 1	0	0	0	0	0	0	0	PTSA 08 (0)	PTSA 07 (0)	PTSA 06 (0)	PTSA 05 (0)	PTSA 04 (0)	PTSA 03 (0)	PTSA 02 (0)	PTSA 01 (0)	PTSA 00 (0)
	82h	GRAM end line address 1	0	0	0	0	0	0	0	PTEA 08 (0)	PTEA 07 (0)	PTEA 06 (0)	PTEA 05 (0)	PTEA 04 (0)	PTEA 03 (0)	PTEA 02 (0)	PTEA 01 (0)	PTEA 00 (0)
	83h	Display Position 2	0	0	0	0	0	0	0	PTDP 18 (0)	PTDP 17 (0)	PTDP 16 (0)	PTDP 15 (0)	PTDP 14 (0)	PTDP 13 (0)	PTDP 12 (0)	PTDP 11 (0)	PTDP 10 (0)
	84h	GRAM start line address 2	0	0	0	0	0	0	0	PTSA 18 (0)	PTSA 17 (0)	PTSA 16 (0)	PTSA 15 (0)	PTSA 14 (0)	PTSA 13 (0)	PTSA 12 (0)	PTSA 11 (0)	PTSA 10 (0)
	85h	GRAM end line address 2	0	0	0	0	0	0	0	PTEA 18 (0)	PTEA 17 (0)	PTEA 16 (0)	PTEA 15 (0)	PTEA 14 (0)	PTEA 13 (0)	PTEA 12 (0)	PTEA 11 (0)	PTEA 10 (0)
	90h	Panel Interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (0)	RTNI1 (0)	RTNI0 (0)
	92h	Panel Interface Control 2	0	0	0	0	0	NOWI 2(0)	NOWI 1(0)	NOWI 0(0)	0	0	0	0	0	0	0	0
	93h	Panel Interface Control 3	0	0	0	0	0	0	VEQW 11(0)	VEQW 10(0)	0	0	0	0	0	MCPI2 (0)	MCPI1 (0)	MCPI0 (0)
	95h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1 (0)	DIVE0 (0)	0	0	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)
	97h	Panel Interface Control 5	0	0	0	0	NOW E3(0)	NOW E2(0)	NOW E1(0)	NOW E0(0)	0	0	0	0	0	0	0	0
	98h	Panel Interface Control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2 (0)	MCPE1 (0)	MCPE0 (0)
	A0h	NVM Conmtrol1	0	0	0	0	0	0	0	0	TE (0)	0	EOP1 (0)	EOP0 (0)	0	0	EAD1 (0)	EAD0(0)
	A1h	NVM Control 2	0	0	0	0	0	0	0	0	ED7 (0)	0	0	ED4 (0)	ED3 (0)	ED2 (0)	ED1 (0)	ED0 (0)
	A4h	Calibration control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB (0)

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

6. Quality Units For N-Grade

6.1. Scope:

The incoming inspection standards shall be applied to TFT-LCD with cell-finished panel (hereinafter called "panel") that supplied by JINGHUA DISPLAYS LTD, except of those with special requirements from customer.

6.2. Incoming inspection:

The buyer (customer) shall inspect the panel within twenty calendar days of the delevery date (the "inspection period") at its own cost. The results of the inspection (acceptance or rejection) shall be recorded in writing, and a copy of this writing will be promptly sent to the seller. If the results of the inspection from buyer does not send to the seller within twenty calendar days of the delivery date. The shipment shall be regarded as accepted.

The buyer may, under commercially reasonable reject procedures, reject an entire lot in the delivery involved if, within the inspection period ,such samples of panel within such lot show an unacceptable number of defects in accordance with this incoming inspection standards provided, however the buyer shall notify the seller in writing of any such rejection promptly, and no later in three business days of the end of the inspection period.

Should the buyer fail to notify the seller within the inspection period, the buyer's right to reject the panel shall be lapsed and the panel shall be deemed “Accepted” by the buyer

6.3. Inspection sampling plan:

6.3.1.Lot size: Quantity per shipment lot per model.

6.3.2.Sampling type: Normal inspection, single sampling.

6.3.3.Sampling level: Level II.

6.3.4.Acceptable quality level (AQL):

6.3.4.1.Major defect: AQL=2.5%.

6.3.4.2.Minor defect: AQL=2.5%

6.4. Inspection instruments:

6.4.1.A single 20W fluorescent lamp.

6.4.2.Pattern generator: Philips PM5518 or equivalent model.

6.4.3.Video board:JINGHUA video board or equivalent. The output of the signal shall comply to the specifications provided by JINGHUA

6.4.4.Luminance colorimeter: Topcon BM-7 or equivalent model.

6.5. Inspection environment conditions:

6.5.1.Room temperature: 25 ± 5 ℃.

6.5.2.Inspection time: 10 ± 5 seconds for one modules.

6.5.3.Inspection distance: 30 ± 5 cm.

6.5.4.Viewing angle: The viewing line should be perpendicular to the surface of the module.

6.5.5. Lighting: Fluorescent light(Day-Light Type) display surface illumination to be 800~1200 Lux for cosmetic inspection. 100~400 Lux for function inspection.

6.6. Classification of defects:

Defects are classified as major defects and minor defects according to the degree of defectiveness defined herein.

6.6.1.Major defects:

A major defect is a defect that is likely to result in failure, or to reduce the usability of the product for its intended purpose.

6.6.1.1.Abnormal operation: panel cannot display normally.

6.6.1.2.Line defect.

6.6.1.3.Extensive Glass Crack (Refer to 6-2-2).

6.6.2.Minor defects:

A minor defect is a defect that is not likely to reduce the usability of the product for its intended purpose.

6.6.2.1.Dot defect:

A. Inspection pattern : Full white,full black, full red, full green, full blue and grey screens.

B. Criteria :(acceptable)

Item	**Total**
Black dot defect	≦ 2
Bright dot defect (Red, Green, Blue, White)	≦ 2
Total	≦ 4

Note: 1. Dot defect is defined as the defective area of the dot area is larger than 50 % of the dot area and it is invisible through 5% ND filter.

2. Tiny bright dot: Meaning the bright dot is small than 50% of the dot area and it also should be invisible under 5% ND filter.
(Don’t defin the amount)

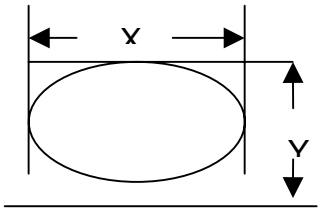
6.6.2.2.Scratches, dent, and extraneous substances:

Dimensional unit: mm

Item		**Dimension (unit: mm)**		**Criteria/ Judgment**
Polarizer Scratch/ particle	Dot shape	d≦0.15		Ignore
		0.15＜d≦0.3		N≦4
		d＞0.3		None
	Line shape	W≦0.05		Ignore
		0.05＜W≦0.1	L≦0.5	Ignore
			0.5＜L≦2.5	N≦4
			L＞2.5	None
		W＞0.1		None
Polarizer bubble/ dent (active area)	Dot shape	d≦0.4		Ignore
		0.4<d≦0.7		N≦4
		d ＞0.7		None
	Line shape	W≦0.05		Ignore
		0.05＜W≦0.1	L≦0.5	Ignore
			0.5＜L≦2.5	N≦4
			L＞2.5	None
		W＞0.1		None
Dirty / surface stain	display area/ bonding area	No-define		If the defect could be wiped by alcohol is acceptable.

Note 1. The definition of d is defined as follows:

Average diameter (d)=(X+Y)/2, where



2. Polarizer bubble/bubble line is defined as the bubble/bubble line appears on active display area. The defect of polarizer bubble/ bubble line shall be ignored if the polarizer bubble/bubble line appears on the outside of the active display area.

6.6.3.Glass crack

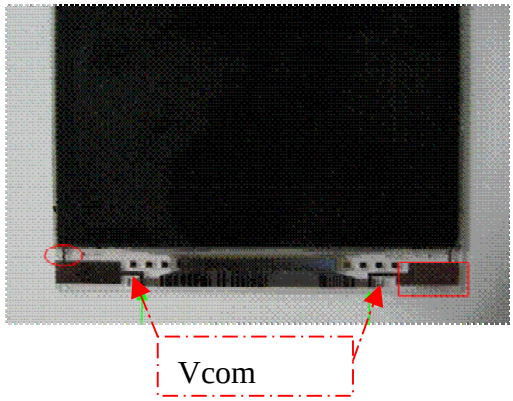
The criterion for glass crack is established as it doesn't cause any functional and relibility failure and other galss crack without this concern shall be accepted. (refer to picture)

6.6.3.1 Can't damage alignment mark of IC and FPC

6.6.3.2. Function test can be work as normally.

6.6.3.3. Both the citcuit of Vcom can't open, (Both the route shall be ok from FPC pad to display area)

6.6.3.4.The outline of Vcom signal might be different with our other modules.



6.6.4. All the defects shall be determined only after polarizer attached and COG process.

6.7. Inspection judgement:

6.7.1.The judgement of the shipped lot(acceptance or rejection) should follow the sampling plan of MIL-STD-105E,single sampling,normal inspection,level II.

6.7.2.If the number of defects is equal to or less than the applicable acceptance level, the lot shall be accepted.

6.7.3.If the number of defects is more than the applicable acceptance level, the lot shall be rejected and the buyer should inform the seller of the result of incoming inspection in writing.

6.8 Precaution:

Please pay attention to the following items when you use the LCD panel.

6.8.1 Do not twist or bend the panel and prevent the unsuitable external force for panel during assembly.
6.8.2 Adopt measures for good heat radiation. Be sure to use the panel with in the specified temperature.
6.8.3 Avoid dust or oil mist during assembly.
6.8.4 Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the panel.
6.8.5 Less EMI: it will be more safety and less noise.
6.8.6 Please operate panel in suitable temperature. The response time & brightness will drift by different temperature.
6.8.7 Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
6.8.8 Be sure to turn off the power when connecting or disconnecting the circuit.
6.8.9 Display surface never likes dirt or stains.
6.8.10 A dewdrop may lead to destruction. Please wipe off any moisture before using panel.
6.8.11 Sudden temperature changes cause condensation.
6.8.12 High temperature and humidity may degrade performance. Please do not expose the panel to the direct sunlight and so on.
6.8.13 Acetic acid or chlorine compounds are not friends with TFT display panel.
6.8.14 Static electricity will damage the panel; please do not touch the panel without any grounded device.
6.8.15 No strong vibration or shock. It would lead glass broken.
6.8.16 Storage the panel in suitable environment with regular packing.
6.8.17 Be careful of injury from a broken display panel.
6.8.18 Please avoid the pressure adding to the surface (front or rear side) of panel, because it will cause the display non-uniformity or other function issue.

7. Quality Units For P-Grade

7.1. Scope:

The incoming inspection standards shall be applied to TFT-LCD CELL (hereinafter called "CELL") that supplied by JINGHUA DISPLAYS LTD, except of those with special requirements from customer.

7.2. Incoming inspection:

The buyer (customer) shall inspect the modules within twenty calendar days of the delivery date (the "inspection period") at its own cost. The results of the inspection (acceptance or rejection) shall be recorded in writing, and a copy of this writing will be promptly sent to the seller. If the results of the inspection from buyer does not send to the seller within twenty calendar days of the delivery date. The modules shall be regards as acceptance.

The buyer may, under commercially reasonable reject procedures, reject an entire lot in the delivery involved if, within the inspection period, such samples of modules within such lot show an unacceptable number of defects in accordance with this incoming inspection standards, provided however that the buyer must notify the seller in writing of any such rejection promptly, and not later than within three business days of the end of the inspection period. Should the buyer fail to notify the seller within the inspection period, the buyer's right to reject the modules shall be lapsed and the modules shall be deemed to have been accepted by the buyer.

7.3. Inspection sampling plan:

Unless otherwise agreed in writing, the sampling plan of incoming inspection shall be based on MIL-STD-105E.

7.3.1.Lot size: Quantity per shipment lot per model.

7.3.2.Sampling type: Normal inspection, single sampling.

7.3.3.Sampling level: Level II.

7.3.4.Acceptable quality level (AQL):

7.3.4.1.Major defect: AQL=0.65%.

7.3.4.2.Minor defect: AQL=1.0%

7.4. Inspection instruments:

7.4.1.A single 20W fluorescent lamp.

7.4.2.Luminance colorimeter: Topcon BM-7 or equivalent model.

7.5. Inspection environment conditions:

7.5.1.Room temperature: 25±5 ℃.

7.5.2. Humidity: 55 ± 10 % RH.

7.5.3.Lighting: Fluorescent light(Day-Light Type) display surface illumination to be 800~1200 Lux for cosmetic inspection. 100~400 Lux for function inspection.

7.5.4.The-viewing line should be perpendicular to the surface of the module.

7.5.5.Inspection distance:30±5 cm.

7.6. Classification of defects:

Defects are classified as major defects and minor defects according to the degree of defectiveness defined herein.

7.6.1.Major defects:

A major defect is a defect that is likely to result in failure, or to reduce the usability of the product for its intended purpose.

7.6.1.1.Abnormal operation: panel cannot display normally.

7.6.1.2.Line defect.

7.6.1.3.Extensive Glass Crack (Refer to 6-4).

7.6.1.4.LC bubble & LC leakage.

7.6.2.Minor defects:

A minor defect is a defect that is not likely to reduce the usability of the product for its intended purpose.

7.6.2.1.Dot defect:

A. Inspection pattern: Full white, full black, full gray, horizontal white-black flicker, vertical white-black flicker

B. Criteria :(acceptable)

Item	**Total**
Black dot defect	N≦ 2
Bright dot defect	N≦ 1
Total	N≦ 2

Item	**Criteria/judgnment**	
Tiny bright dot	Invisible under ND 0.4	Ingore
	Invisible under ND 0.4	Not allowed

Note 1. This inspection cannot be evaluated before module assembly.

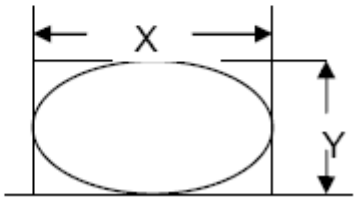
2. Dot defect is defined as the defective area of the dot area, which is larger than 50% of the dot area. The distance between dot defects should be more than 5mm apart. (Tiny bright dot can’t adapt to this rule.)
3. Tiny bright dot: Meaning the bright dot is small than 50% of the dot area and it should be invisible under ND filter 39.85%. (ND-0.4).

7.6.3.Scratches and extraneous substances:

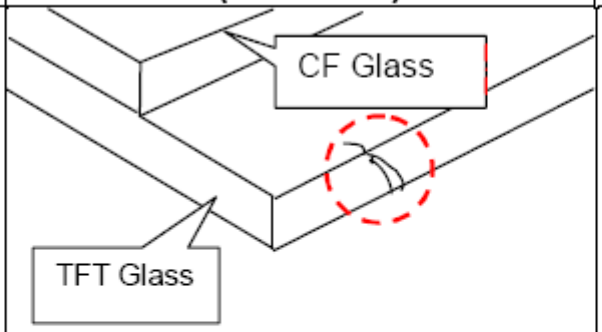
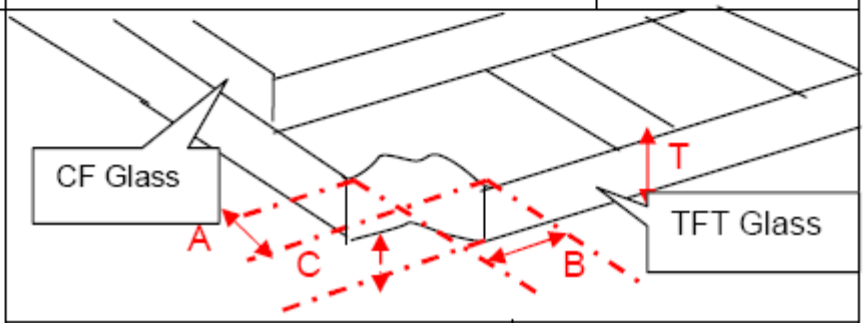
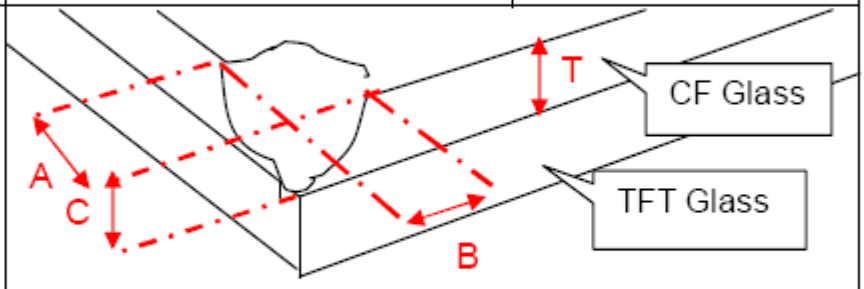
Dimensional unit: mm

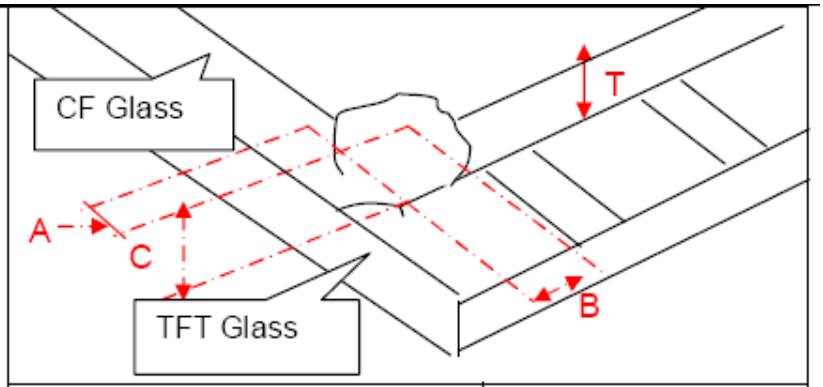
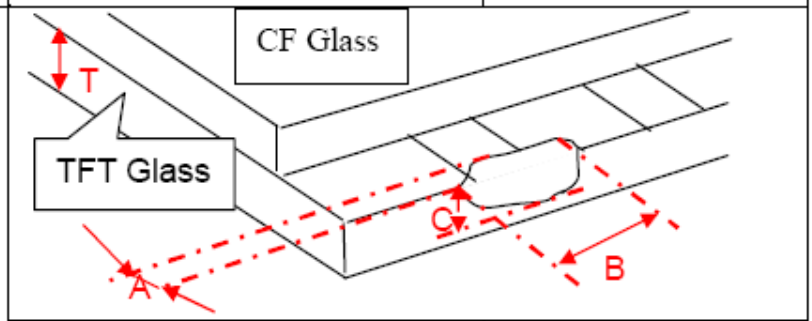
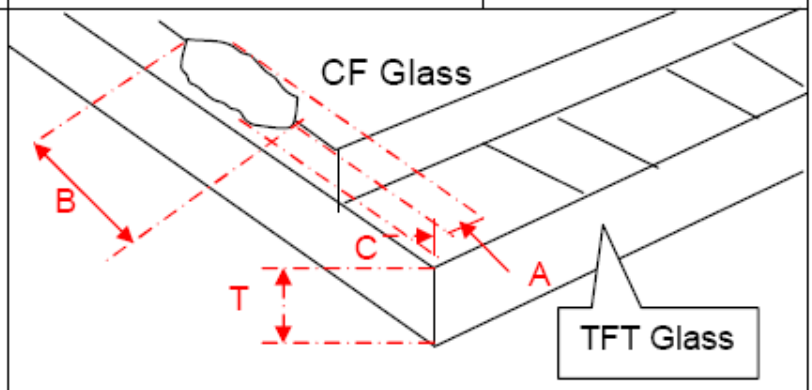
Item		Dimension (unit: mm)	Criteria/Judgment
Scratch	Display area	W≤0.03	Ignore
		L≤2.5 , 0.03<W≤0.05	N≤2
		L>2.5 or W>0.05	None
Extraneous Substances/ Foreign material (Inside the Cell)	Black/ White spots(The distance between dot defects shuould be more 5mm apart)	D ≦0.15	Ignore
		0.15<D≦0.2	N≦2
		D＞0.2	Not allowed
	Black/ White lines L: Length W: Width	W≦0.03	Ignore
		L≦2.5 0.03＜W≦0.05	N≦2
		L>2.5 orW＞0.05	None
Dirty / surface stain	display area/ bonding area	No-define	If the defect could be wiped by alcohol is acceptable.

Note 1. The definition of D is defined as follows:
Average diameter D=(X+Y)/2, where



7.6.4 Glass Broken and Chipping

Item		Dimension (unit: mm)	Criteria/ Judgment
Glass Crack	Extensive Crack		Not allowed
Glass Broken	Cornor Broken (I)		
		A≦2.0, B≦2.0, C≦T	Ignore
		A>2.0 or B>2.0	Not allowed
	Cornor Broken (II)	 Note: To be applied to both CF and TFT Glass	
		A≦1.5, B≦1.5, C≦T	Ignore
		A>1.5 or B>1.5	Not allowed

(Continued)	Cornor Broken (III)		
		A≦1.5, B≦1.5, C≦T	Ignore
		A>1.5 or B>1.5	Not allowed
	Pad Broken		
		A≦0.8, B≦5, C≦T	Ignore
		A>0.8 or B>5	Not allowed
	Side Broken	 Note: To be applied to both CF and TFT glass.	
		A≦0.5, B≦5, C≦T	Ignore
		A>0.5 or B>5	Not allowed

Note: 1. Extensive crack is not allowed.
2. "T" stands for "Thickness" of the TFT, CF glass.

7.7 Precaution:

Please pay attention to the following items when you use the LCD panel.

7.7.1 Do not twist or bend the panel and prevent the unsuitable external force for panel during assembly.

7.7.2 Adopt measures for good heat radiation. Be sure to use the panel with in the specified temperature.

7.7.3 Avoid dust or oil mist during assembly.

7.7.4 Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the panel.

7.7.5 Less EMI: it will be more safety and less noise.

7.7.6 Please operate panel in suitable temperature. The response time & brightness will drift by different temperature.

7.7.7 Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.

7.7.8 Be sure to turn off the power when connecting or disconnecting the circuit.

7.7.9 Display surface never likes dirt or stains.

7.7.10 A dew drop may lead to destruction. Please wipe off any moisture before using panel.

7.7.11 Sudden temperature changes cause condensation.

7.7.12 High temperature and humidity may degrade performance. Please do not expose the panel to the direct sunlight and so on.

7.7.13 Acetic acid or chlorine compounds are not friends with TFT display panel.

7.7.14 Static electricity will damage the panel, please do not touch the panel without any grounded device.

7.7.15 No strong vibration or shock. It would lead glass broken.

7.7.16 Storage the panel in suitable environment with regular packing.

7.7.17 be careful of injury from a broken display panel.

7.7.18 Please avoid the pressure adding to the surface (front or rear side) of panel, because it will cause the display non-uniformity or other function issue.

- END -