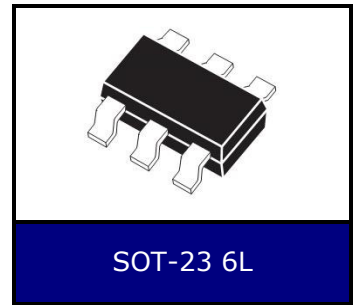




LOW CAPACITANCE TVS DIODE ARRAY

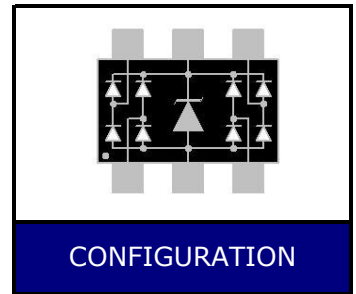
The PJSRV05-4 has a low capacitance of 2.1pF and operates with virtually no insertion loss to 1GHz. This makes the device ideal for protection of high-speed data lines such as USB2.0, firewire, DVI, and gigabit Ethernet interfaces.

The low capacitance array configuration allows the user to protect Four high-speed data or transmission lines. The low inductance construction minimizes voltageovershoot during high current surges. They may be used to meet the ESD immunity requirements of IEC61000-4-2, Level 4 (15kV air, 8kVcontact discharge).



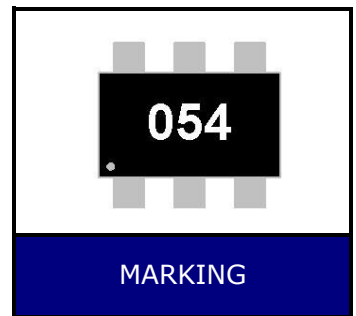
SPECIFICATION FEATURES

- IEC61000-4-2 ESD 15kV Air, 8kV Contact compliance
- Low leakage current,maxiimum of 1uA at rated voltage
- Low clamping voltage
- Peak power dissipation of 350W under 8/20us waveform
- Protect four I/O lines.
- Molded JEDEC SOT-23 6L package
- Flammability rating UL94V-0
- Lead Free package 100% tin plating matt finish



APPLICATIONS

- USB 2.0 Power and Data Line Protection
- Video Graphics Cards
- Monitors and Flat Panel Displays
- Digital Vedio Interface (DVI)
- 10/100/1000 Ethernet
- ATM Interfaces



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Pulse Power (8/20us waveform)	P _{PP}	350	W
Peak Pulse Current (8/20us waveform)	I _{PPM}	12	A
ESD Voltage (HBM Contact)	V _{ESD}	>8	kV
Operating Temperature Range	T _J	-55~+150	°C
Storage Temperature Range	T _{STG}	-55~+150	°C



ELECTRICAL CHARACTERISTICS (T_J=25°C)

PJSRV05-4

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse Stand-Off Voltage	V _{WRM}				5	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} =1mA, PIN 5 to 2	6			V
Reverse Leakage Current	I _R	V _R =5V, PIN 5 to 2		1.2	3	uA
Clamping Voltage (8/20us)	V _C	I _{pp} =1A, Any I/O pin to Pin 2			12	V
Clamping Voltage (8/20us)	V _C	I _{pp} =5A, Any I/O pin to Pin 2			17	V
Off State Junction Capacitance	C _J	0Vdc, f=1MHZ between I/O lines and GND		2.1	3	pF
Off State Junction Capacitance	C _J	0Vdc, f=1MHZ between I/O lines		1	1.5	pF



TYPICAL CHARACTERISTICS CURVES

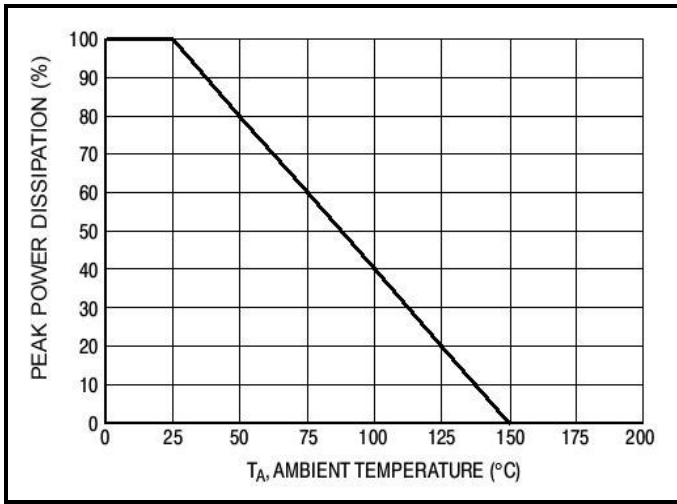


Figure 1. Power Derating Curve

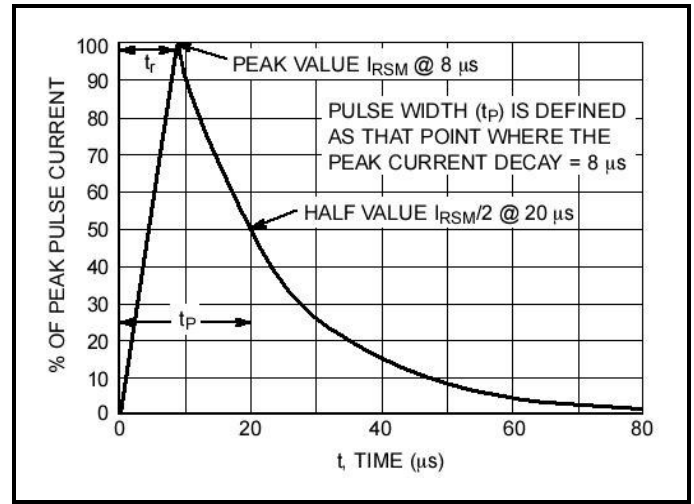


Figure 2. 8x20us Pulse Waveform

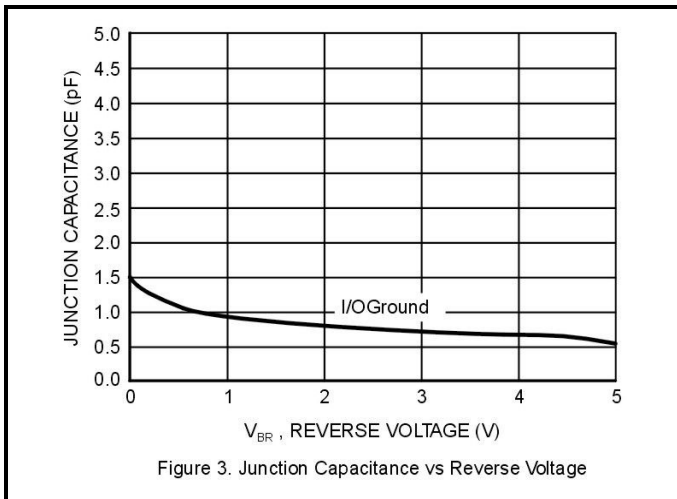


Figure 3. Junction Capacitance vs Reverse Voltage

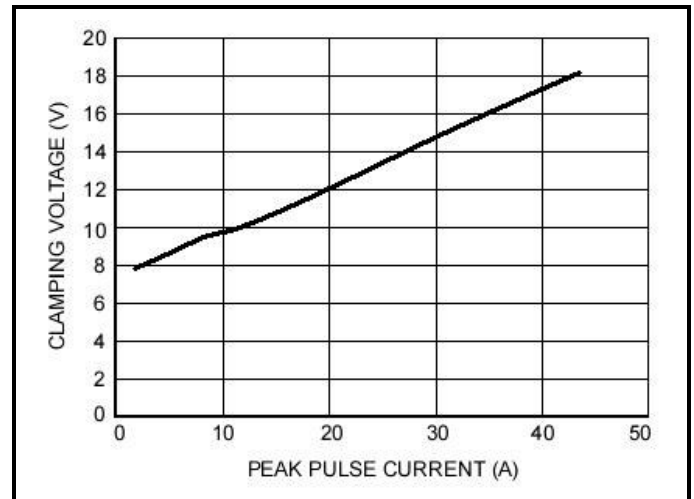


Figure 4. Clamping Voltage vs Peak Pulse Current (8x20 Waveform)

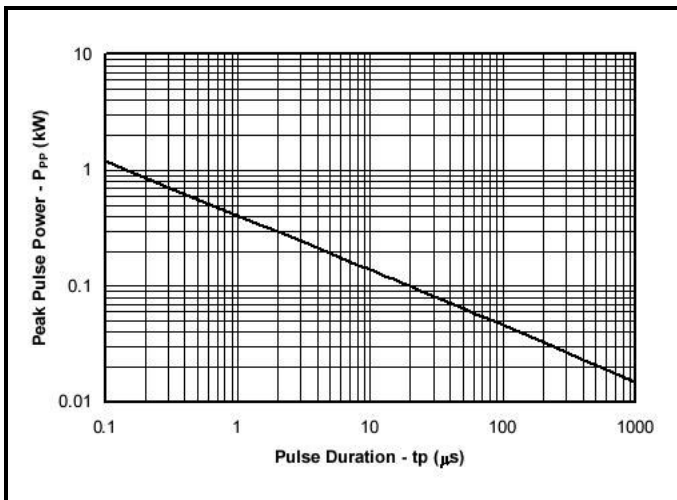


Figure 5. Non-Repetitive Peak Pulse vs. Pulse Time

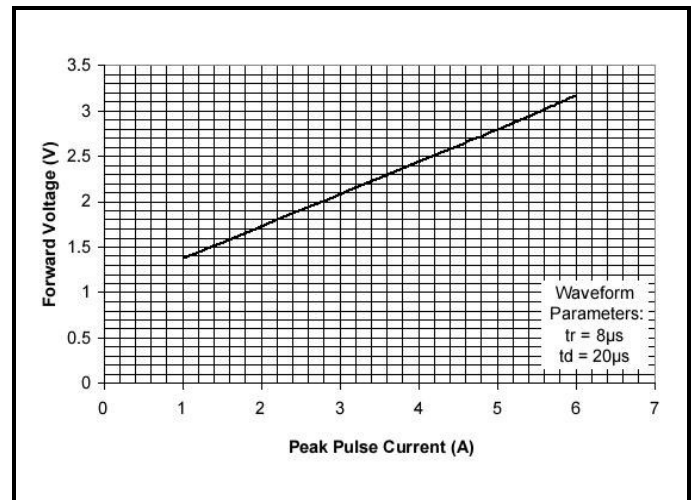
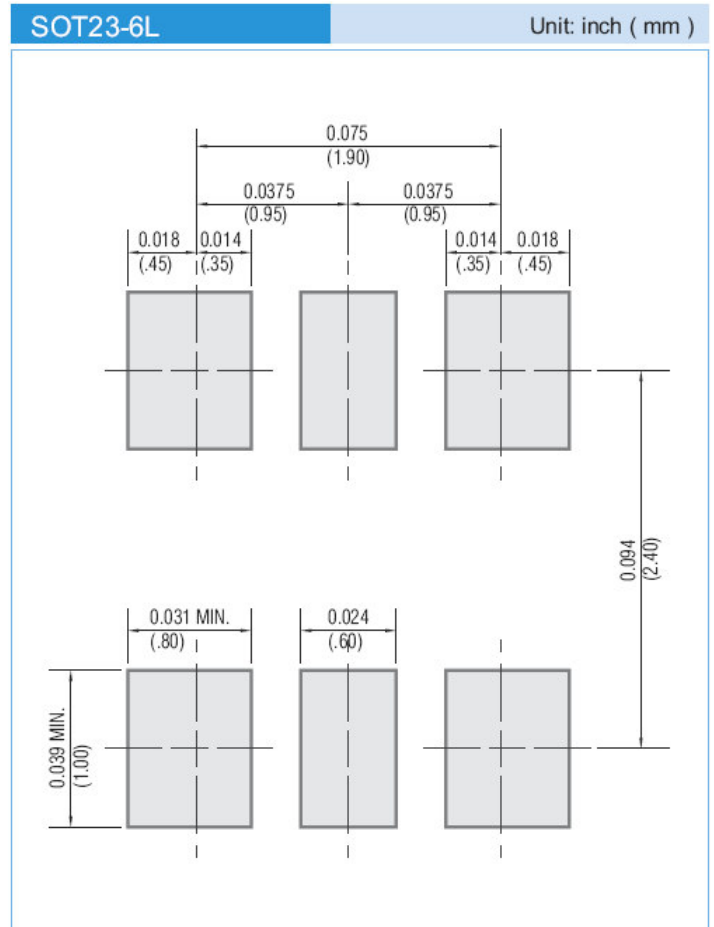
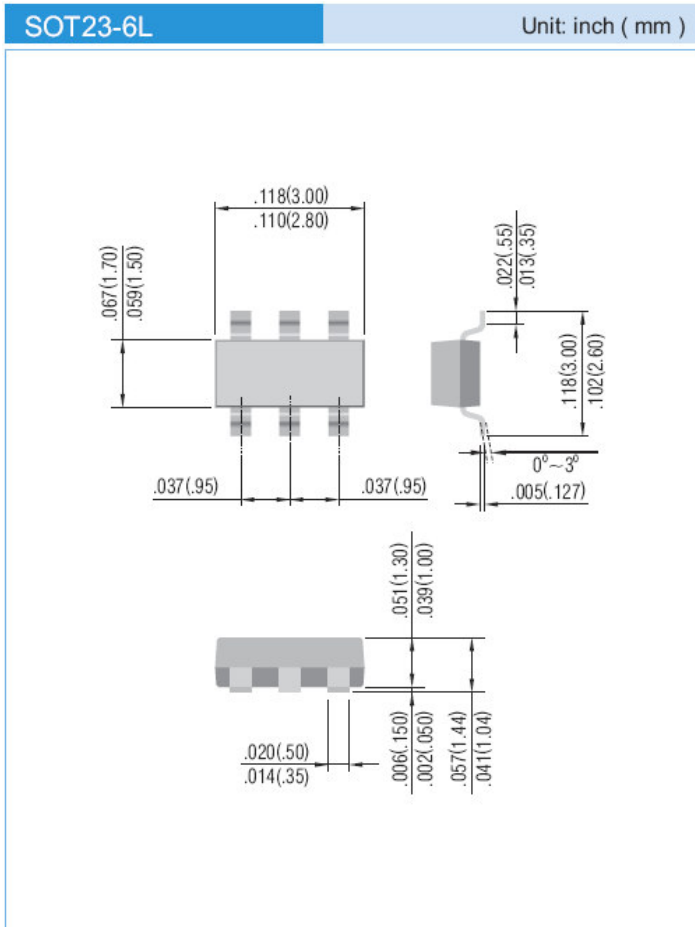


Figure 6. Forward Voltage vs. Forward Current



PACKAGE AND SUGGESTED PAD LAYOUT DIMENSION



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