LINEAR TECHNOLOGY

INITIAL RELEASE
Final Electrical Specifications

LTC1665

Micropower Octal 8-Bit DAC

February 1999

FEATURES

- **Tiny: 8 DACs in the Board Space of an SO-8**
- **Ultralow Power: 56μA per DAC Plus 1μA Sleep Mode for Extended Battery Life**
- Wide 2.7V to 5.5V Supply Range
- Restores Last DAC Setting After Sleep
- Asynchronous $\overline{CLR}$ Function
- **Rail-to-Rail Voltage Outputs Drive 1000pF**
- Reference Range Includes Supply for Ratiometric 0V-to-V_{CC} Output
- 3-Wire Serial Interface with Schmitt Trigger Inputs and Daisy-Chain Capability
- Differential Nonlinearity: ≤±0.5LSB Max
- Pin Compatible with the 10-Bit LTC1660

APPLICATIONS

- Mobile Communications
- Digitally Controlled Amplifiers and Attenuators
- Portable Battery-Powered Instruments
- Automatic Calibration for Manufacturing
- Remote Industrial Devices

DESCRIPTION

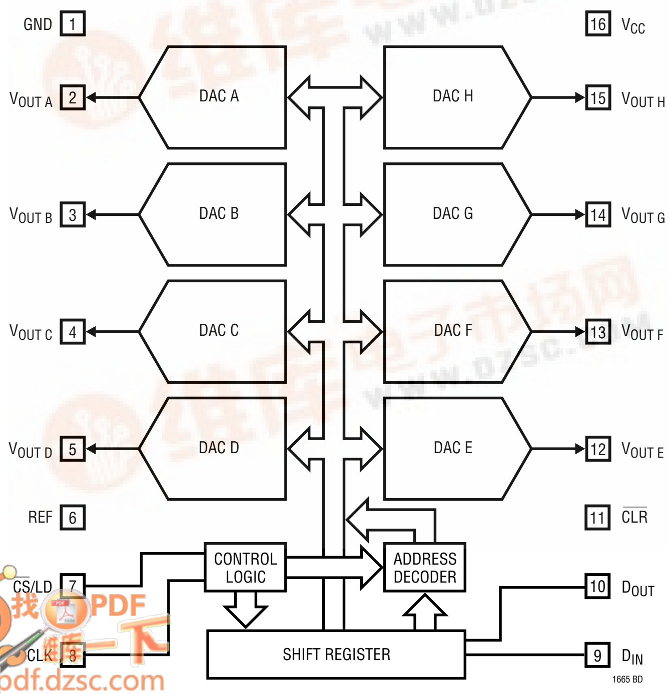
The LTC®1665 integrates eight accurate, addressable, 8-bit digital-to-analog converters (DACs) in a single tiny 16-pin narrow SSOP package. Each buffered DAC consumes just 56μA total supply current, yet is capable of supplying DC output currents in excess of 5mA and reliably driving capacitive loads up to 1000pF. Sleep mode further reduces total supply current to a negligible 1μA.

Linear Technology's proprietary, inherently monotonic architecture provides excellent linearity while allowing for an exceptionally small external form factor.

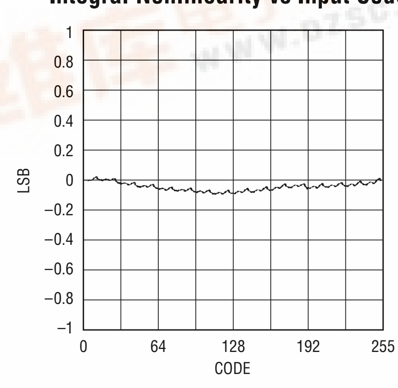
Ultralow supply current, power-saving Sleep mode and extremely compact size make the LTC1665 ideal for battery-powered applications, while its straightforward usability, high performance and wide supply range make it an excellent choice as a general purpose converter.

For higher resolution, please refer to the pin compatible LTC1660 micropower octal 10-bit DAC.

BLOCK DIAGRAM



Integral Nonlinearity vs Input Code



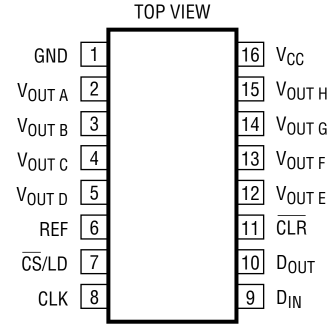
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND .... −0.5V to 7.5V
Logic Inputs to GND .... −0.5V to 7.5V
$V_{OUT\ A}$, $V_{OUT\ B}$…$V_{OUT\ H}$,
REF to GND .... −0.2V to (V_{CC} + 0.2V)
Maximum Junction Temperature .... 125°C
Operating Temperature Range
  LTC1665C.. 0°C to 70°C
  LTC1665I.. −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)................ 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



GN PACKAGE 16-LEAD PLASTIC SSOP
N PACKAGE 16-LEAD PDIP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W (GN)
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N)

ORDER PART NUMBER
LTC1665CGN LTC1665CN LTC1665IGN LTC1665IN
GN PART MARKING
1665 1665I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V to 5.5V, $V_{REF} \le V_{CC}$, V_{OUT} Unloaded, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Accuracy							
	Resolution		●	8			Bits
	Monotonicity	$V_{REF} \le V_{CC}$ – 0.1V (Note 2)	●	8			Bits
DNL	Differential Nonlinearity	$V_{REF} \le V_{CC}$ – 0.1V (Note 2)	●		±0.1	±0.5	LSB
INL	Integral Nonlinearity	$V_{REF} \le V_{CC}$ – 0.1V (Note 2)	●		±0.2	±1.0	LSB
V_{OS}	Offset Error	Measured at Code 4	●		±4	±30	mV
	V_{OS} Temperature Coefficient				±15		µV/°C
FSE	Full-Scale Error	V_{CC} = 5V, V_{REF} = 4.096V	●		±1	±4	LSB
	Full-Scale Error Temperature Coefficient				±30		µV/°C
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Not in Sleep Mode	●	35	65		kΩ
	Capacitance	(Note 6)			15		pF
I_{REF}	Reference Current	Sleep Mode	●		0.001	1	µA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3) V_{CC} = 3V (Note 3) Sleep Mode (Note 3)	● ● ●		450 340 1	730 550 3	µA µA µA
DC Performance							
	Short-Circuit Current Low	V_{OUT} = 0V, V_{CC} = V_{REF} = 5V, Code = 255	●	10	30	100	mA
	Short-Circuit Current High	V_{OUT} = V_{CC} = V_{REF} = 5V, Code = 0	●	10	27	120	mA
AC Performance							
	Voltage Output Slew Rate	Rising (Notes 4, 5) Falling (Notes 4, 5)			0.60 0.25		V/µs V/µs
	Voltage Output Settling Time	To ±0.5LSB (Notes 4, 5)			30		µs

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V to 5.5V, $V_{REF} \le V_{CC}$, V_{OUT} Unloaded, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 2.7V to 5.5V V_{CC} = 2.7V to 3.6V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V V_{CC} = 2.7V to 5.5V	● ●			0.8 0.6	V V
V_{OH}	Digital Output High Voltage	I_{OUT} = –1mA, D_{OUT} Only	●	V_{CC} – 1			V
V_{OL}	Digital Output Low Voltage	I_{OUT} = 1mA, D_{OUT} Only	●			0.4	V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 6)	●			10	pF

TIMING CHARACTERISTICS (See Figure 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} = 4.5V to 5.5V							
t_1	D_{IN} Valid to CLK Setup		●	40	15		ns
t_2	D_{IN} Valid to CLK Hold		●	0	–11		ns
t_3	CLK High Time	(Note 6)	●	30	5		ns
t_4	CLK Low Time	(Note 6)	●	30	7		ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	80	30		ns
t_6	LSB CLK High to $\overline{CS}$/LD High	(Note 6)	●	30	4		ns
t_7	$\overline{CS}$/LD Low to CLK High	(Note 6)	●	80	26		ns
t_8	D_{OUT} Propagation Delay	C_{LOAD} = 15pF (Note 6)	●	5	26	80	ns
t_9	CLK Low to $\overline{CS}$/LD Low	(Note 6)	●	20	0		ns
t_{10}	$\overline{CLR}$ Pulse Width	(Note 6)	●	100	37		ns
t_{11}	$\overline{CS}$/LD High to CLK Positive Edge	(Note 6)	●	30	0		ns
V_{CC} = 2.7V to 5.5V							
t_1	D_{IN} Valid to CLK Setup	(Note 6)	●	60	20		ns
t_2	D_{IN} Valid to CLK Hold	(Note 6)	●	0	–14		ns
t_3	CLK High Time	(Note 6)	●	50	8		ns
t_4	CLK Low Time	(Note 6)	●	50	12		ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	100	30		ns
t_6	LSB CLK High to $\overline{CS}$/LD High	(Note 6)	●	50	5		ns
t_7	$\overline{CS}$/LD Low to CLK High	(Note 6)	●	100	27		ns
t_8	D_{OUT} Propagation Delay	C_{LOAD} = 15pF (Note 6)	●	5	47	150	ns
t_9	CLK Low to $\overline{CS}$/LD Low	(Note 6)	●	30	0		ns
t_{10}	$\overline{CLR}$ Pulse Width	(Note 6)	●	120	41		ns
t_{11}	$\overline{CS}$/LD High to CLK Positive Edge	(Note 6)	●	30	0		ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Nonlinearity and monotonicity are defined from code 4 to code 255 (full scale). See Applications Information.

Note 3: Digital inputs at 0V or V_{CC}.

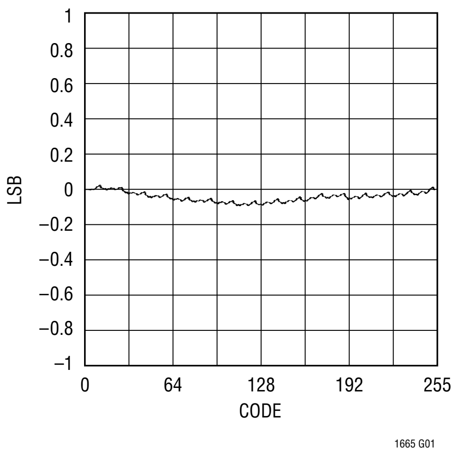
Note 4: Load is 10kΩ in parallel with 100pF.

Note 5: $V_{CC} = V_{REF}$ = 5V. DAC switched between $0.1V_{FS}$ and $0.9V_{FS}$, i.e., codes k = 26 and k = 230.

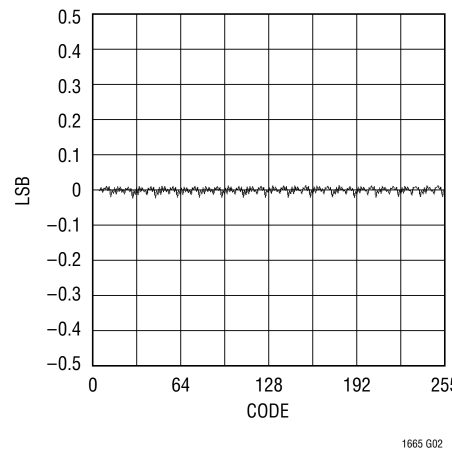
Note 6: Guaranteed by design and not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

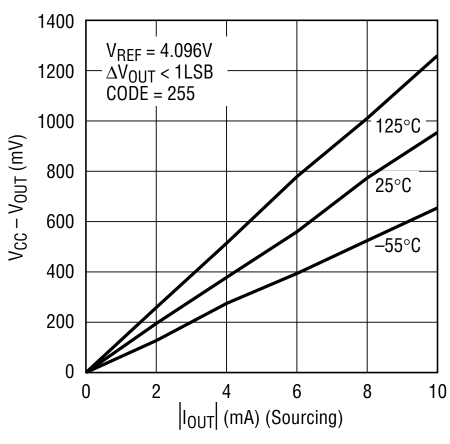
Integral Nonlinearity (INL)



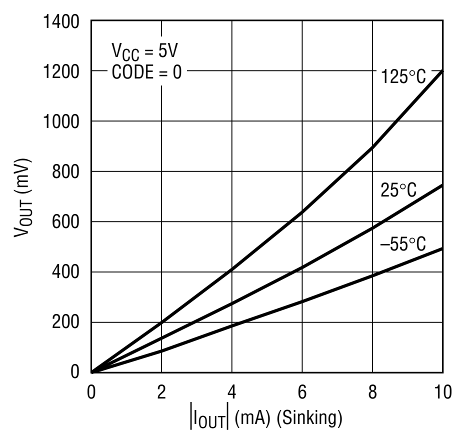
Differential Nonlinearity (DNL)



Minimum Supply Headroom vs Load Current (Output Sourcing)

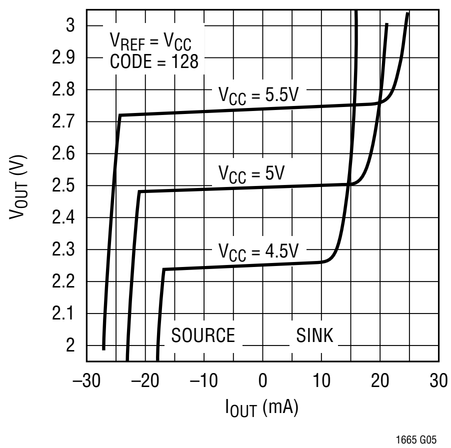


Minimum V_{OUT} vs Load Current (Output Sinking)

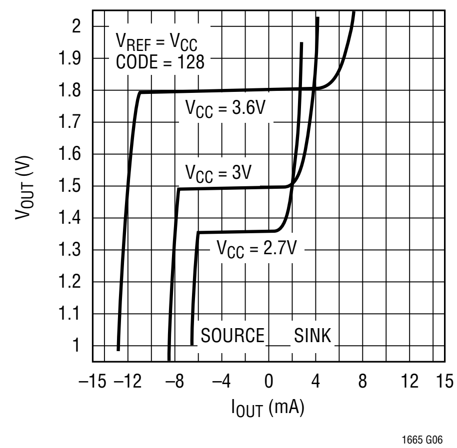


TYPICAL PERFORMANCE CHARACTERISTICS

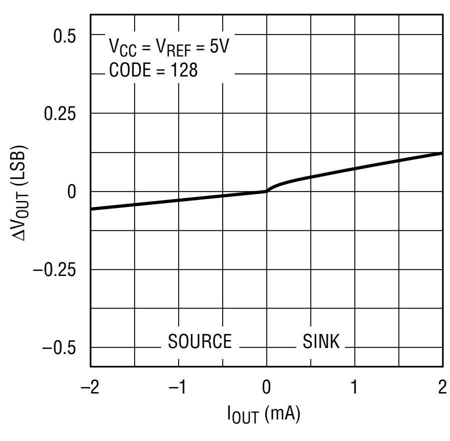
Midscale Output Voltage vs Load Current



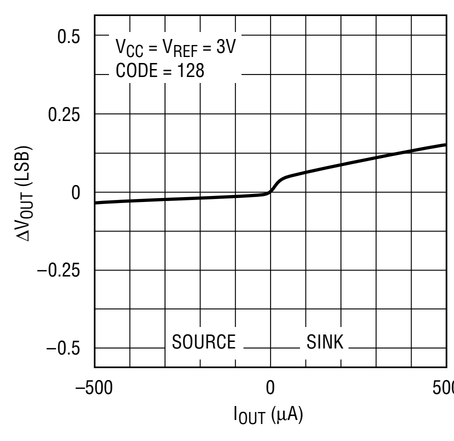
Midscale Output Voltage vs Load Current



Load Regulation vs Output Current

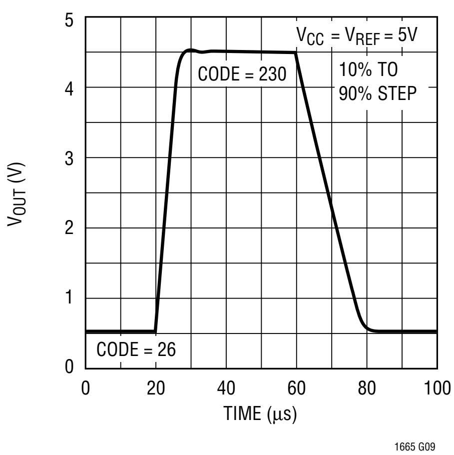


Load Regulation vs Output Current

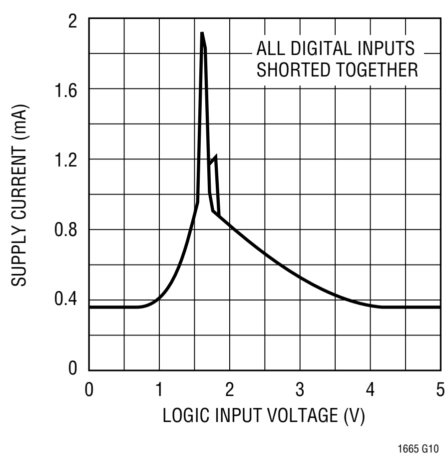


TYPICAL PERFORMANCE CHARACTERISTICS

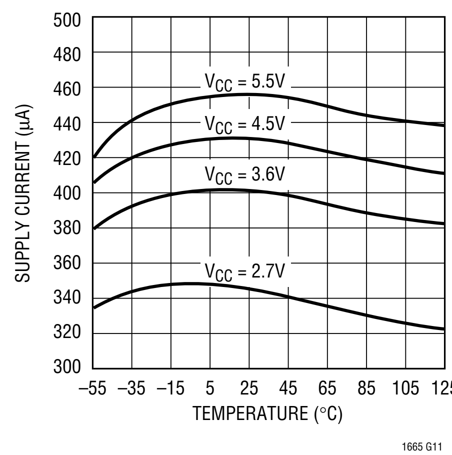
Large-Signal Step Response



Supply Current vs Logic Input Voltage



Supply Current vs Temperature



PIN FUNCTIONS

GND (Pin 1): System Ground.

$V_{OUT\ A}$ to $V_{OUT\ H}$ (Pins 2-5 and 12-15): DAC Analog Voltage Outputs. The output range is

$$0 \text{ to } \left(\frac{255}{256}\right)V_{REF}$$

REF (Pin 6): Reference Voltage Input. $0V \le V_{REF} \le V_{CC}$.

$\overline{CS}$/LD (Pin 7): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, CLK is enabled for shifting data on D_{IN} into the register. When $\overline{CS}$/LD is pulled high, CLK is disabled and data is loaded from the shift register into the specified DAC register(s), updating the analog output(s). CMOS and TTL compatible.

CLK (Pin 8): Serial Interface Clock Input. CMOS and TTL compatible.

D_{IN} (Pin 9): Serial Interface Data Input. Data on the D_{IN} pin is shifted into the 16-bit register on the rising edge of CLK. CMOS and TTL compatible.

D_{OUT} (Pin 10): Serial Interface Data Output. Data appears on D_{OUT} 16 positive CLK edges after being applied to D_{IN}. May be tied to D_{IN} of another LTC1665 for daisy-chain operaton. CMOS and TTL compatible.

$\overline{CLR}$ (Pin 11): Asynchronous Clear Input. All internal shift and DAC registers are cleared to zero at the falling edge of the $\overline{CLR}$ signal, forcing the analog outputs to zero scale. CMOS and TTL compatible.

V_{CC} (Pin 16): Supply Voltage Input. $2.7V \le V_{CC} \le 5.5V$.

DEFINITIONS

Differential Nonlinearity (DNL): The difference between the measured change and the ideal 1LSB change for any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} – LSB)/LSB$$

Where ΔV_{OUT} is the measured voltage difference between two adjacent codes.

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

Full-Scale Error (FSE): The deviation of the actual full-scale voltage from ideal. FSE includes the effects of offset and gain errors (see Applications Information).

Integral Nonlinearity (INL): The deviation from a straight line passing through the endpoints of the DAC transfer curve (Endpoint INL). Because the output cannot go below zero, the linearity is measured between full scale and the lowest code which guarantees the output will be greater than zero. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} – V_{OS} – (V_{FS} – V_{OS})(code/255)]/LSB$$

Where V_{OUT} is the output voltage of the DAC measured at the given input code.

Least Significant Bit (LSB): The ideal voltage difference between two successive codes.

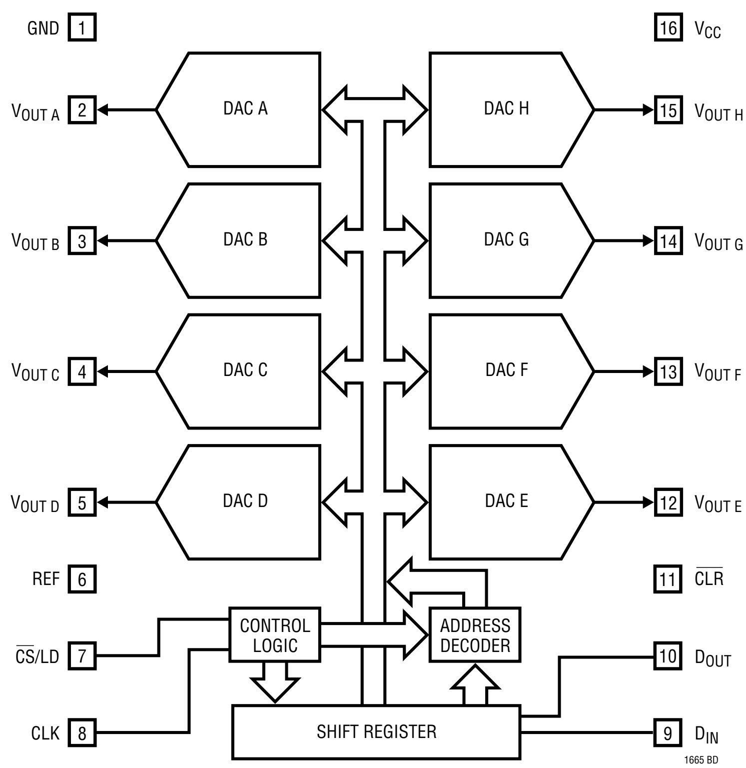
$$LSB = V_{REF}/256$$

Resolution (n): Defines the number of DAC output states (2^n) that divide the full-scale range. Resolution does not imply linearity.

Voltage Offset Error (V_{OS}): Nominally, the voltage at the output when the DAC is loaded with all zeros. A single supply DAC can have a true negative offset, but the output cannot go below zero (see Applications Information).

For this reason, single supply DAC offset is measured at the lowest code that guarantees the output will be greater than zero.

BLOCK DIAGRAM



TIMING DIAGRAM

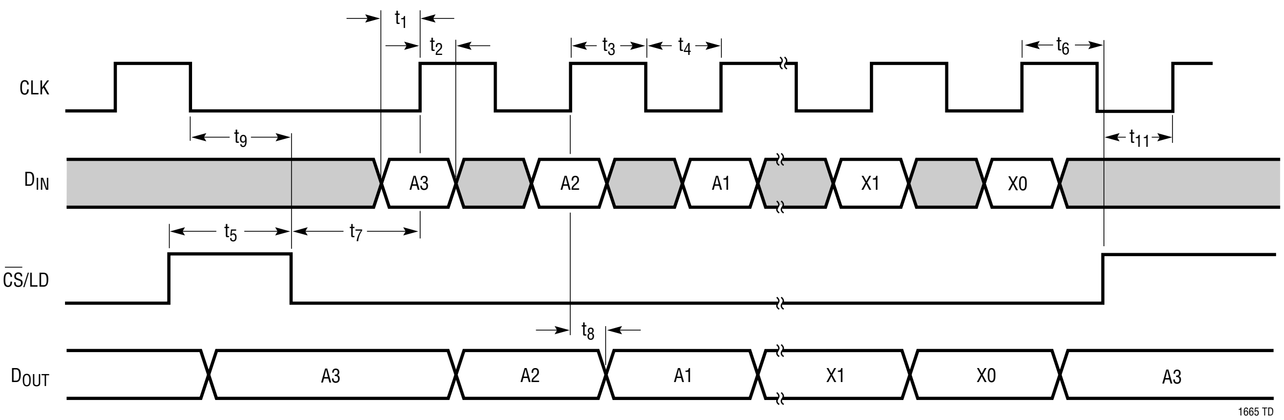


Figure 1

OPERATION

Transfer Function

The ideal transfer function for the LTC1665 is

$$V_{OUT(IDEAL)} = \left(\frac{k}{256}\right)V_{REF}$$

where k is the decimal equivalent of the binary DAC input code D7-D0 and V_{REF} is the voltage at REF (Pin 6).

Power-On Reset

The LTC1665 positively clears the outputs to zero scale when power is first applied, making system initialization consistent and repeatable.

Power Supply Sequencing

The voltage at REF (Pin 6) must not ever exceed the voltage at V_{CC} (Pin 16) by more than 0.2V. Particular care should be taken to assure that this limit is observed during power supply turn-on and turn-off sequences. See Absolute Maximum Ratings section.

Serial Interface

Referring to Figure 2: With $\overline{CS}$/LD held low, data on the D_{IN} input is shifted into the 16-bit shift register on the positive edge of CLK. The 4-bit DAC address, A3-A0, is loaded first (see Table 2), then the 8-bit input code, D7-D0, ordered MSB-to-LSB in each case. Four don't-care bits, X3-X0, are loaded last. When the full 16-bit word has been shifted in, $\overline{CS}$/LD is pulled high, loading the DAC register with the word and causing the addressed DAC output(s) to update. The clock is disabled internally when $\overline{CS}$/LD is high. Note: CLK must be low before $\overline{CS}$/LD is pulled low.

The buffered serial output of the shift register is available on the D_{OUT} pin, which swings from GND to V_{CC}. Data appears on D_{OUT} 16 positive CLK edges after being applied to D_{IN}.

Multiple LTC1665's can be controlled from a single 3-wire serial port (i.e., CLK, D_{IN} and $\overline{CS}$/LD) by using the included "daisy-chain" facility. A series of *m* chips is configured by connecting each D_{OUT} (except the last) to D_{IN} of the next chip, forming a single 16*m*-bit shift register. The CLK and $\overline{CS}$/LD signals are common to all chips in the chain. In use, $\overline{CS}$/LD is held low while *m* 16-bit words are clocked to D_{IN} of the first chip; $\overline{CS}$/LD is then pulled high, updating all of them simultaneously.

Sleep Mode

DAC address 1110_b is reserved for the special Sleep instruction (see Table 2). In this mode, internal bias currents are disabled while all digital circuitry stays fully active; static power consumption is thus virtually eliminated. The analog outputs are set in a high impedance state and all DAC settings are retained in memory so that when Sleep mode is exited, the outputs of DACs not updated by the Wake command are restored to their last active state.

OPERATION

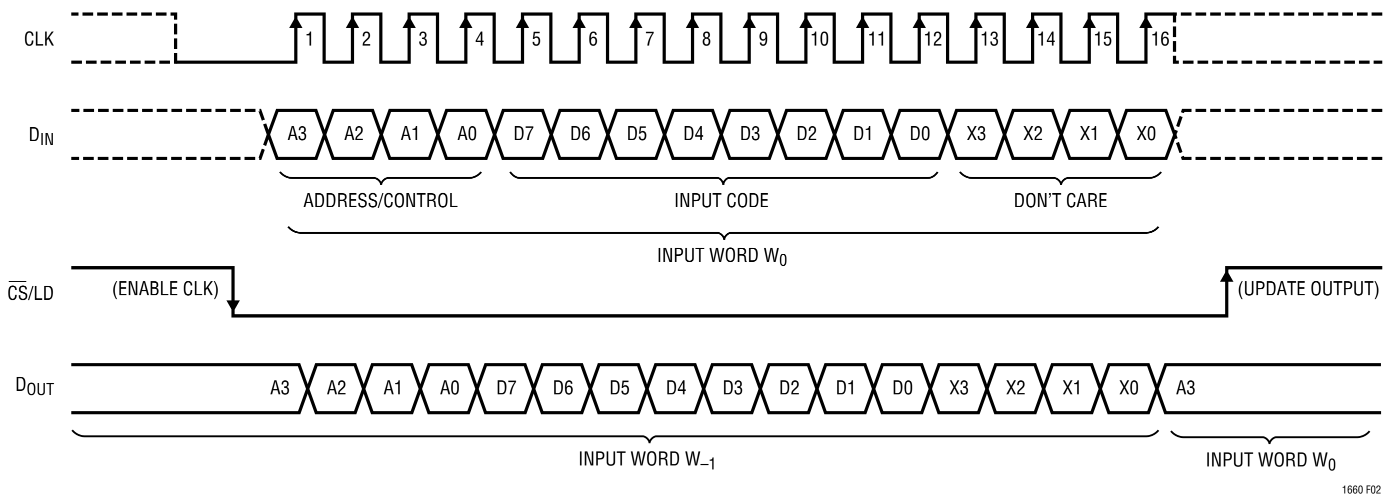


Figure 2. Register Loading Sequence

Table 1. LTC1665 Input Word

A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	X3	X2	X1	X0
Address/Control				Input Code								Don't Care			

Sleep mode is initiated by performing a load sequence to address 1110_b (the DAC input word D7-D0 is ignored). Once in Sleep mode, a load sequence to any other address (including "No Change" addresses 0000_b and $1001\text{-}1101_b$) causes the LTC1665 to Wake. It is possible to keep one or more chips of a daisy chain in continuous Sleep mode by giving the Sleep instruction to these chips each time the active chips in the chain are updated.

Voltage Outputs

Each of the eight rail-to-rail output amplifiers contained in the LTC1665 can source or sink up to 5mA. The outputs swing to within a few millivolts of either supply rail when unloaded and have an equivalent output resistance of 85Ω when driving a load to the rails. The output amplifiers are stable driving capacitive loads up to 1000pF.

A small resistor placed in series with the output can be used to achieve stability for any load capacitance. For example, a 0.1μF load can be successfully driven by inserting a 110Ω resistor. The phase margin of the resulting circuit is 45°, and increases monotonically from this point if larger values of resistance, capacitance or both are substituted for the values given.

Table 2. DAC Address/Control Functions

ADDRESS/CONTROL				DAC STATUS	SLEEP STATUS
A3	**A2**	**A1**	**A0**		
0	0	0	0	No Change	Wake
0	0	0	1	Load DAC A	Wake
0	0	1	0	Load DAC B	Wake
0	0	1	1	Load DAC C	Wake
0	1	0	0	Load DAC D	Wake
0	1	0	1	Load DAC E	Wake
0	1	1	0	Load DAC F	Wake
0	1	1	1	Load DAC G	Wake
1	0	0	0	Load DAC H	Wake
1	0	0	1	No Change	Wake
1	0	1	0	No Change	Wake
1	0	1	1	No Change	Wake
1	1	0	0	No Change	Wake
1	1	0	1	No Change	Wake
1	**1**	**1**	**0**	**No Change**	**Sleep**
1	1	1	1	Load **ALL** DACs with Same 8-Bit Code	Wake

APPLICATIONS INFORMATION

Rail-to-Rail Output Considerations

In any rail-to-rail DAC, the output is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 3b.

Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 3c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

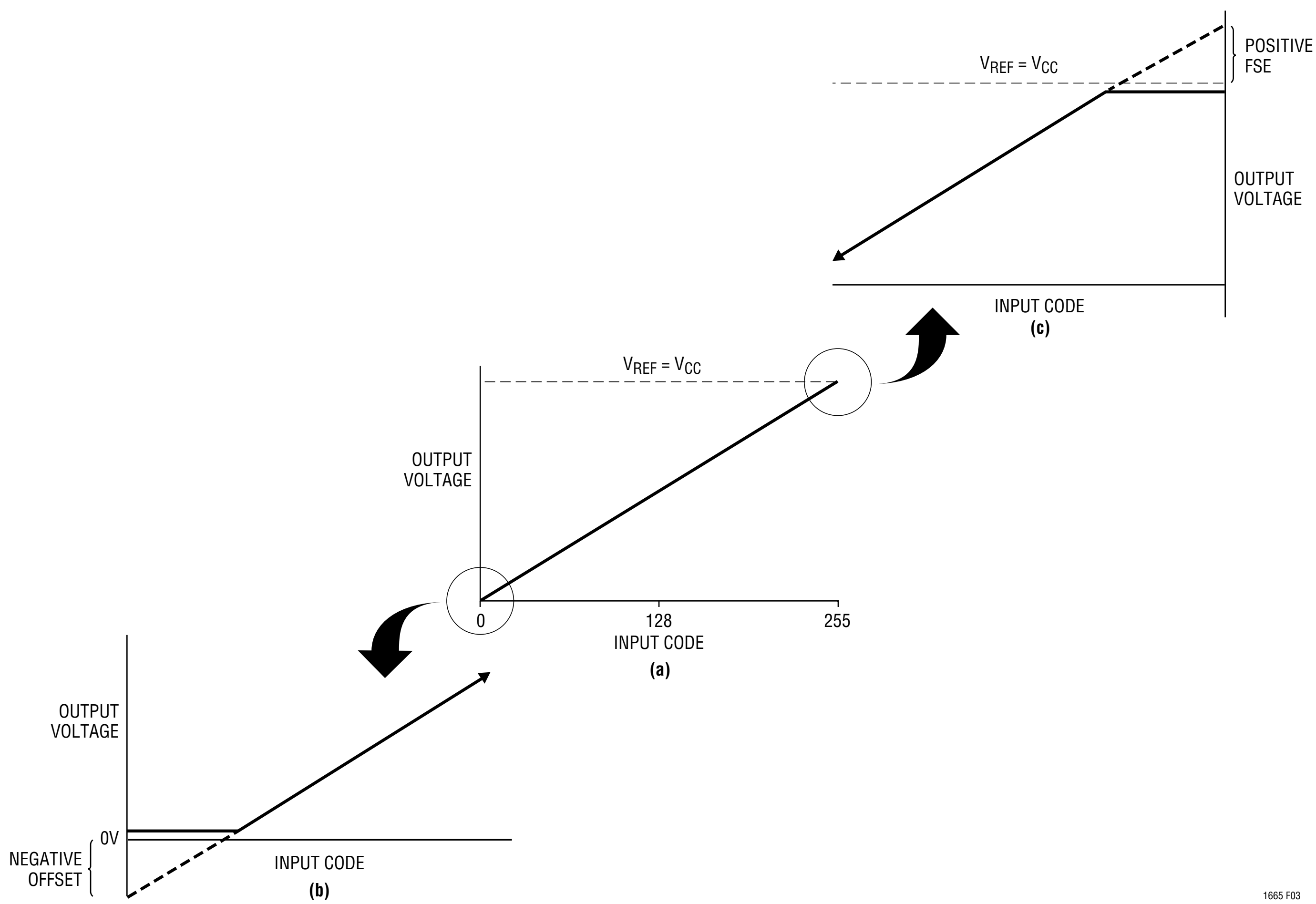
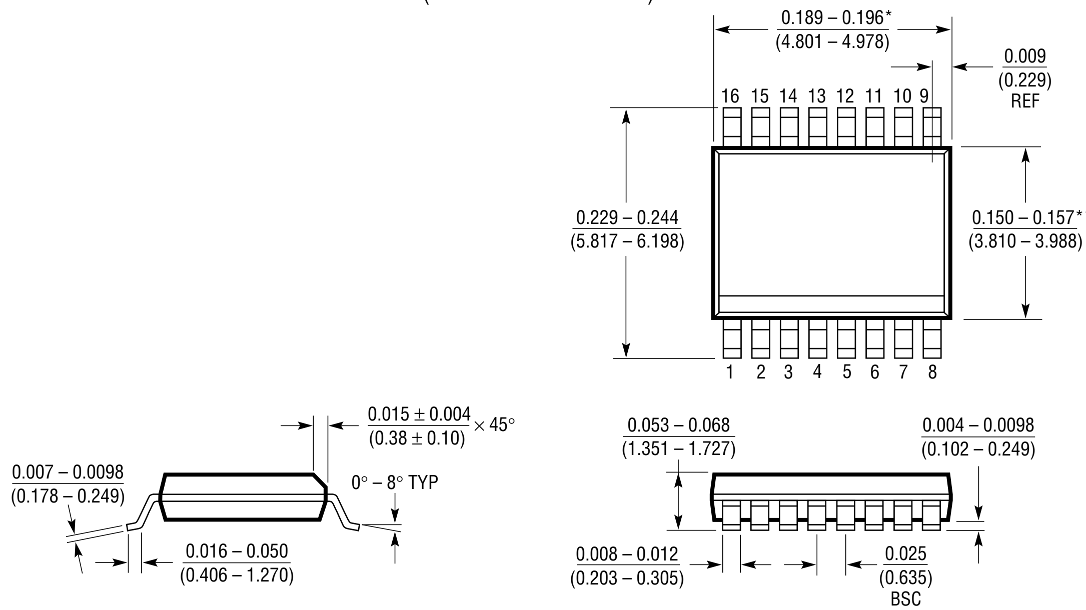


Figure 3. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When $V_{REF} = V_{CC}$

PACKAGE DESCRIPTION
Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)

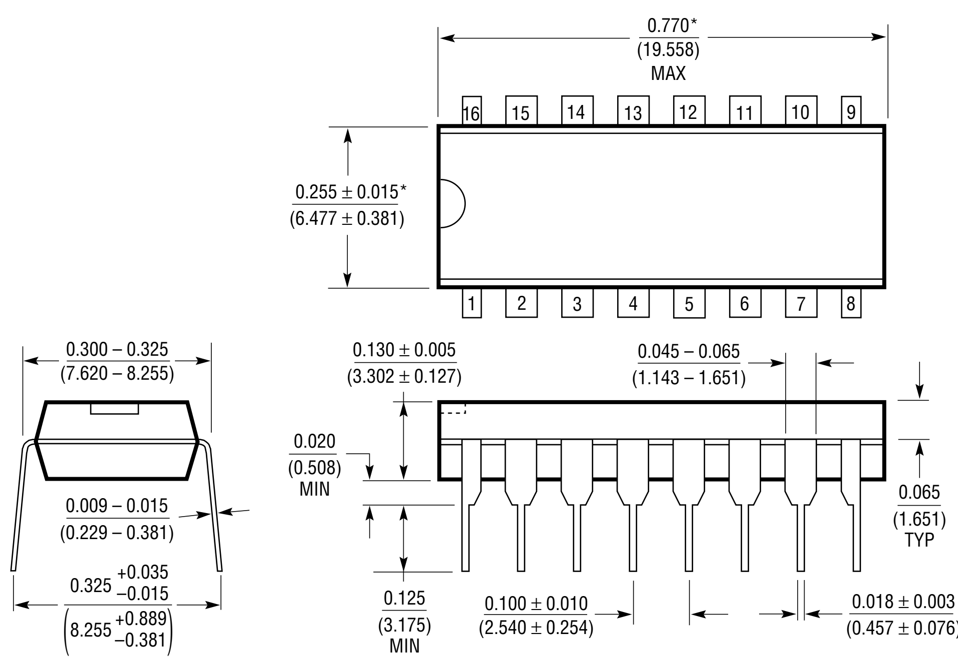


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0398

N Package
16-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

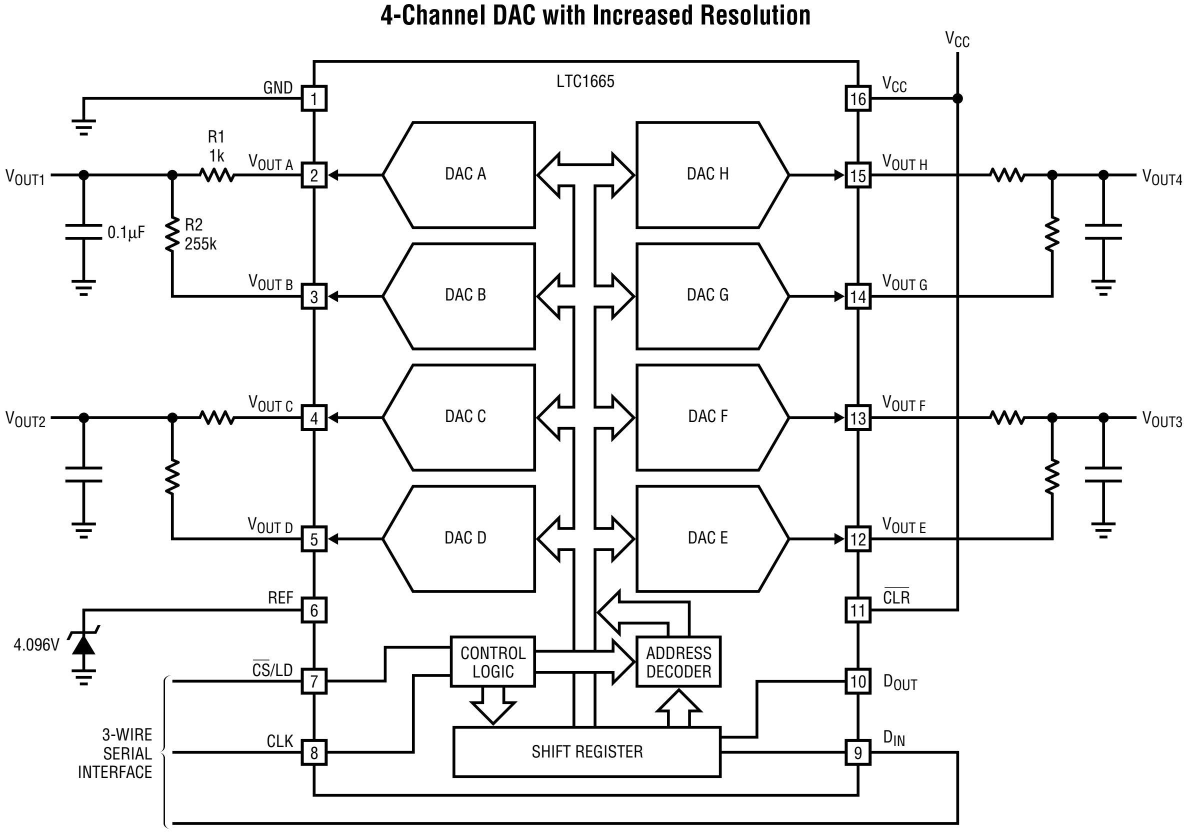


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N16 1197

TYPICAL APPLICATION

4-Channel DAC with Increased Resolution



$$V_{OUT1} = \frac{V_{REF}}{256}\left[\left(\frac{R2}{R1 + R2}\right)CODE_A + \left(\frac{R1}{R1 + R2}\right)CODE_B\right]$$

$$= \frac{4.096}{256}\left[\frac{255}{256}\ CODE_A + \frac{1}{256}\ CODE_B\right]$$

1665 TA01

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1660	Octal 10-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V Micropower Rail-to-Rail Output
LTC1661	Dual 10-Bit V_{OUT} DAC in 8-Lead MSOP Package	V_{CC} = 2.7V to 5.5V Micropower Rail-to-Rail Output
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package with Internal Reference	LTC1446: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1448	Dual 12-Bit V_{OUT} DAC in SO-8 Package	V_{CC} = 2.7V to 5.5V, External Reference Can Be Tied to V_{CC}
LTC1454/LTC1454L	Dual 12-Bit V_{OUT} DACs in SO-16 Package with Added Functionality	LTC1454: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1454L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1590	Dual 12-Bit I_{OUT} DAC in SO-16 Package	V_{CC} = 4.5V to 5.5V, 4-Quadrant Multiplication
LTC1659	Single Rail-to-Rail 12-Bit V_{OUT} DAC in 8-Lead MSOP Package V_{CC}: 2.7V to 5.5V	Low Power Multiplying V_{OUT} DAC. Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}
LT1460	Micropower Precision Series Reference, 2.5V, 5V, 10V Versions	0.075% Max, 10ppm/°C Max, Only 130µA Supply Current

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