

Advance InformationMPC8280EC/D
Rev. 0.2, 11/2002MPC8280
Hardware Specifications**MOTOROLA**
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This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for .13μm (HiP7) members of the PowerQUICC II™ family of integrated communications processors—the MPC8280 and the MPC8270 (collectively referred to throughout this document as the MPC8280).

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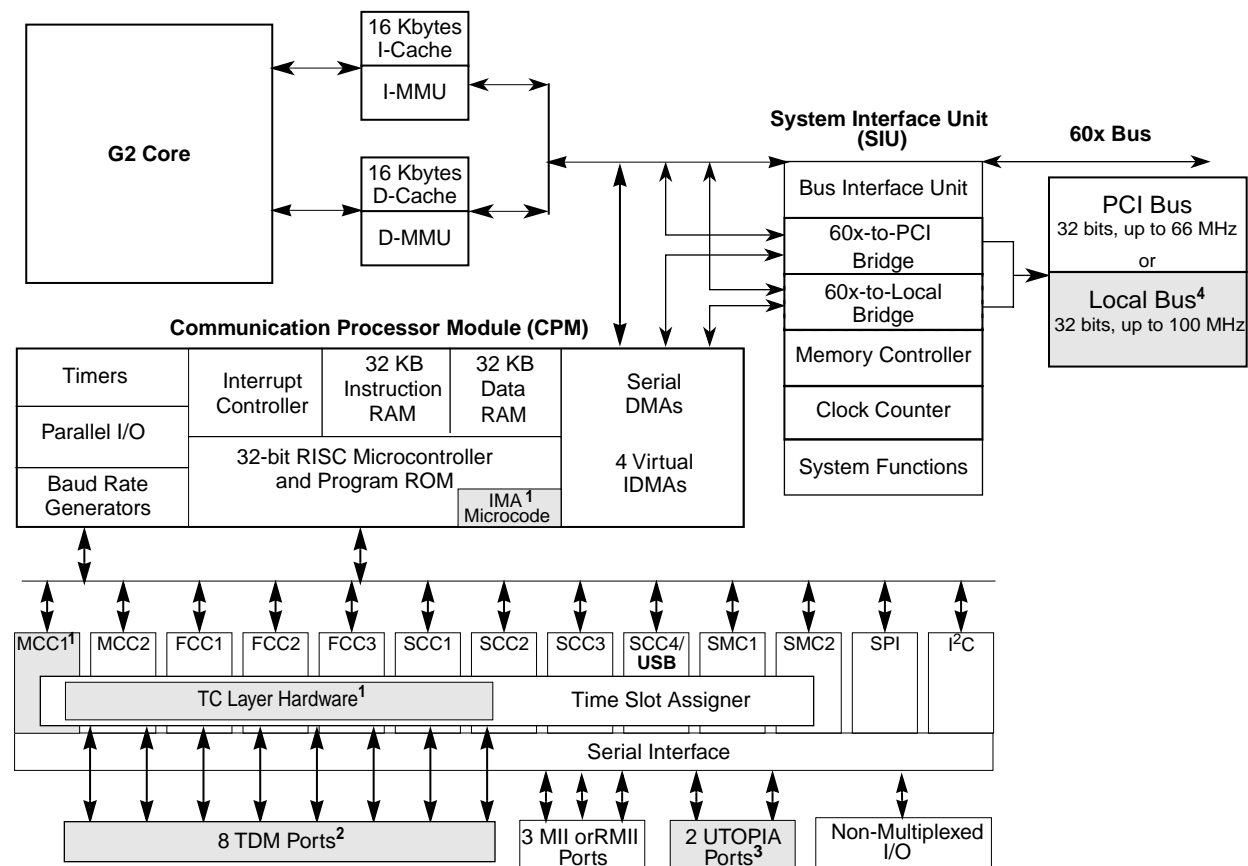
HiP7 members of the PowerQUICC II™ family are available in two packages—the standard ZU package and an alternate VR package—as shown in Table 1. For more information on VR packages, contact your Motorola sales office. Note that throughout this document references to the MPC8280 are inclusive of VR-package devices unless otherwise specified.

Table 1. HiP7 PowerQUICC II Device Packages

ZU (480 TBGA)	VR (516 PBGA)
MPC8280	—
—	MPC8275VR
MPC8270	MPC8270VR

Features

Figure 1 shows the block diagram for the MPC8280. Shaded portions are device- or package-specific; refer to the notes below.



Notes:

- ¹ MPC8280 only (not on MPC8270 nor the VR package (MPC8270VR and MPC8275VR))
- ² MPC8280 only (4 TDMs on MPC8270 and the VR package (MPC8270VR and MPC8275VR))
- ³ MPC8280 and MPC8275VR only (not on MPC8270 nor MPC8270VR)
- ⁴ No local bus on the VR package (MPC8270VR and MPC8275VR)

Figure 1. MPC8280 Block Diagram

1.1 Features

The major features of the MPC8280 are as follows:

- Dual-issue integer (G2) core
 - A core version of the EC603e microprocessor
 - System core microprocessor supporting frequencies of 150–450 MHz
 - Separate 16-Kbyte data and instruction caches:
 - Four-way set associative
 - Physically addressed
 - LRU replacement algorithm
 - PowerPC architecture-compliant memory management unit (MMU)
 - Common on-chip processor (COP) test interface

- High-performance (855 Dhrystones MIPS at 450 MHz)
- Supports bus snooping for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
 - G2 core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1 ratios
 - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
 - Programmable host bridge and agent
 - 32-bit data bus, 66.67/83.3/100 MHz, 3.3 V
 - Synchronous and asynchronous 60x and PCI clock modes
 - All internal address space available to external PCI host
 - DMA for memory block transfers
 - PCI-to-60x address remapping
- PCI bridge
 - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
 - On-chip arbitration
 - Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming
 - PCI Host Bridge or Peripheral capabilities
 - Includes 4 DMA channels for the following transfers:
 - PCI-to-60x to 60x-to-PCI
 - 60x-to-PCI to PCI-to-60x
 - PCI-to-60x to PCI-to-60x
 - 60x-to-PCI to 60x-to-PCI
 - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8280) required by the PCI standard as well as message and doorbell registers
 - Supports the I₂O standard
 - Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0)

Features

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- Support for 66.67/83.33/100 MHz, 3.3 V specification
- 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
- Makes use of the local bus signals, so there is no need for additional pins
- System interface unit (SIU)
 - Clock synthesizer
 - Reset controller
 - Real-time clock (RTC) register
 - Periodic interrupt timer
 - Hardware bus monitor and software watchdog timer
 - IEEE 1149.1 JTAG test access port
- Twelve-bank memory controller
 - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
 - Byte write enables and selectable parity generation
 - 32-bit address decodes with programmable bank size
 - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
 - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
 - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
 - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
 - Interfaces to G2 core through an on-chip 32-Kbyte dual-port data RAM, an on-chip 32-Kbyte dual-port instruction RAM and DMA controller
 - Serial DMA channels for receive and transmit on all serial channels
 - Parallel I/O registers with open-drain and interrupt capability
 - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
 - Three fast communications controllers supporting the following protocols:
 - 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII) or reduced media independent interface (RMII)
 - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections (no ATM support for the MPC8270)
 - Transparent
 - HDLC—Up to T3 rates (clear channel)
 - FCC2 can also be connected to the TC layer (MPC8280 only)
 - Two multichannel controllers (MCCs) (one MCC on the MPC8270)
 - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split

- into four subgroups of 32 channels each.
- Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
- Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
 - Ethernet/IEEE 802.3 CDMA/CS
 - HDLC/SDLC and HDLC bus
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Binary synchronous (BISYNC) communications
 - Transparent
- Universal serial bus (USB) controller—supports both host and slave modes
- Two serial management controllers (SMCs), identical to those of the MPC860
 - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
 - Transparent
 - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One inter-integrated circuit (I²C) controller (identical to the MPC860 I²C controller)
 - Microwire compatible
 - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8270)
 - Supports two groups of four TDM channels for a total of eight TDMs (one group of four on the MPC8270)
 - 2,048 bytes of SI RAM
 - Bit or byte resolution
 - Independent transmit and receive routing, frame synchronization
 - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Motorola interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers
- Inverse multiplexing for ATM capabilities (IMA) (MPC8280 only).Supported by eight transfer transmission convergence (TC) layers between the TDMs and FCC2.
- Transmission convergence (TC) layer (MPC8280 only)

Electrical and Thermal Characteristics

1.2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC8280.

1.2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC8280. Table 2 shows the maximum electrical ratings.

Table 2. Absolute Maximum Ratings¹

Rating	Symbol	Value	Unit
Core supply voltage ²	VDD	-0.3 – 2.25	V
PLL supply voltage ²	VCCSYN	-0.3 – 2.25	V
I/O supply voltage ³	VDDH	-0.3 – 4.0	V
Input voltage ⁴	VIN	GND(-0.3) – 3.6	V
Junction temperature	T _j	120	°C
Storage temperature range	T _{STG}	(-55) – (+150)	°C

¹ Absolute maximum ratings are stress ratings only; functional operation (see Table 3) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

² **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.

³ **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

⁴ **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 3 lists recommended operational voltage conditions.

Table 3. Recommended Operating Conditions¹

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.425 – 1.575	V
PLL supply voltage	VCCSYN	1.425 – 1.575	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (-0.3) – 3.465	V
Junction temperature (maximum)	T _j	105 ²	°C
Ambient temperature	T _A	0–70 ²	°C

¹ **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

² Note that for extended temperature parts the range is (-40)_{T_A} – 105_{T_j}.

NOTE

VDDH and VDD must track each other and both must vary in the same direction—in the positive direction (+0.165 VDDH and +0.075 VDD) or in the negative direction (-0.165 VDDH and -0.075 VDD).

Electrical and Thermal Characteristics

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Table 4 shows DC electrical characteristics.

Table 4. DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, $V_{IN} = V_{DDH}^1$	I_{IN}	—	10	μA
Hi-Z (off state) leakage current, $V_{IN} = V_{DDH}^1$	I_{OZ}	—	10	μA
Signal low input current, $V_{IL} = 0.8$ V	I_L	—	1	μA
Signal high input current, $V_{IH} = 2.0$ V	I_H	—	1	μA
Output high voltage, $I_{OH} = -2$ mA except UTOPIA mode, and open drain pins In UTOPIA mode ² (UTOPIA pins only): $I_{OH} = -8.0$ mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OH}	2.4	—	V
In UTOPIA mode ² (UTOPIA pins only): $I_{OL} = 8.0$ mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OL}	—	0.5	V

Electrical and Thermal Characteristics

Table 4. DC Electrical Characteristics (Continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 7.0\text{mA}$ $\overline{\text{BR}}$ $\overline{\text{BG}}$ $\overline{\text{ABB/IRQ2}}$ $\overline{\text{TS}}$ $\text{A}[0-31]$ $\text{TT}[0-4]$ $\overline{\text{TBST}}$ $\text{TSIZE}[0-3]$ $\overline{\text{AACK}}$ $\overline{\text{ARTRY}}$ $\overline{\text{DBG}}$ $\overline{\text{DBB/IRQ3}}$ $\text{D}[0-63]$ $\text{DP}(0)/\overline{\text{RSRV/EXT_BR2}}$ $\text{DP}(1)/\overline{\text{IRQ1/EXT_BG2}}$ $\text{DP}(2)/\overline{\text{TLBISYNC/IRQ2/EXT_DBG2}}$ $\text{DP}(3)/\overline{\text{IRQ3/EXT_BR3/CKSTP_OUT}}$ $\text{DP}(4)/\overline{\text{IRQ4/EXT_BG3/CORE_SREST}}$ $\text{DP}(5)/\overline{\text{TBEN/IRQ5/EXT_DBG3}}$ $\text{DP}(6)/\overline{\text{CSE}(0)/\text{IRQ6}}$ $\text{DP}(7)/\overline{\text{CSE}(1)/\text{IRQ7}}$ $\overline{\text{PSDVAL}}$ $\overline{\text{TA}}$ $\overline{\text{TEA}}$ $\overline{\text{GBL/IRQ1}}$ $\overline{\text{CI/BADDR29/IRQ2}}$ $\overline{\text{WT/BADDR30/IRQ3}}$ $\overline{\text{L2_HIT/IRQ4}}$ $\overline{\text{CPU_BG/BADDR31/IRQ5}}$ $\overline{\text{CPU_DBG}}$ $\overline{\text{CPU_BR}}$ $\overline{\text{IRQ0/NMI_OUT}}$ $\overline{\text{IRQ7/INT_OUT/APE}}$ $\overline{\text{PORESET}}$ $\overline{\text{HRESET}}$ $\overline{\text{SRESET}}$ $\overline{\text{RSTCONF}}$ $\overline{\text{QREQ}}$	V_{OL}	—	0.4	V

Table 4. DC Electrical Characteristics (Continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3\text{mA}$ $\overline{CS}[0-9]$ $\overline{CS}(10)/\overline{BCTL1}$ $\overline{CS}(11)/\overline{AP}(0)$ $\overline{BADDR}[27-28]$ \overline{ALE} $\overline{BCTL0}$ $\overline{PWE}[0-7]/\overline{PSDDQM}[0-7]/\overline{PBS}[0-7]$ $\overline{PSDA10}/\overline{PGPL0}$ $\overline{PSDWE}/\overline{PGPL1}$ $\overline{POE}/\overline{PSDRAS}/\overline{PGPL2}$ $\overline{PSDCAS}/\overline{PGPL3}$ $\overline{PGTA}/\overline{PUPMWAIT}/\overline{PGPL4}/\overline{PPBS}$ $\overline{PSDAMUX}/\overline{PGPL5}$ $\overline{LWE}[0-3]/\overline{LSDDQM}[0-3]/\overline{LBS}[0-3]/\overline{PCI_CFG}[0-3]$ $\overline{LSDA10}/\overline{LGPL0}/\overline{PCI_MODCKH0}$ $\overline{LSDWE}/\overline{LGPL1}/\overline{PCI_MODCKH1}$ $\overline{LOE}/\overline{LSDRAS}/\overline{LGPL2}/\overline{PCI_MODCKH2}$ $\overline{LSDCAS}/\overline{LGPL3}/\overline{PCI_MODCKH3}$ $\overline{LGTA}/\overline{LUPMWAIT}/\overline{LGPL4}/\overline{LPBS}$ $\overline{LSDAMUX}/\overline{LGPL5}/\overline{PCI_MODCK}$ \overline{LWR} $\overline{MODCK1}/\overline{AP}(1)/\overline{TC}(0)/\overline{BNKSEL}(0)$ $\overline{MODCK2}/\overline{AP}(2)/\overline{TC}(1)/\overline{BNKSEL}(1)$ $\overline{MODCK3}/\overline{AP}(3)/\overline{TC}(2)/\overline{BNKSEL}(2)$	V_{OL}	—	0.4	V
$I_{OL} = 3.2\text{mA}$ $\overline{L_A14}/\overline{PAR}$ $\overline{L_A15}/\overline{FRAME}/\overline{SMI}$ $\overline{L_A16}/\overline{TRDY}$ $\overline{L_A17}/\overline{IRDY}/\overline{CKSTP_OUT}$ $\overline{L_A18}/\overline{STOP}$ $\overline{L_A19}/\overline{DEVSEL}$ $\overline{L_A20}/\overline{IDSEL}$ $\overline{L_A21}/\overline{PERR}$ $\overline{L_A22}/\overline{SERR}$ $\overline{L_A23}/\overline{REQ0}$ $\overline{L_A24}/\overline{REQ1}/\overline{HSEJSW}$ $\overline{L_A25}/\overline{GNT0}$ $\overline{L_A26}/\overline{GNT1}/\overline{HSLED}$ $\overline{L_A27}/\overline{GNT2}/\overline{HSENUM}$ $\overline{L_A28}/\overline{RST}/\overline{CORE_SRESET}$ $\overline{L_A29}/\overline{INTA}$ $\overline{L_A30}/\overline{REQ2}$ $\overline{L_A31}$ $\overline{LCL_D}(0-31)/\overline{AD}(0-31)$ $\overline{LCL_DP}(0-3)/\overline{C}/\overline{BE}(0-3)$ $\overline{PA}[0-31]$ $\overline{PB}[4-31]$ $\overline{PC}[0-31]$ $\overline{PD}[4-31]$ \overline{TDO}				

¹ The leakage current is measured for nominal VDDH and VDD or both VDDH and VDD must vary in the same direction—VDDH and VDD must both vary in the positive direction (+0.165 VDDH and +0.075 VDD) or both vary in the negative direction (-0.165 VDDH and -0.075 VDD).

² MPC8280 only.

Electrical and Thermal Characteristics

1.2.2 Thermal Characteristics

Table 5 describes thermal characteristics for both the packages. Refer to Table 1 for information on a given device's package.

Table 5. Thermal Characteristics

Characteristic	Symbol	Value		Unit	Air Flow
		480 TBGA (ZU package)	516 PBGA (VR package)		
Junction to ambient— single-layer board ¹	θ_{JA}	13.07	27	°C/W	Natural convection
		9.55	21		1 m/s
Junction to ambient— four-layer board	θ_{JA}	10.48	19	°C/W	Natural convection
		7.78	16		1 m/s

¹ Assumes no thermal vias

1.2.2.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μ F by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC8280 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 6 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above $P_D = 3W$ (when the ambient temperature is 70° C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 6. Estimated Power Dissipation for Various Configurations¹

Bus (MHz)	CPM Multiplication Factor	CPM (MHz)	CPU Multiplication Factor	CPU (MHz)	$P_{INT}(W)^2$	
					V _{ddI} 1.5 Volts	
					Nominal	Maximum
83.33	3	250	4.5	350	1.0	1.2
83.33	3.5	292	5	417	1.1	1.3
83.33	4	333	6	500	1.3	1.5
100	3	300	4	400	1.1	1.3
100	3	300	4.5	450	1.2	1.45
100	3	300	5	500	1.25	1.5

¹ Test temperature = room temperature (25° C)² $P_{INT} = I_{DD} \times V_{DD}$ Watts

1.2.3 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100 MHz MPC8280 devices. Note that AC timings are based on a 50-pf load. Typical output buffer impedances are shown in Table 7.

Table 7. Output Buffer Impedances¹

Output Buffers	Typical Impedance (Ω)
60x bus	45
Local bus	45
Memory controller	45
Parallel I/O	45
PCI	25

¹ These are typical values at 65° C. Impedance may vary by $\pm 25\%$ with process and temperature.

Table 8 lists CPM output characteristics.

Table 8. AC Characteristics for CPM Outputs¹

Spec_num	Characteristic	Maximum Delay (ns)	Minimum Delay (ns)
sp36a	FCC outputs-internal clock (NMSI)	5.5	1
sp36b	FCC outputs-external clock (NMSI)	12	2
sp40	TDM outputs/SI	12	3
sp38a	SCC/SMC/SPI/I2C outputs-internal clock (NMSI)	16	0.5
sp38b	SCC/SMC/SPI/I2C outputs-external clock (NMSI)	16	2
sp42	PIO/TIMER/DMA outputs	11	1
sp43	COL width high (FCC)	—	1.5 CLK

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Electrical and Thermal Characteristics

Table 9 lists CPM input characteristics.

Table 9. AC Characteristics for CPM Inputs¹

Spec_num	Characteristic	Setup (ns)	Hold (ns)
sp16a/sp17a	FCC inputs-internal clock (NMSI)	8	0
sp16b/sp17b	FCC inputs-external clock (NMSI)	2.5	2
sp20/sp21	TDM inputs/SI	5	3
sp18a/sp19a	SCC/SMC/SPI/I2C inputs-internal clock (NMSI)	16	0
sp18b/sp19b	SCC/SMC/SPI/I2C inputs-external clock (NMSI)	4	2
sp22/sp23	PIO/TIMER/DMA inputs	8	1

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

NOTE

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 2 shows the FCC internal clock.

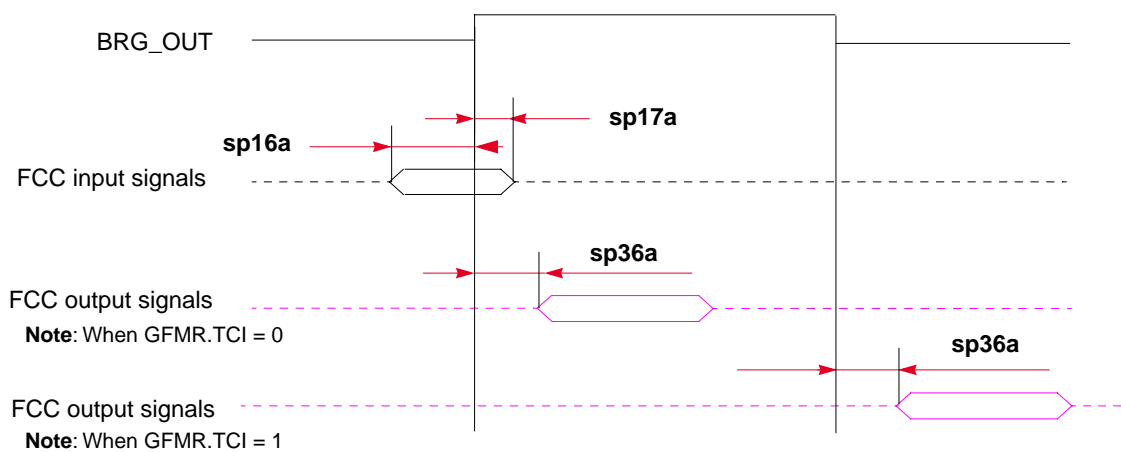


Figure 2. FCC Internal Clock Diagram

Figure 3 shows the FCC external clock.

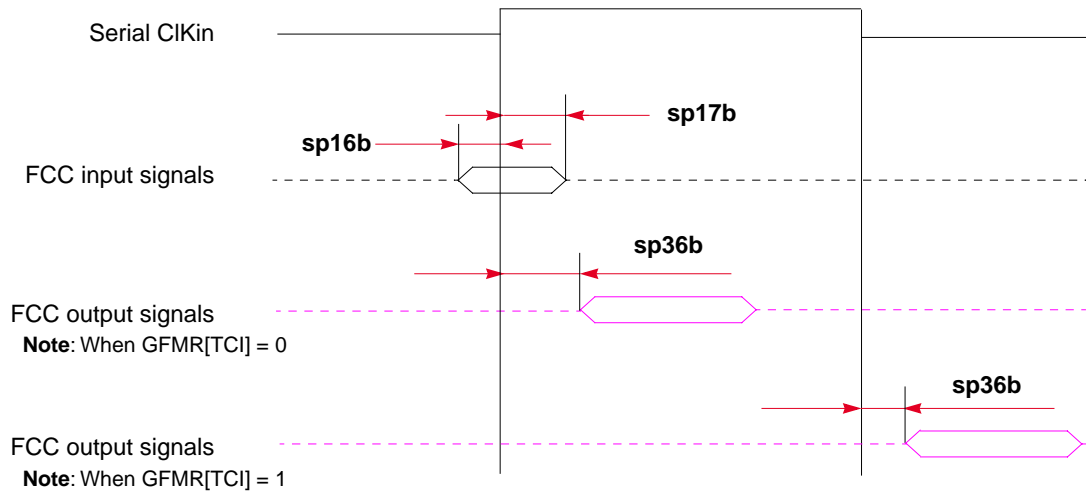


Figure 3. FCC External Clock Diagram

Figure 4 shows the SCC/SMC/SPI/I²C external clock.

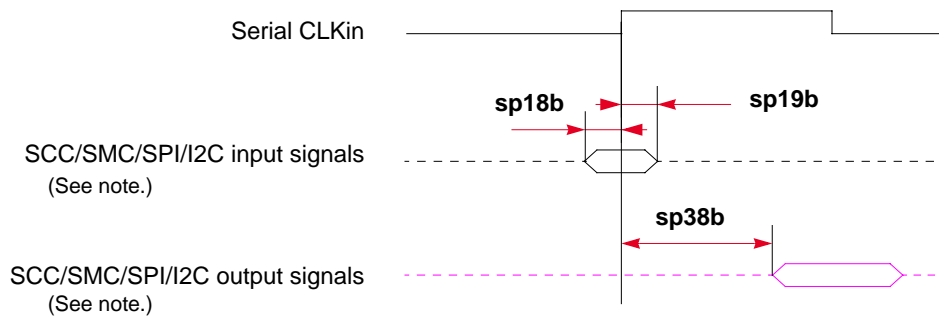


Figure 4. SCC/SMC/SPI/I²C External Clock Diagram

Figure 5 shows the SCC/SMC/SPI/I²C internal clock.

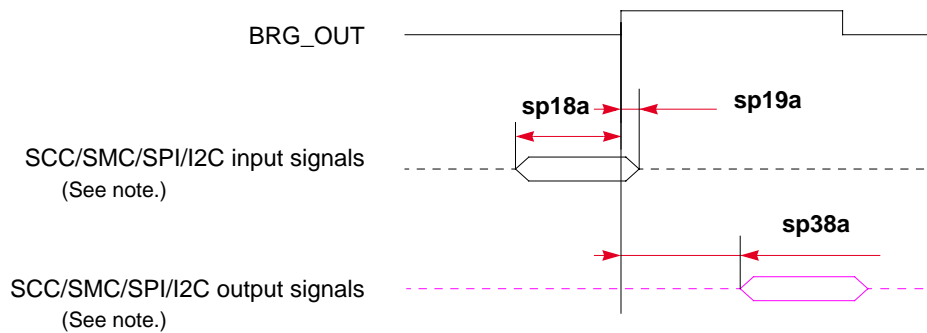
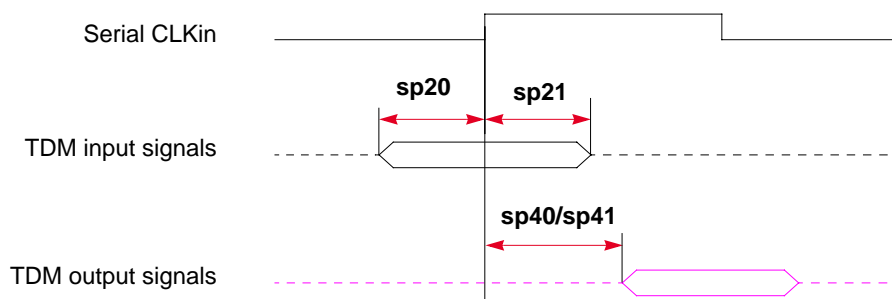


Figure 5. SCC/SMC/SPI/I²C Internal Clock Diagram

Electrical and Thermal Characteristics

Figure 6 shows TDM input and output signals.



Note: There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. TDM Signal Diagram

Figure 7 shows PIO and timer signals.

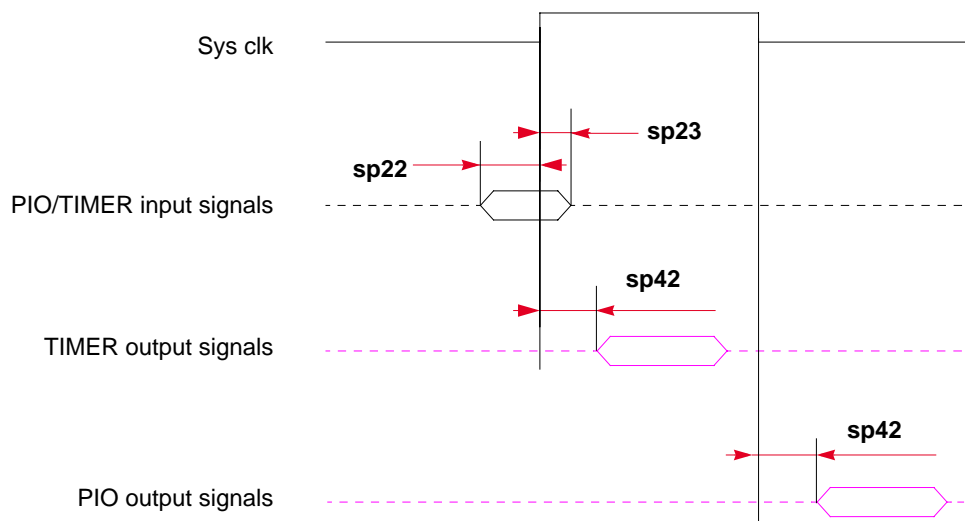


Figure 7. PIO and Timer Signal Diagram

Table 10 lists SIU input characteristics.

Electrical and Thermal Characteristics

Table 10. AC Characteristics for SIU Inputs¹

Spec_num	Characteristic	Setup (ns)			Hold (ns)		
		66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp11/sp10	AACK/TA/TS/DBG/BG/BR	6	5	3.5	0.5	0.5	0.5
sp11a/sp10	ARTRY/TEA	6	5	4	0.5	0.5	0.5
sp12/sp10	Data bus in normal mode	5	4	3.5	0.5	0.5	0.5
sp13/sp10	Data bus in ECC and PARITY modes	8	6	3.5	0.5	0.5	0.5
sp13a/sp10	Pipeline mode— Data bus in ECC and PARITY modes	—	4	2.5	0.5	0.5	0.5
sp14/sp10	DP pins	7	6	3.5	0.5	0.5	0.5
sp14a/sp10	Pipeline mode—DP pins	—	4	2.5	0.5	0.5	0.5
sp15/sp10	All other pins	5	4	3.5	0.5	0.5	0.5

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 11 lists SIU output characteristics.

Table 11. AC Characteristics for SIU Outputs¹

Spec_num (max/min)	Characteristic	Maximum Delay (ns)			Minimum Delay (ns)		
		66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp31/sp30	PSDVAL/TEA/TA	7	6	5.5	0.5	0.5	0.5
sp32/sp30	ADD/ADD_atr./BADDR/CI/GBL/WT ^{2,3}	8	6.5	5.5	0.5 ²	0.5 ²	0.5 ²
sp33a/sp30	Data bus ^{2, 3}	6.5	6.5	5.5	0.5 ²	0.5 ²	0.5 ²
sp33b/sp30	DP	8	7	6	1	1	1
sp34/sp30	Memory controller signals/ALE ²	6	5.5	5.5	0.5 ²	0.5 ²	0.5 ²
sp35/sp30	All other signals ²	6	5.5	5.5	0.5 ²	0.5 ²	0.5 ²
sp35a/sp30	AP	7	7	7	0.5	0.5	0.5

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

² The signals in **boldface** have a minimum delay of 1 ns at 66.67/83.33/100 MHz when communicating to SDRAM:

A[0–31]	LCL_D[0–31]	OE/SDRAS/GP12	LSDCAS/GP13
BADDR[27–31]	LCL_DP[0–3]	SDCAS/GP13	MODCLK[1–3]/AP[1–3]/TC[0–2]/BNKSEL[0–2]
D[0–63]	CS[0–11]	LSDA10/GP10	LWE[0–3]/LSDDQM[0–3]/LBS[0–3]
DP[0–7]	SDA10/GP10	LSWE/GP11	PWE[0–7]/PSDDQM[0–7]/PBS[0–7]
L_A[14–31]	SDWE/GP11	LOE/LSDRAS/GP12	

³ A minimum loading of 20 pF is required to meet 1 ns hold time for communicating to SDRAM.

NOTE

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing. Also, sp33a can be used as the AC specification for DP signals.

Electrical and Thermal Characteristics

Figure 8 shows the interaction of several bus signals.

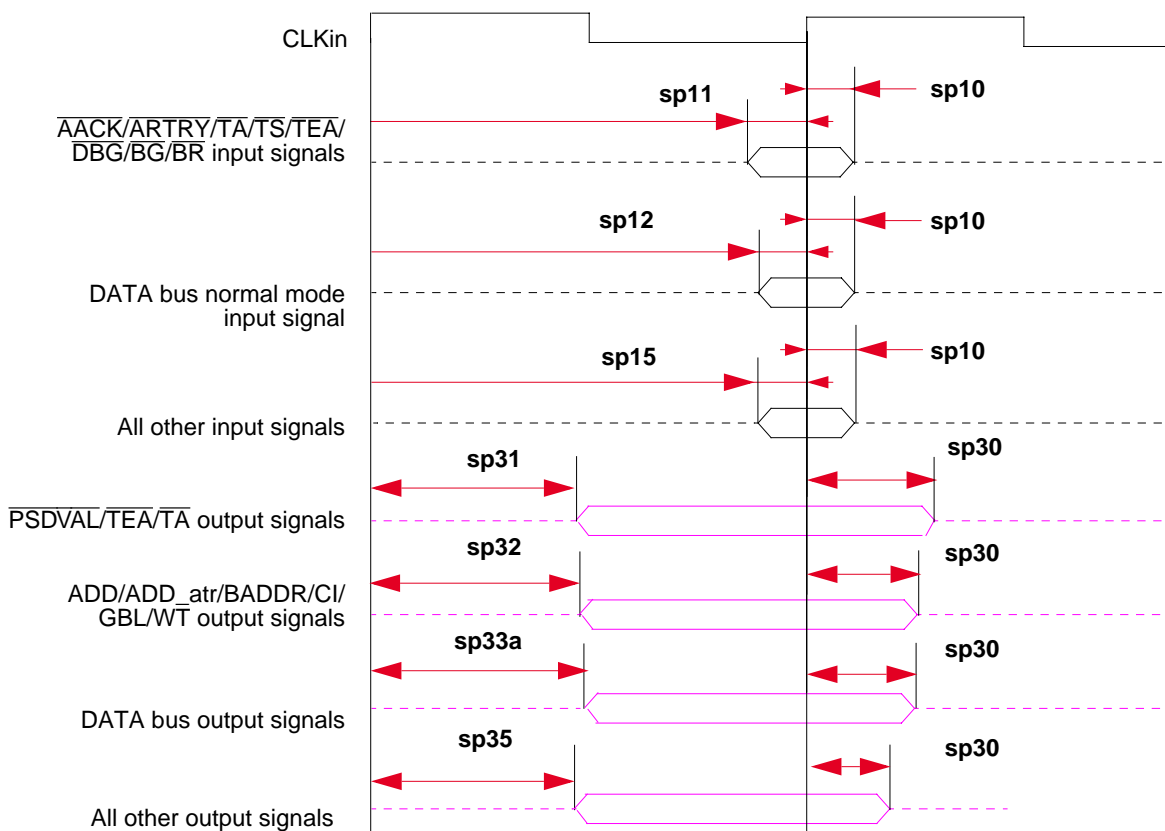


Figure 8. Bus Signals

Figure 9 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

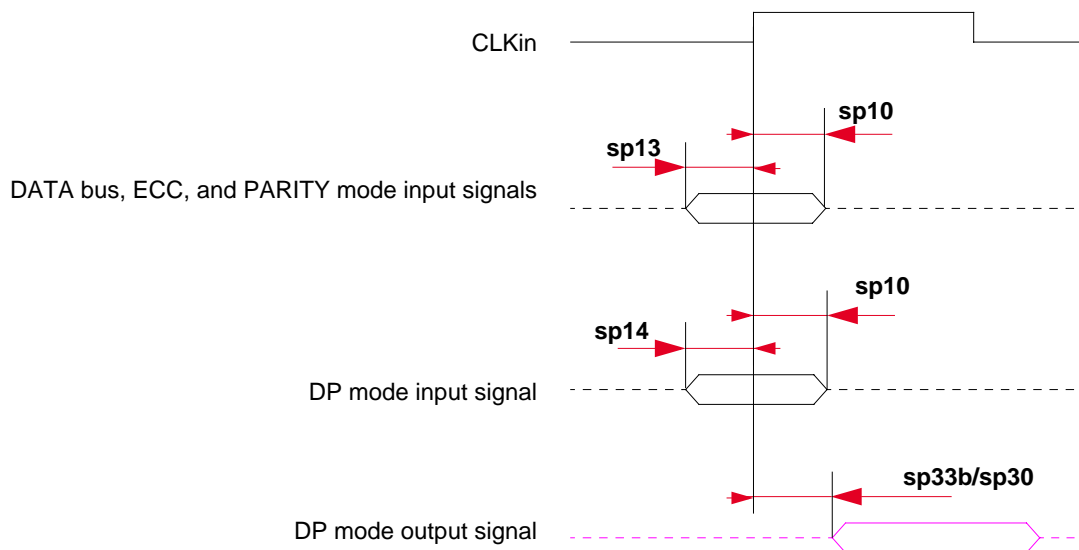


Figure 9. Parity Mode Diagram

Figure 10 shows signal behavior in MEMC mode.

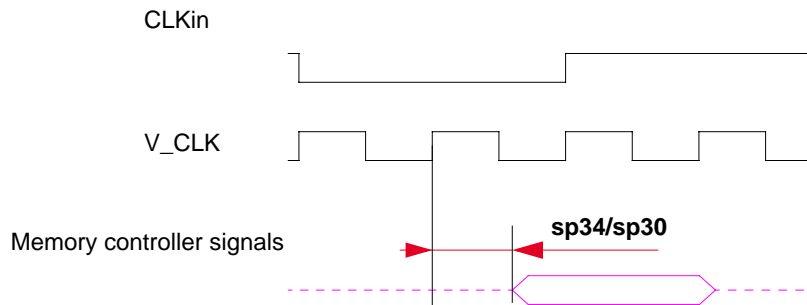


Figure 10. MEMC Mode Diagram

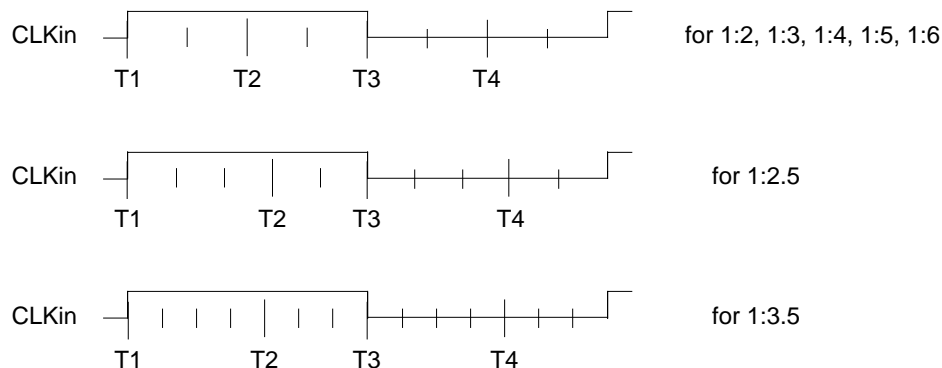
NOTE

Generally, all MPC8280 bus and system output signals are driven from the rising edge of the input clock (CLKIn). Memory controller signals, however, trigger on four points within a CLKIn cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKIn. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 12.

Table 12. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKIn)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKIn	1/2 CLKIn	3/4 CLKIn
1:2.5	3/10 CLKIn	1/2 CLKIn	8/10 CLKIn
1:3.5	4/14 CLKIn	1/2 CLKIn	11/14 CLKIn

Figure 11 is a representation of the information in Table 12.

**Figure 11. Internal Tick Spacing for Memory Controller Signals****NOTE**

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKIn's rising edge.

1.3 Clock Configuration Modes

The MPC8280 has three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins—PCI_MODE, PCI_CFG[0], PCI_MODCK—as shown in Table 13.

Table 13. MPC8280 Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK ¹			
1	—	—	Local bus	—	Table 14
0	0	0	PCI Host	50–66	Table 15
0	0	1		25–50	Table 16
0	1	0	PCI Agent	50–66	Table 17
0	1	1		25–50	Table 18

¹ Determines PCI clock frequency range. Refer to Section 1.3.2, “PCI Mode.”

In each clocking mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-up reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected MPC8280 clock operation mode as described in the following sections.

1.3.1 Local Bus Mode

Table 14 lists default and full configurations for the MPC8280 in local bus mode.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

Note also that basic modes are shown in boldface type.

Table 14. Local Bus Clock Modes

Mode ¹	Bus Clock ^{2,3} (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)	
	low	high		low	high		low	high
MODCK_H-MODCK[1-3]								
Default Modes (MODCK_H= 0000)								
0000_000	62.5	133.3	3	187.5	400.0	4	250.0	533.3
0000_001	50.0	133.3	3	150.0	400.0	5	250.0	666.7
0000_010	62.5	100.0	4	250.0	400.0	4	250.0	400.0
0000_011	50.0	100.0	4	200.0	400.0	5	250.0	500.0
0000_100	50.0	167.0	2	100.0	334.0	2.5	125.0	417.5
0000_101	50.0	167.0	2	100.0	334.0	3	150.0	501.0
0000_110	50.0	160.0	2.5	125.0	400.0	2.5	125.0	400.0
0000_111	41.7	160.0	2.5	104.2	400.0	3	125.0	480.0
Full Configuration Modes								

Clock Configuration Modes

Table 14. Local Bus Clock Modes (Continued)

Mode ¹	Bus Clock ^{2,3} (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)	
MODCK_H-MODCK[1-3]	low	high		low	high		low	high
0001_000	62.5	167.0	2	125.0	334.0	4	250.0	668.0
0001_001	50.0	167.0	2	100.0	334.0	5	250.0	835.0
0001_010	50.0	167.0	2	100.0	334.0	6	300.0	1002.0
0001_011	Reserved							
0001_100	Reserved							
0001_101	62.5	133.3	3	187.5	400.0	4	250.0	533.3
0001_110	50.0	133.3	3	150.0	400.0	5	250.0	666.7
1000_111	45.5	133.3	3	136.4	400.0	5.5	250.0	733.3
0001_111	41.7	133.3	3	125.0	400.0	6	250.0	800.0
0010_000	Reserved							
0010_001	Reserved							
0010_010	62.5	100.0	4	250.0	400.0	4	250.0	400.0
0010_011	50.0	100.0	4	200.0	400.0	5	250.0	500.0
0010_100	41.7	100.0	4	166.7	400.0	6	250.0	600.0
0010_101	35.7	100.0	4	142.9	400.0	7	250.0	700.0
0010_110	31.3	100.0	4	125.0	400.0	8	250.0	800.0
0010_111	Reserved							
0011_000	50.0	80.0	5	250.0	400.0	5	250.0	400.0
0011_001	41.7	80.0	5	208.3	400.0	6	250.0	480.0
0011_010	35.7	80.0	5	178.6	400.0	7	250.0	560.0
0011_011	31.3	80.0	5	156.3	400.0	8	250.0	640.0
0011_100	Reserved							
0011_101	Reserved							
0011_110	41.7	66.7	6	250.0	400.0	6	250.0	400.0
0011_111	35.7	66.7	6	214.3	400.0	7	250.0	466.7
0100_000	31.3	66.7	6	187.5	400.0	8	250.0	533.3
0101_101	62.5	167.0	2	125.0	334.0	2	125.0	334.0
0101_110	50.0	167.0	2	100.0	334.0	2.5	125.0	417.5
0101_111	50.0	167.0	2	100.0	334.0	3	150.0	501.0

Clock Configuration Modes

Table 14. Local Bus Clock Modes (Continued)

Mode ¹	Bus Clock ^{2,3} (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)	
	low	high		low	high		low	high
MODCK_H-MODCK[1-3]								
0110_000	71.4	167.0	2	142.9	334.0	3.5	250.0	584.5
0110_001	62.5	167.0	2	125.0	334.0	4	250.0	668.0
0110_010	55.6	167.0	2	111.1	334.0	4.5	250.0	751.5
0110_011	Reserved							
0110_100	50.0	160.0	2.5	125.0	400.0	2.5	125.0	400.0
0110_101	41.7	160.0	2.5	104.2	400.0	3	125.0	480.0
0110_110	71.4	160.0	2.5	178.6	400.0	3.5	250.0	560.0
0110_111	62.5	160.0	2.5	156.3	400.0	4	250.0	640.0
0111_000	55.6	160.0	2.5	138.9	400.0	4.5	250.0	720.0
0111_001	Reserved							
0111_010	Reserved							
0111_011	41.7	133.3	3	125.0	400.0	3	125.0	400.0
0111_100	71.4	133.3	3	214.3	400.0	3.5	250.0	466.7
0111_101	62.5	133.3	3	187.5	400.0	4	250.0	533.3
0111_110	55.6	133.3	3	166.7	400.0	4.5	250.0	600.0
0111_111	Reserved							
1000_000	Reserved							
1000_001	Reserved							
1000_010	71.4	114.3	3.5	250.0	400.0	3.5	250.0	400.0
1000_011	62.5	114.3	3.5	218.8	400.0	4	250.0	457.1
1000_100	55.6	114.3	3.5	194.4	400.0	4.5	250.0	514.3
1000_101	50.0	114.3	3.5	175.0	400.0	5	250.0	571.4
1000_110	45.5	114.3	3.5	159.1	400.0	5.5	250.0	628.6
1100_000	50.0	167.0	2	100.0	334.0	Bypass	50.0	167.0
1100_001	40.0	160.0	2.5	100.0	400.0	Bypass	40.0	160.0
1100_010	33.3	133.3	3	100.0	400.0	Bypass	33.3	133.3
1101_000	Reserved							

¹ MODCK_H = hard reset configuration word [28–31]. Refer to Section 5.4 in the *MPC8260 User's Manual*; MODCK[1-3] = three hardware configuration pins.

² 60x and local bus frequency. Identical to CLKIN.

³ 'High' and 'low' indicate frequency limits for a given configuration.

⁴ CPM multiplication factor = CPM clock/bus clock

⁵ CPU multiplication factor = Core PLL multiplication factor

1.3.2 PCI Mode

The following tables show the possible clock configurations for the MPC8280 in both PCI host and PCI agent modes. In addition, note the following:

NOTE

In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

NOTE

The minimum Tval = 2 when PCI_MODCK = 1 and minimum Tval = 1 when PCI_MODCK = 0; therefore, board designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

1.3.2.1 PCI Host Mode

Table 15 and Table 16 show configurations for PCI host mode. Note that the range of the PCI clock frequency is determined by PCI_MODCK.

Table 15. Clock Configurations for PCI Host Mode (PCI_MODCK=0)¹

Mode ²	Bus Clock ^{3,4} (MHz)		CPM Multiplication Factor ⁵	CPM Clock ⁴ (MHz)		CPU Multiplication Factor ⁶	CPU Clock ⁴ (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
Default Modes (MODCK_H=0000)											
0000_000	50.0	66.7	2	100.0	133.3	2.5	125.0	166.7	2	50.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0000_011	71.4	80.0	2.5	178.6	200.0	3.5	250.0	280.0	3	59.5	66.7
0000_100	62.5	80.0	2.5	156.3	200.0	4	250.0	320.0	3	52.1	66.7
0000_101	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_110	PCI host mode (PCI_MODCK=1) only (refer to Table 16)										
0000_111	62.5	66.7	3	187.5	200.0	4	250.0	266.6	3	62.5	66.7
Full Configuration Modes											
0001_000	50.0	66.7	3	150.0	200.0	5	250.0	333.3	3	50.0	66.7
0001_001	50.0	66.7	3	150.0	200.0	6	300.0	400.0	3	50.0	66.7
0001_010	50.0	66.7	3	150.0	200.0	7	350.0	466.6	3	50.0	66.7
0001_011	50.0	66.7	3	150.0	200.0	8	400.0	533.3	3	50.0	66.7

Clock Configuration Modes

Table 15. Clock Configurations for PCI Host Mode (PCI_MODCK=0)¹ (Continued)

Mode ²	Bus Clock ^{3,4} (MHz)		CPM Multiplication Factor ⁵	CPM Clock ⁴ (MHz)		CPU Multiplication Factor ⁶	CPU Clock ⁴ (MHz)		PCI Division Factor	PCI Clock (MHz)	
	low	high		low	high		low	high		low	high
MODCK_H-MODCK[1-3]											
0010_000	50.0	66.7	4	200.0	266.6	5	250.0	333.3	4	50.0	66.7
0010_001	50.0	66.7	4	200.0	266.6	6	300.0	400.0	4	50.0	66.7
0010_010	50.0	66.7	4	200.0	266.6	7	350.0	466.6	4	50.0	66.7
0010_011	50.0	66.7	4	200.0	266.6	8	400.0	533.3	4	50.0	66.7
0010_100	75.0	100.0	4	300.0	400.0	5	375.0	500.0	6	50.0	66.7
0010_101	75.0	100.0	4	300.0	400.0	5.5	412.5	549.9	6	50.0	66.7
0010_110	75.0	100.0	4	300.0	400.0	6	450.0	599.9	6	50.0	66.7
0011_000	50.0	66.7	5	250.0	333.3	5	250.0	333.3	5	50.0	66.7
0011_001	50.0	66.7	5	250.0	333.3	6	300.0	400.0	5	50.0	66.7
0011_010	50.0	66.7	5	250.0	333.3	7	350.0	466.6	5	50.0	66.7
0011_011	50.0	66.7	5	250.0	333.3	8	400.0	533.3	5	50.0	66.7
0100_000	Reserved										
0100_001	50.0	66.7	6	300.0	400.0	6	300.0	400.0	6	50.0	66.7
0100_010	50.0	66.7	6	300.0	400.0	7	350.0	466.6	6	50.0	66.7
0100_011	50.0	66.7	6	300.0	400.0	8	400.0	533.3	6	50.0	66.7
0101_000	50.0	66.7	2	100.0	133.3	2.5	125.0	166.7	2	50.0	66.7
0101_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0101_010	PCI host mode (PCI_MODCK=1) only (refer to Table 16)										
0101_011	62.5	66.7	2	125.0	133.3	4	250.0	266.6	2	62.5	66.7
0101_100	55.6	66.7	2	111.1	133.3	4.5	250.0	300.0	2	55.6	66.7
0110_000	60.0	80.0	2.5	150.0	200.0	2.5	150.0	200.0	3	50.0	66.7
0110_001	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0110_010	71.4	80.0	2.5	178.6	200.0	3.5	250.0	280.0	3	59.5	66.7
0110_011	62.5	80.0	2.5	156.3	200.0	4	250.0	320.0	3	52.1	66.7
0110_100	60.0	80.0	2.5	150.0	200.0	4.5	270.0	360.0	3	50.0	66.7
0110_101	60.0	80.0	2.5	150.0	200.0	5	300.0	400.0	3	50.0	66.7
0110_110	60.0	80.0	2.5	150.0	200.0	6	360.0	480.0	3	50.0	66.7

Clock Configuration Modes

Table 15. Clock Configurations for PCI Host Mode (PCI_MODCK=0)¹ (Continued)

Mode ²	Bus Clock ^{3,4} (MHz)		CPM Multiplication Factor ⁵	CPM Clock ⁴ (MHz)		CPU Multiplication Factor ⁶	CPU Clock ⁴ (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
0111_000	Reserved										
0111_001	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0111_010	PCI host mode (PCI_MODCK=1) only (refer to Table 16)										
0111_011	62.5	66.7	3	187.5	200.0	4	250.0	266.6	3	62.5	66.7
0111_100	55.6	66.7	3	166.7	200.0	4.5	250.0	300.0	3	55.6	66.7
1000_000	Reserved										
1000_001	66.7	88.9	3	200.0	266.6	3	200.0	266.6	4	50.0	66.7
1000_010	71.4	88.9	3	214.3	266.6	3.5	250.0	311.1	4	53.6	66.7
1000_011	66.7	88.9	3	200.0	266.6	4	266.7	355.5	4	50.0	66.7
1000_100	66.7	88.9	3	200.0	266.6	4.5	300.0	400.0	4	50.0	66.7
1000_101	66.7	88.9	3	200.0	266.6	6	400.0	533.3	4	50.0	66.7
1000_110	66.7	88.9	3	200.0	266.6	6.5	433.3	577.7	4	50.0	66.7
1001_000	57.1	76.2	3.5	200.0	266.6	2.5	142.9	190.5	4	50.0	66.7
1001_001	57.1	76.2	3.5	200.0	266.6	3	171.4	228.5	4	50.0	66.7
1001_010	71.4	76.2	3.5	250.0	266.6	3.5	250.0	266.6	4	62.5	66.7
1001_011	62.5	76.2	3.5	218.8	266.6	4	250.0	304.7	4	54.7	66.7
1001_100	57.1	76.2	3.5	200.0	266.6	4.5	257.1	342.8	4	50.0	66.7
1001_101	85.7	114.3	3.5	300.0	400.0	5	428.6	571.4	6	50.0	66.7
1001_110	85.7	114.3	3.5	300.0	400.0	5.5	471.4	628.5	6	50.0	66.7
1001_111	85.7	114.3	3.5	300.0	400.0	6	514.3	685.6	6	50.0	66.7
1010_000	75.0	100.0	2	150.0	200.0	2	150.0	200.0	3	50.0	66.7
1010_001	75.0	100.0	2	150.0	200.0	2.5	187.5	250.0	3	50.0	66.7
1010_010	75.0	100.0	2	150.0	200.0	3	225.0	300.0	3	50.0	66.7
1010_011	75.0	100.0	2	150.0	200.0	3.5	262.5	350.0	3	50.0	66.7
1010_100	75.0	100.0	2	150.0	200.0	4	300.0	400.0	3	50.0	66.7
1011_000	Reserved										
1011_001	80.0	106.7	2.5	200.0	266.6	2.5	200.0	266.6	4	50.0	66.7
1011_010	80.0	106.7	2.5	200.0	266.6	3	240.0	320.0	4	50.0	66.7

Clock Configuration Modes

Table 15. Clock Configurations for PCI Host Mode (PCI_MODCK=0)¹ (Continued)

Mode ²	Bus Clock ^{3,4} (MHz)		CPM Multiplication Factor ⁵	CPM Clock ⁴ (MHz)		CPU Multiplication Factor ⁶	CPU Clock ⁴ (MHz)		PCI Division Factor	PCI Clock (MHz)	
	low	high		low	high		low	high		low	high
1011_011	80.0	106.7	2.5	200.0	266.6	3.5	280.0	373.3	4	50.0	66.7
1011_100	80.0	106.7	2.5	200.0	266.6	4	320.0	426.6	4	50.0	66.7
1011_101	80.0	106.7	2.5	200.0	266.6	4.5	360.0	480.0	4	50.0	66.7
1101_000	100.0	133.3	2.5	250.0	333.3	3	300.0	400.0	5	50.0	66.7
1101_001	100.0	133.3	2.5	250.0	333.3	3.5	350.0	466.6	5	50.0	66.7
1101_010	100.0	133.3	2.5	250.0	333.3	4	400.0	533.3	5	50.0	66.7
1101_011	100.0	133.3	2.5	250.0	333.3	4.5	450.0	599.9	5	50.0	66.7
1101_100	100.0	133.3	2.5	250.0	333.3	5	500.0	666.6	5	50.0	66.7
1101_101	125.0	166.7	2	250.0	333.3	3	375.0	500.0	5	50.0	66.7
1101_110	125.0	166.7	2	250.0	333.3	4	500.0	666.6	5	50.0	66.7
1110_000	100.0	133.3	3	300.0	400.0	3.5	350.0	466.6	6	50.0	66.7
1110_001	100.0	133.3	3	300.0	400.0	4	400.0	533.3	6	50.0	66.7
1110_010	100.0	133.3	3	300.0	400.0	4.5	450.0	599.9	6	50.0	66.7
1110_011	100.0	133.3	3	300.0	400.0	5	500.0	666.6	6	50.0	66.7
1110_100	100.0	133.3	3	300.0	400.0	5.5	550.0	733.3	6	50.0	66.7
1100_000	50.0	66.7	2	100.0	133.3	Bypass	50.0	66.7	2	50.0	66.7
1100_001	60.0	80.0	2.5	150.0	200.0	Bypass	60.0	80.0	3	50.0	66.7
1100_010	50.0	66.7	3	150.0	200.0	Bypass	50.0	66.7	3	50.0	66.7

¹ As shown in Table 13, PCI_MODCK determines the PCI clock frequency range. Refer to Table 16 for lower range configurations.

² MODCK_H = hard reset configuration word [28–31]. Refer to Section 5.4 in the *MPC8260 User's Manual*; MODCK[1-3] = three hardware configuration pins.

³ 60x and local bus frequency. Identical to CLKIN.

⁴ 'High' and 'low' indicate frequency limits for a given configuration.

⁵ CPM multiplication factor = CPM clock/bus clock

⁶ CPU multiplication factor = Core PLL multiplication factor

Clock Configuration Modes

Table 16. Clock Configurations for PCI Host Mode (PCI_MODCK=1)¹

Mode ²	Bus Clock ^{3,4} (MHz)		CPM Multiplication Factor ⁵	CPM Clock ⁴ (MHz)		CPU Multiplication Factor ⁶	CPU Clock ⁴ (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
Default Modes (MODCK_H=0000)											
0000_000	50.0	100.0	2	100.0	200.0	2.5	125.0	250.0	4	25.0	50.0
0000_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0000_010	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0000_011	71.4	120.0	2.5	178.6	300.0	3.5	250.0	420.0	6	29.8	50.0
0000_100	62.5	120.0	2.5	156.3	300.0	4	250.0	480.0	6	26.0	50.0
0000_101	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0000_110	71.4	100.0	3	214.3	300.0	3.5	250.0	350.0	6	35.7	50.0
0000_111	62.5	100.0	3	187.5	300.0	4	250.0	400.0	6	31.3	50.0
Full Configuration Modes											
0001_000	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
0001_001	50.0	100.0	3	150.0	300.0	6	300.0	600.0	6	25.0	50.0
0001_010	50.0	100.0	3	150.0	300.0	7	350.0	700.0	6	25.0	50.0
0001_011	50.0	100.0	3	150.0	300.0	8	400.0	800.0	6	25.0	50.0
0010_000	50.0	100.0	4	200.0	400.0	5	250.0	500.0	8	25.0	50.0
0010_001	50.0	100.0	4	200.0	400.0	6	300.0	600.0	8	25.0	50.0
0010_010	50.0	100.0	4	200.0	400.0	7	350.0	700.0	8	25.0	50.0
0010_011	50.0	100.0	4	200.0	400.0	8	400.0	800.0	8	25.0	50.0
0010_100	50.0	75.0	4	200.0	300.0	5	250.0	375.0	6	33.3	50.0
0010_101	45.5	75.0	4	181.8	300.0	5.5	250.0	412.5	6	30.3	50.0
0010_110	41.7	75.0	4	166.7	300.0	6	250.0	450.0	6	27.8	50.0
0011_000	50.0	50.0	5	250.0	250.0	5	250.0	250.0	5	50.0	50.0
0011_001	41.7	50.0	5	208.3	250.0	6	250.0	300.0	5	41.7	50.0
0011_010	35.7	50.0	5	178.6	250.0	7	250.0	350.0	5	35.7	50.0
0011_011	31.3	50.0	5	156.3	250.0	8	250.0	400.0	5	31.3	50.0
0100_000	Reserved										
0100_001	41.7	50.0	6	250.0	300.0	6	250.0	300.0	6	41.7	50.0
0100_010	35.7	50.0	6	214.3	300.0	7	250.0	350.0	6	35.7	50.0
0100_011	31.3	50.0	6	187.5	300.0	8	250.0	400.0	6	31.3	50.0

Clock Configuration Modes

Table 16. Clock Configurations for PCI Host Mode (PCI_MODCK=1)¹ (Continued)

Mode ²	Bus Clock ^{3,4} (MHz)		CPM Multiplication Factor ⁵	CPM Clock ⁴ (MHz)		CPU Multiplication Factor ⁶	CPU Clock ⁴ (MHz)		PCI Division Factor	PCI Clock (MHz)	
	low	high		low	high		low	high		low	high
MODCK_H- MODCK[1-3]											
0101_000	50.0	100.0	2	100.0	200.0	2.5	125.0	250.0	4	25.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	71.4	100.0	2	142.9	200.0	3.5	250.0	350.0	4	35.7	50.0
0101_011	62.5	100.0	2	125.0	200.0	4	250.0	400.0	4	31.3	50.0
0101_100	55.6	100.0	2	111.1	200.0	4.5	250.0	450.0	4	27.8	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	71.4	120.0	2.5	178.6	300.0	3.5	250.0	420.0	6	29.8	50.0
0110_011	62.5	120.0	2.5	156.3	300.0	4	250.0	480.0	6	26.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	71.4	100.0	3	214.3	300.0	3.5	250.0	350.0	6	35.7	50.0
0111_011	62.5	100.0	3	187.5	300.0	4	250.0	400.0	6	31.3	50.0
0111_100	55.6	100.0	3	166.7	300.0	4.5	250.0	450.0	6	27.8	50.0
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0
1000_010	71.4	133.3	3	214.3	400.0	3.5	250.0	466.7	8	26.8	50.0
1000_011	66.7	133.3	3	200.0	400.0	4	266.7	533.3	8	25.0	50.0
1000_100	66.7	133.3	3	200.0	400.0	4.5	300.0	600.0	8	25.0	50.0
1000_101	66.7	133.3	3	200.0	400.0	6	400.0	800.0	8	25.0	50.0
1000_110	66.7	133.3	3	200.0	400.0	6.5	433.3	866.7	8	25.0	50.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	71.4	114.3	3.5	250.0	400.0	3.5	250.0	400.0	8	31.3	50.0
1001_011	62.5	114.3	3.5	218.8	400.0	4	250.0	457.1	8	27.3	50.0

Clock Configuration Modes

Table 16. Clock Configurations for PCI Host Mode (PCI_MODCK=1)¹ (Continued)

Mode ²	Bus Clock ^{3,4} (MHz)		CPM Multiplication Factor ⁵	CPM Clock ⁴ (MHz)		CPU Multiplication Factor ⁶	CPU Clock ⁴ (MHz)		PCI Division Factor	PCI Clock (MHz)	
	low	high		low	high		low	high		low	high
1001_100	57.1	114.3	3.5	200.0	400.0	4.5	257.1	514.3	8	25.0	50.0
1001_101	50.0	85.7	3.5	175.0	300.0	5	250.0	428.6	6	29.2	50.0
1001_110	45.5	85.7	3.5	159.1	300.0	5.5	250.0	471.4	6	26.5	50.0
1001_111	42.9	85.7	3.5	150.0	300.0	6	257.1	514.3	6	25.0	50.0
1010_000	75.0	150.0	2	150.0	300.0	2	150.0	300.0	6	25.0	50.0
1010_001	75.0	150.0	2	150.0	300.0	2.5	187.5	375.0	6	25.0	50.0
1010_010	75.0	150.0	2	150.0	300.0	3	225.0	450.0	6	25.0	50.0
1010_011	75.0	150.0	2	150.0	300.0	3.5	262.5	525.0	6	25.0	50.0
1010_100	75.0	150.0	2	150.0	300.0	4	300.0	600.0	6	25.0	50.0
1011_000	Reserved										
1011_001	80.0	160.0	2.5	200.0	400.0	2.5	200.0	400.0	8	25.0	50.0
1011_010	80.0	160.0	2.5	200.0	400.0	3	240.0	480.0	8	25.0	50.0
1011_011	80.0	160.0	2.5	200.0	400.0	3.5	280.0	560.0	8	25.0	50.0
1011_100	80.0	160.0	2.5	200.0	400.0	4	320.0	640.0	8	25.0	50.0
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	50.0	100.0	2.5	125.0	250.0	3	150.0	300.0	5	25.0	50.0
1101_001	71.4	100.0	2.5	178.6	250.0	3.5	250.0	350.0	5	35.7	50.0
1101_010	62.5	100.0	2.5	156.3	250.0	4	250.0	400.0	5	31.3	50.0
1101_011	55.6	100.0	2.5	138.9	250.0	4.5	250.0	450.0	5	27.8	50.0
1101_100	50.0	100.0	2.5	125.0	250.0	5	250.0	500.0	5	25.0	50.0
1101_101	62.5	125.0	2	125.0	250.0	3	187.5	375.0	5	25.0	50.0
1101_110	62.5	125.0	2	125.0	250.0	4	250.0	500.0	5	25.0	50.0
1110_000	71.4	100.0	3	214.3	300.0	3.5	250.0	350.0	6	35.7	50.0
1110_001	62.5	100.0	3	187.5	300.0	4	250.0	400.0	6	31.3	50.0
1110_010	55.6	100.0	3	166.7	300.0	4.5	250.0	450.0	6	27.8	50.0
1110_011	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
1110_100	50.0	100.0	3	150.0	300.0	5.5	275.0	550.0	6	25.0	50.0

Clock Configuration Modes

Table 16. Clock Configurations for PCI Host Mode (PCI_MODCK=1)¹ (Continued)

Mode ²	Bus Clock ^{3,4} (MHz)		CPM Multiplication Factor ⁵	CPM Clock ⁴ (MHz)		CPU Multiplication Factor ⁶	CPU Clock ⁴ (MHz)		PCI Division Factor	PCI Clock (MHz)	
	low	high		low	high		low	high		low	high
MODCK_H- MODCK[1-3]											
1100_000	50.0	100.0	2	100.0	200.0	Bypass	50.0	100.0	4	25.0	50.0
1100_001	60.0	120.0	2.5	150.0	300.0	Bypass	60.0	120.0	6	25.0	50.0
1100_010	50.0	100.0	3	150.0	300.0	Bypass	50.0	100.0	6	25.0	50.0

¹ As shown in Table 13, PCI_MODCK determines the PCI clock frequency range. Refer to Table 15 for higher range configurations.

² MODCK_H = hard reset configuration word [28–31]. Refer to Section 5.4 in the *MPC8260 User's Manual*; MODCK[1-3] = three hardware configuration pins.

³ 60x and local bus frequency. Identical to CLKIN.

⁴ 'High' and 'low' indicate frequency limits for a given configuration.

⁵ CPM multiplication factor = CPM clock/bus clock

⁶ CPU multiplication factor = Core PLL multiplication factor

1.3.2.2 PCI Agent Mode

Table 17 and Table 18 show configurations for PCI agent mode. Note that the range of the PCI clock frequency is determined by PCI_MODCK.

Table 17. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)¹

Mode ²	PCI Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)		Bus Division Factor	Bus Clock ^{3,6} (MHz)	
	low	high		low	high		low	high		low	high
MODCK_H- MODCK[1-3]											
Default Modes (MODCK_H=0000)											
0000_000	50.0	66.7	2	100.0	133.3	2.5	125.0	166.7	2	50.0	66.7
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7
0000_010	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0000_011	62.5	66.7	3	187.5	200.0	4	250.0	266.6	3	62.5	66.7
0000_100	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0000_101	59.5	66.7	3	178.6	200.0	3.5	250.0	280.0	2.5	71.4	80.0
0000_110	53.6	66.7	4	214.3	266.6	3.5	250.0	311.1	3	71.4	88.9
0000_111	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
Full Configuration Modes											
0001_001	Reserved										
0001_010	Reserved										
0001_011	Reserved										
0001_100	62.5	66.7	2	125.0	133.3	8	250.0	266.6	4	31.3	33.3

Clock Configuration Modes

Table 17. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)¹ (Continued)

Mode ²	PCI Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)		Bus Division Factor	Bus Clock ^{3,6} (MHz)	
	low	high		low	high		low	high		low	high
MODCK_H- MODCK[1-3]											
0010_001	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0010_010	59.5	66.7	3	178.6	200.0	3.5	250.0	280.0	2.5	71.4	80.0
0010_011	52.1	66.7	3	156.3	200.0	4	250.0	320.0	2.5	62.5	80.0
0010_100	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0
0011_000	Reserved										
0011_001	Reserved										
0011_010	Reserved										
0011_011	Reserved										
0011_100	Reserved										
0100_000	Reserved										
0100_001	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0100_010	Reserved										
0100_011	62.5	66.7	3	187.5	200.0	4	250.0	266.6	3	62.5	66.7
0100_100	55.6	66.7	3	166.7	200.0	4.5	250.0	300.0	3	55.6	66.7
0101_000	50.0	66.7	5	250.0	333.3	2.5	250.0	333.3	2.5	100.0	133.3
0101_001	50.0	66.7	5	250.0	333.3	3	300.0	400.0	2.5	100.0	133.3
0101_010	50.0	66.7	5	250.0	333.3	3.5	350.0	466.6	2.5	100.0	133.3
0101_011	50.0	66.7	5	250.0	333.3	4	400.0	533.3	2.5	100.0	133.3
0101_100	50.0	66.7	5	250.0	333.3	4.5	450.0	599.9	2.5	100.0	133.3
0101_101	50.0	66.7	5	250.0	333.3	5	500.0	666.6	2.5	100.0	133.3
0101_110	50.0	66.7	5	250.0	333.3	5.5	550.0	733.3	2.5	100.0	133.3
0110_000	Reserved										
0110_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
0110_010	53.6	66.7	4	214.3	266.6	3.5	250.0	311.1	3	71.4	88.9
0110_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
0110_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
0111_000	50.0	66.7	3	150.0	200.0	2	150.0	200.0	2	75.0	100.0

Clock Configuration Modes

Table 17. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)¹ (Continued)

Mode ²	PCI Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)		Bus Division Factor	Bus Clock ^{3,6} (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
0111_001	50.0	66.7	3	150.0	200.0	2.5	187.5	250.0	2	75.0	100.0
0111_010	50.0	66.7	3	150.0	200.0	3	225.0	300.0	2	75.0	100.0
0111_011	50.0	66.7	3	150.0	200.0	3.5	262.5	350.0	2	75.0	100.0
1000_000	Reserved										
1000_001	50.0	66.7	3	150.0	200.0	2.5	150.0	200.0	2.5	60.0	80.0
1000_010	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
1000_011	59.5	66.7	3	178.6	200.0	3.5	250.0	280.0	2.5	71.4	80.0
1000_100	52.1	66.7	3	156.3	200.0	4	250.0	320.0	2.5	62.5	80.0
1000_101	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	62.5	66.7	4	250.0	266.6	4	250.0	266.6	4	62.5	66.7
1001_100	55.6	66.7	4	222.2	266.6	4.5	250.0	300.0	4	55.6	66.7
1010_000	Reserved										
1010_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
1010_010	53.6	66.7	4	214.3	266.6	3.5	250.0	311.1	3	71.4	88.9
1010_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
1010_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
1011_000	Reserved										
1011_001	50.0	66.7	4	200.0	266.6	2.5	200.0	266.6	2.5	80.0	106.7
1011_010	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
1011_011	50.0	66.7	4	200.0	266.6	3.5	280.0	373.3	2.5	80.0	106.7
1011_100	50.0	66.7	4	200.0	266.6	4	320.0	426.6	2.5	80.0	106.7
1100_101	50.0	66.7	6	300.0	400.0	4	400.0	533.3	3	100.0	133.3
1100_110	50.0	66.7	6	300.0	400.0	4.5	450.0	599.9	3	100.0	133.3
1100_111	50.0	66.7	6	300.0	400.0	5	500.0	666.6	3	100.0	133.3
1101_000	50.0	66.7	6	300.0	400.0	5.5	550.0	733.3	3	100.0	133.3

Clock Configuration Modes

Table 17. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)¹ (Continued)

Mode ²	PCI Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)		Bus Division Factor	Bus Clock ^{3,6} (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
1101_001	50.0	66.7	6	300.0	400.0	3.5	420.0	559.9	2.5	120.0	160.0
1101_010	50.0	66.7	6	300.0	400.0	4	480.0	639.9	2.5	120.0	160.0
1101_011	50.0	66.7	6	300.0	400.0	4.5	540.0	719.9	2.5	120.0	160.0
1101_100	50.0	66.7	6	300.0	400.0	5	600.0	799.9	2.5	120.0	160.0
1110_000	50.0	66.7	5	250.0	333.3	2.5	312.5	416.6	2	125.0	166.7
1110_001	50.0	66.7	5	250.0	333.3	3	375.0	500.0	2	125.0	166.7
1110_010	50.0	66.7	5	250.0	333.3	3.5	437.5	583.3	2	125.0	166.7
1110_011	50.0	66.7	5	250.0	333.3	4	500.0	666.6	2	125.0	166.7
1110_100	50.0	66.7	5	250.0	333.3	4	333.3	444.4	3	83.3	111.1
1110_101	50.0	66.7	5	250.0	333.3	4.5	375.0	500.0	3	83.3	111.1
1110_110	50.0	66.7	5	250.0	333.3	5	416.7	555.5	3	83.3	111.1
1110_111	50.0	66.7	5	250.0	333.3	5.5	458.3	611.1	3	83.3	111.1
1100_000	50.0	66.7	2	100.0	133.3	Bypass	50.0	66.7	2	50.0	66.7
1100_001	50.0	66.7	3	150.0	200.0	Bypass	60.0	80.0	2.5	60.0	80.0
1100_010	50.0	66.7	3	150.0	200.0	Bypass	50.0	66.7	3	50.0	66.7

¹ As shown in Table 13, PCI_MODCK determines the PCI clock frequency range. Refer to Table 18 for lower range configurations.

² MODCK_H = hard reset configuration word [28–31]. Refer to Section 5.4 in the *MPC8260 User's Manual*; MODCK[1-3] = three hardware configuration pins.

³ 'High' and 'low' indicate frequency limits for a given configuration.

⁴ CPM multiplication factor = CPM clock/bus clock

⁵ CPU multiplication factor = Core PLL multiplication factor

⁶ 60x and local bus frequency. Identical to CLKIN.

Clock Configuration Modes

Table 18. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)¹

Mode ²	PCI Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)		Bus Division Factor	Bus Clock ^{3,6} (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
Default Modes (MODCK_H=0000)											
0000_000	25.0	50.0	4	100.0	200.0	2.5	125.0	250.0	2	50.0	100.0
0000_001	25.0	50.0	4	100.0	200.0	3	150.0	300.0	2	50.0	100.0
0000_010	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0000_011	31.3	50.0	6	187.5	300.0	4	250.0	400.0	3	62.5	100.0
0000_100	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0000_101	29.8	50.0	6	178.6	300.0	3.5	250.0	420.0	2.5	71.4	120.0
0000_110	26.8	50.0	8	214.3	400.0	3.5	250.0	466.7	3	71.4	133.3
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
Full Configuration Modes											
0001_001	50.0	50.0	4	200.0	200.0	5	250.0	250.0	4	50.0	50.0
0001_010	41.7	50.0	4	166.7	200.0	6	250.0	300.0	4	41.7	50.0
0001_011	35.7	50.0	4	142.9	200.0	7	250.0	350.0	4	35.7	50.0
0001_100	31.3	50.0	4	125.0	200.0	8	250.0	400.0	4	31.3	50.0
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	29.8	50.0	6	178.6	300.0	3.5	250.0	420.0	2.5	71.4	120.0
0010_011	26.0	50.0	6	156.3	300.0	4	250.0	480.0	2.5	62.5	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
0011_000	Reserved										
0011_001	31.3	50.0	4	125.0	200.0	2.5	125.0	200.0	3	41.7	66.7
0011_010	Reserved										
0011_011	46.9	50.0	4	187.5	200.0	4	250.0	266.7	3	62.5	66.7
0011_100	41.7	50.0	4	166.7	200.0	4.5	250.0	300.0	3	55.6	66.7
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0100_010	35.7	50.0	6	214.3	300.0	3.5	250.0	350.0	3	71.4	100.0
0100_011	31.3	50.0	6	187.5	300.0	4	250.0	400.0	3	62.5	100.0
0100_100	27.8	50.0	6	166.7	300.0	4.5	250.0	450.0	3	55.6	100.0

Clock Configuration Modes

Table 18. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)¹ (Continued)

Mode ²	PCI Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)		Bus Division Factor	Bus Clock ^{3,6} (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
0101_000	25.0	50.0	5	125.0	250.0	2.5	125.0	250.0	2.5	50.0	100.0
0101_001	25.0	50.0	5	125.0	250.0	3	150.0	300.0	2.5	50.0	100.0
0101_010	35.7	50.0	5	178.6	250.0	3.5	250.0	350.0	2.5	71.4	100.0
0101_011	31.3	50.0	5	156.3	250.0	4	250.0	400.0	2.5	62.5	100.0
0101_100	27.8	50.0	5	138.9	250.0	4.5	250.0	450.0	2.5	55.6	100.0
0101_101	25.0	50.0	5	125.0	250.0	5	250.0	500.0	2.5	50.0	100.0
0101_110	25.0	50.0	5	125.0	250.0	5.5	275.0	550.0	2.5	50.0	100.0
0110_000	Reserved										
0110_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
0110_010	26.8	50.0	8	214.3	400.0	3.5	250.0	466.7	3	71.4	133.3
0110_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
0110_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
0111_000	25.0	50.0	6	150.0	300.0	2	150.0	300.0	2	75.0	150.0
0111_001	25.0	50.0	6	150.0	300.0	2.5	187.5	375.0	2	75.0	150.0
0111_010	25.0	50.0	6	150.0	300.0	3	225.0	450.0	2	75.0	150.0
0111_011	25.0	50.0	6	150.0	300.0	3.5	262.5	525.0	2	75.0	150.0
1000_000	Reserved										
1000_001	25.0	50.0	6	150.0	300.0	2.5	150.0	300.0	2.5	60.0	120.0
1000_010	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
1000_011	29.8	50.0	6	178.6	300.0	3.5	250.0	420.0	2.5	71.4	120.0
1000_100	26.0	50.0	6	156.3	300.0	4	250.0	480.0	2.5	62.5	120.0
1000_101	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	31.3	50.0	8	250.0	400.0	4	250.0	400.0	4	62.5	100.0
1001_100	27.8	50.0	8	222.2	400.0	4.5	250.0	450.0	4	55.6	100.0
1010_000	Reserved										

Clock Configuration Modes

Table 18. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)¹ (Continued)

Mode ²	PCI Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)		Bus Division Factor	Bus Clock ^{3,6} (MHz)	
	low	high		low	high		low	high		low	high
1010_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
1010_010	26.8	50.0	8	214.3	400.0	3.5	250.0	466.7	3	71.4	133.3
1010_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
1010_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
1011_000	Reserved										
1011_001	25.0	50.0	8	200.0	400.0	2.5	200.0	400.0	2.5	80.0	160.0
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1100_101	31.3	50.0	6	187.5	300.0	4	250.0	400.0	3	62.5	100.0
1100_110	27.8	50.0	6	166.7	300.0	4.5	250.0	450.0	3	55.6	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	29.8	50.0	6	178.6	300.0	3.5	250.0	420.0	2.5	71.4	120.0
1101_010	26.0	50.0	6	156.3	300.0	4	250.0	480.0	2.5	62.5	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0
1110_000	25.0	50.0	5	125.0	250.0	2.5	156.3	312.5	2	62.5	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	28.6	50.0	5	142.9	250.0	3.5	250.0	437.5	2	71.4	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	37.5	50.0	5	187.5	250.0	4	250.0	333.3	3	62.5	83.3
1110_101	33.3	50.0	5	166.7	250.0	4.5	250.0	375.0	3	55.6	83.3
1110_110	30.0	50.0	5	150.0	250.0	5	250.0	416.7	3	50.0	83.3
1110_111	27.3	50.0	5	136.4	250.0	5.5	250.0	458.3	3	45.5	83.3

Table 18. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)¹ (Continued)

Mode ²	PCI Clock ³ (MHz)		CPM Multiplication Factor ⁴	CPM Clock ³ (MHz)		CPU Multiplication Factor ⁵	CPU Clock ³ (MHz)		Bus Division Factor	Bus Clock ^{3,6} (MHz)	
	low	high		low	high		low	high		low	high
MODCK_H- MODCK[1-3]											
1100_000	25.0	50.0	4	100.0	200.0	Bypass	50.0	100.0	2	50.0	100.0
1100_001	25.0	50.0	6	150.0	300.0	Bypass	60.0	120.0	2.5	60.0	120.0
1100_010	25.0	50.0	6	150.0	300.0	Bypass	50.0	100.0	3	50.0	100.0

¹ As shown in Table 13, PCI_MODCK determines the PCI clock frequency range. Refer to Table 17 for higher range configurations.

² MODCK_H = hard reset configuration word [28–31]. Refer to Section 5.4 in the *MPC8260 User's Manual*; MODCK[1-3] = three hardware configuration pins.

³ 'High' and 'low' indicate frequency limits for a given configuration.

⁴ CPM multiplication factor = CPM clock/bus clock

⁵ CPU multiplication factor = Core PLL multiplication factor

⁶ 60x and local bus frequency. Identical to CLKIN.

1.4 Pinout

This section provides the pin assignments and pinout lists for both HiP7 PowerQUICC II packages.

1.4.1 ZU Package—MPC8280 and MPC8270

The following figures and table represent the standard 480 TBGA package. For information on the alternate package for the MPC8280 and the MPC8270, refer to Section 1.4.2, “VR Package—MPC8275VR and MPC8270VR” on page 49.

1.4.1.1 ZU Pin Assignments

Figure 12 shows the pinout of the ZU package as viewed from the top surface.

Pinout

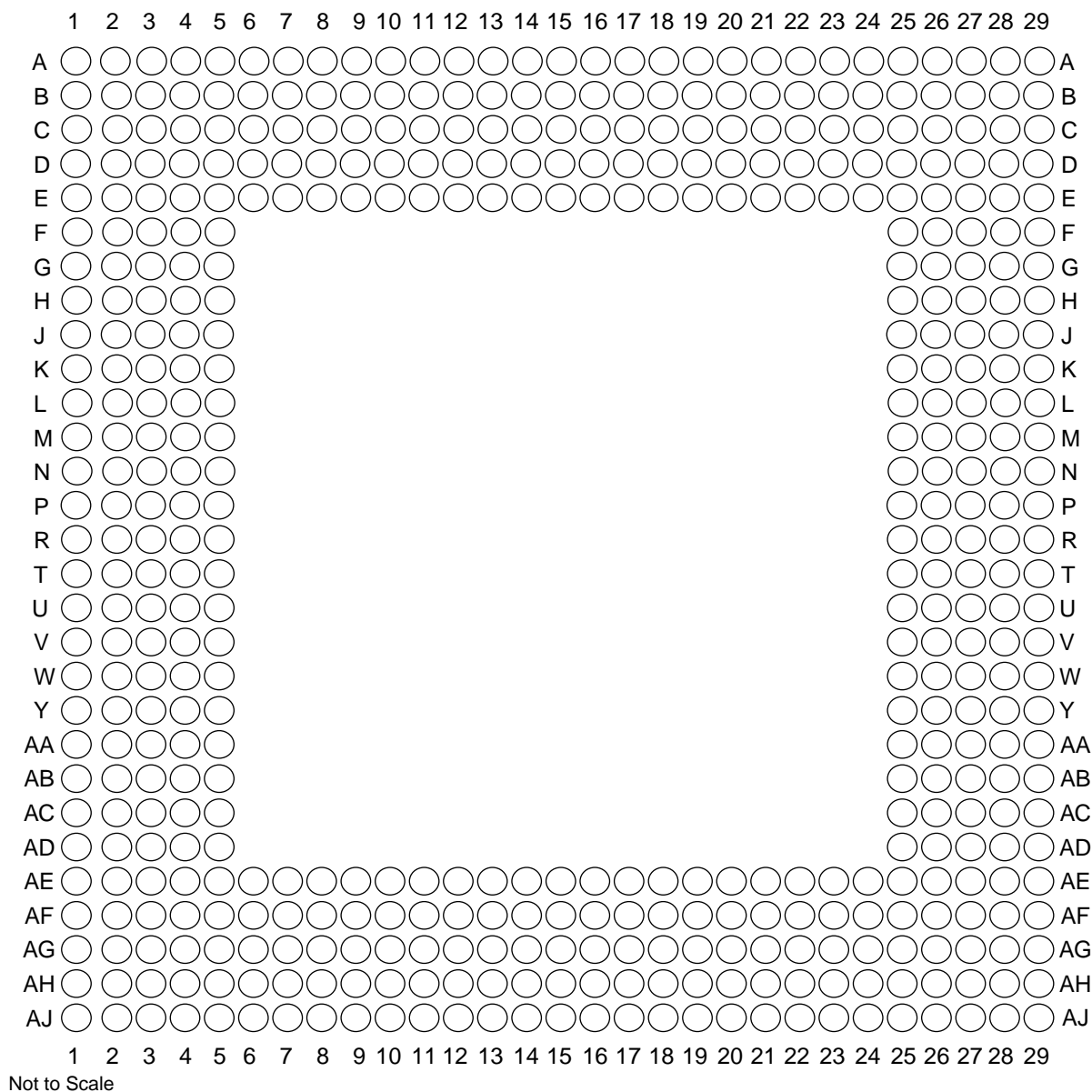


Figure 12. Pinout of the 480 TBGA Package (View from Top)

Figure 13 shows the side profile of the TBGA package to indicate the direction of the top surface view.

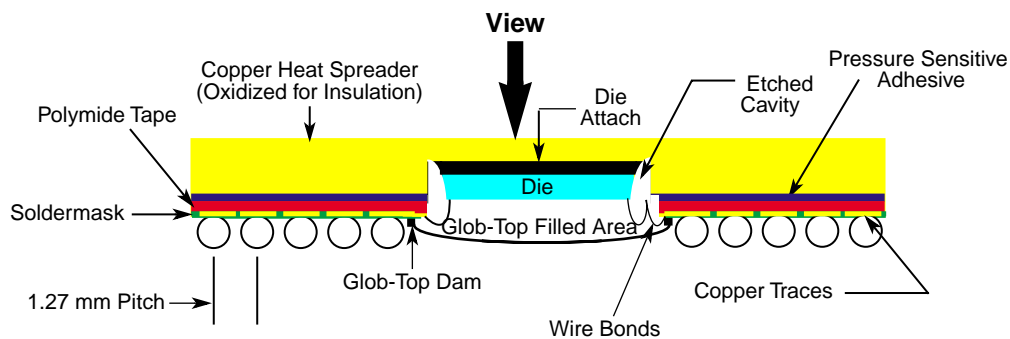


Figure 13. Side View of the TBGA Package

Table 19 shows the pinout list of the MPC8280 and MPC8270. Table 20 defines conventions and acronyms used in Table 19.

Table 19. MPC8280 and MPC8270 Pinout List

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
$\overline{\text{BR}}$		W5
$\overline{\text{BG}}$		F4
$\overline{\text{ABB/IRQ2}}$		E2
$\overline{\text{TS}}$		E3
A0		G1
A1		H5
A2		H2
A3		H1
A4		J5
A5		J4
A6		J3
A7		J2
A8		J1
A9		K4
A10		K3
A11		K2
A12		K1
A13		L5
A14		L4
A15		L3
A16		L2
A17		L1
A18		M5
A19		N5
A20		N4
A21		N3
A22		N2
A23		N1
A24		P4
A25		P3
A26		P2
A27		P1

Pinout

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
A28		R1
A29		R3
A30		R5
A31		R4
TT0		F1
TT1		G4
TT2		G3
TT3		G2
TT4		F2
TBST		D3
TSIZ0		C1
TSIZ1		E4
TSIZ2		D2
TSIZ3		F5
AACK		F3
ARTRY		E1
DBG		V1
DBB/IRQ3		V2
D0		B20
D1		A18
D2		A16
D3		A13
D4		E12
D5		D9
D6		A6
D7		B5
D8		A20
D9		E17
D10		B15
D11		B13
D12		A11
D13		E9
D14		B7
D15		B4

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
D16		D19
D17		D17
D18		D15
D19		C13
D20		B11
D21		A8
D22		A5
D23		C5
D24		C19
D25		C17
D26		C15
D27		D13
D28		C11
D29		B8
D30		A4
D31		E6
D32		E18
D33		B17
D34		A15
D35		A12
D36		D11
D37		C8
D38		E7
D39		A3
D40		D18
D41		A17
D42		A14
D43		B12
D44		A10
D45		D8
D46		B6
D47		C4
D48		C18
D49		E16

Pinout

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
D50		B14
D51		C12
D52		B10
D53		A7
D54		C6
D55		D5
D56		B18
D57		B16
D58		E14
D59		D12
D60		C10
D61		E8
D62		D6
D63		C2
DP0/RSRV/EXT_BR2		B22
IRQ1/DP1/EXT_BG2		A22
IRQ2/DP2/TLBISYNC/EXT_DBG2		E21
IRQ3/DP3/CKSTP_OUT/EXT_BR3		D21
IRQ4/DP4/CORE_SRESET/EXT_BG3		C21
IRQ5/DP5/TBEN/EXT_DBG3		B21
IRQ6/DP6/CSE0		A21
IRQ7/DP7/CSE1		E20
PSDVAL		V3
TA		C22
TEA		V5
GBL/IRQ1		W1
CI/BADDR29/IRQ2		U2
WT/BADDR30/IRQ3		U3
L2_HIT/IRQ4		Y4
CPU_BG/BADDR31/IRQ5		U4
CPU_DBG		R2
CPU_BR		Y3
CS0		F25
CS1		C29

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
CS2		E27
CS3		E28
CS4		F26
CS5		F27
CS6		F28
CS7		G25
CS8		D29
CS9		E29
CS10/BCTL1		F29
CS11/AP0		G28
BADDR27		T5
BADDR28		U1
ALE		T2
BCTL0		A27
PWE0/PSDDQM0/PBS0		C25
PWE1/PSDDQM1/PBS1		E24
PWE2/PSDDQM2/PBS2		D24
PWE3/PSDDQM3/PBS3		C24
PWE4/PSDDQM4/PBS4		B26
PWE5/PSDDQM5/PBS5		A26
PWE6/PSDDQM6/PBS6		B25
PWE7/PSDDQM7/PBS7		A25
PSDA10/PGPL0		E23
PSDWE/PGPL1		B24
POE/PSDRAS/PGPL2		A24
PSDCAS/PGPL3		B23
PGTA/PUPMWAIT/PGPL4/PPBS		A23
PSDAMUX/PGPL5		D22
LWE0/LSDDQM0/LBS0/PCI_CFG0		H28
LWE1/LSDDQM1/LBS1/PCI_CFG1		H27
LWE2/LSDDQM2/LBS2/PCI_CFG2		H26
LWE3/LSDDQM3/LBS3/PCI_CFG3		G29
LSDA10/LGPL0/PCI_MODCKH0		D27
LSDWE/LGPL1/PCI_MODCKH1		C28

Pinout

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
LOE/LSDRAS/LGPL2/PCI_MODCKH2		E26
LSDCAS/LGPL3/PCI_MODCKH3		D25
LGTA/LUPMWAIT/LGPL4/LPBS		C26
LGPL5/LSDAMUX/PCI_MODCK		B27
LWR		D28
L_A14/PAR		N27
L_A15/FRAME/SMI		T29
L_A16/TRDY		R27
L_A17/IRDY/CKSTP_OUT		R26
L_A18/STOP		R29
L_A19/DEVSEL		R28
L_A20/IDSEL		W29
L_A21/PERR		P28
L_A22/SERR		N26
L_A23/REQ0		AA27
L_A24/REQ1/HSEJSW		P29
L_A25/GNT0		AA26
L_A26/GNT1/HSLED		N25
L_A27/GNT2/HSENUM		AA25
L_A28/RST/CORE_SRESET		AB29
L_A29/INTA		AB28
L_A30/REQ2		P25
L_A31/DLLOUT		AB27
LCL_D0/AD0		H29
LCL_D1/AD1		J29
LCL_D2/AD2		J28
LCL_D3/AD3		J27
LCL_D4/AD4		J26
LCL_D5/AD5		J25
LCL_D6/AD6		K25
LCL_D7/AD7		L29
LCL_D8/AD8		L27
LCL_D9/AD9		L26
LCL_D10/AD10		L25

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
LCL_D11/AD11		M29
LCL_D12/AD12		M28
LCL_D13/AD13		M27
LCL_D14/AD14		M26
LCL_D15/AD15		N29
LCL_D16/AD16		T25
LCL_D17/AD17		U27
LCL_D18/AD18		U26
LCL_D19/AD19		U25
LCL_D20/AD20		V29
LCL_D21/AD21		V28
LCL_D22/AD22		V27
LCL_D23/AD23		V26
LCL_D24/AD24		W27
LCL_D25/AD25		W26
LCL_D26/AD26		W25
LCL_D27/AD27		Y29
LCL_D28/AD28		Y28
LCL_D29/AD29		Y25
LCL_D30/AD30		AA29
LCL_D31/AD31		AA28
LCL_DP0/C0/ $\overline{\text{BE}}0$		L28
LCL_DP1/C1/ $\overline{\text{BE}}1$		N28
LCL_DP2/C2/ $\overline{\text{BE}}2$		T28
LCL_DP3/C3/ $\overline{\text{BE}}3$		W28
$\overline{\text{IRQ}}0/\text{NMI_OUT}$		T1
$\overline{\text{IRQ}}7/\text{INT_OUT}/\text{APE}$		D1
$\overline{\text{TRST}}$		AH3
TCK		AG5
TMS		AJ3
TDI		AE6
TDO		AF5
$\overline{\text{TRIS}}$		AB4
$\overline{\text{PORESET}}$		AG6

Pinout

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
HRESET		AH5
SRESET		AF6
QREQ		AA3
RSTCONF		AJ4
MODCK1/AP1/TC0/BNKSEL0		W2
MODCK2/AP2/TC1/BNKSEL1		W3
MODCK3/AP3/TC2/BNKSEL2		W4
CLKIN1		AH4
PA0/RESTART1/DREQ3	FCC2_UTM_TXADDR2	AC29
PA1/REJECT1/DONE3	FCC2_UTM_TXADDR1	AC25
PA2/CLK20/DACK3	FCC2_UTM_TXADDR0	AE28
PA3/CLK19/DACK4/L1RXD1A2	FCC2_UTM_RXADDR0	AG29
PA4/REJECT2/DONE4	FCC2_UTM_RXADDR1	AG28
PA5/RESTART2/DREQ4	FCC2_UTM_RXADDR2	AG26
PA6	L1RSYNCA1	AE24
PA7/SMSYN2	L1TSYNCA1/L1GNTA1	AH25
PA8/SMRXD2	L1RXD0A1/L1RXDA1	AF23
PA9/SMTXD2	L1TXD0A1	AH23
PA10/MSNUM5	FCC1_UT8_RXD0/FCC1_UT16_RXD8	AE22
PA11/MSNUM4	FCC1_UT8_RXD1/FCC1_UT16_RXD9	AH22
PA12/MSNUM3	FCC1_UT8_RXD2/ FCC1_UT16_RXD10	AJ21
PA13/MSNUM2	FCC1_UT8_RXD3/ FCC1_UT16_RXD11	AH20
PA14/FCC1_RXD3	FCC1_UT8_RXD4/ FCC1_UT16_RXD12	AG19
PA15/FCC1_RXD2	/FCC1_UT8_RXD5/ FCC1_UT16_RXD13	AF18
PA16/FCC1_RXD1	FCC1_UT8_RXD6/ FCC1_UT16_RXD14	AF17
PA17/FCC1_RXD0/FCC1_RXD	FCC1_UT8_RXD7/ FCC1_UT16_RXD15	AE16
PA18/FCC1_TXD0/FCC1_TXD	FCC1_UT8_TXD7/FCC1_UT16_TXD15	AJ16
PA19/FCC1_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	AG15
PA20/FCC1_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	AJ13
PA21/FCC1_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	AE13

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11
PA24/MSNUM1	/FCC1_UT8_TXD1/FCC1_UT16_TXD9	AH9
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	AJ8
PA26/FCC1_MII_RX_ER	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	AH7
PA27/FCC1_MII_RX_DV	FCC1_UT_RXSOC	AF7
PA28/FCC1_MII_TX_EN	FCC1_UTM_RXENB/ FCC1_UTS_RXENB	AD5
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	AF1
PA30/FCC1_MII_CRD/FCC1_RTS	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	AD3
PA31/FCC1_MII_COL	FCC1_UTM_TXENB/ FCC1_UTS_TXENB	AB5
PB4/FCC3_TXD3/L1RSYNCA2/ FCC3_RTS	FCC2_UT8_RXD0	AD28
PB5/FCC3_TXD2/L1TSYNCA2/ L1GNTA2	FCC2_UT8_RXD1	AD26
PB6/FCC3_TXD1/L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AD25
PB7/FCC3_TXD0/FCC3_TXD/ L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26
PB8/FCC3_RXD0/FCC3_RXD/TXD3	FCC2_UT8_TXD3/L1RSYNCD1	AH27
PB9/FCC3_RXD1/L1TXD2A2	FCC2_UT8_TXD2/L1TSYNCD1/ L1GNTD1	AG24
PB10/FCC3_RXD2	FCC2_UT8_TXD1/L1RXDD1	AH24
PB11/FCC3_RXD3	FCC2_UT8_TXD0/L1TXDD1	AJ24
PB12/FCC3_MII_CRD/TXD2	L1CLKOB1/L1RSYNCC1	AG22
PB13/FCC3_MII_COL/L1TXD1A2	L1RQB1/L1TSYNCC1/L1GNTC1	AH21
PB14/FCC3_MII_TX_EN/RXD3	L1RXDC1	AG20
PB15/FCC3_MII_TX_ER/RXD2	L1TXDC1	AF19
PB16/FCC3_MII_RX_ER/CLK18	L1CLKOA1	AJ18
PB17/FCC3_MII_RX_DV/CLK17	L1RQA1	AJ17
PB18/FCC2_RXD3/L1CLKOD2/ L1RXD2A2	FCC2_UT8_RXD4	AE14
PB19/FCC2_RXD2/L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	AF13
PB20/FCC2_RXD1/L1RSYNCD2/ L1TXD1A1	FCC2_UT8_RXD6	AG12

Pinout

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
PB21/FCC2_RXD0/FCC2_RXD/ L1TSYNCD2/L1GNTD2	FCC2_UT8_RXD7/L1TXD2A1	AH11
PB22/FCC2_TXD0/FCC2_TXD/ L1RXDD2	FCC2_UT8_TXD7/L1RXD1A1	AH16
PB23/FCC2_TXD1/L1TXDD2	FCC2_UT8_TXD6/L1RXD2A1	AE15
PB24/FCC2_TXD2/L1RSYNCC2	FCC2_UT8_TXD5/L1RXD3A1	AJ9
PB25/FCC2_TXD3/L1TSYNCC2/ L1GNTC2	FCC2_UT8_TXD4/L1TXD3A1	AE9
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	AJ7
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	AH6
PB28/FCC2_MII_RX_ER/FCC2_RTS/ L1TSYNCB2/L1GNTB2/TXD1		AE3
PB29/L1RSYNCB2/ FCC2_MII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	AE2
PB30/FCC2_MII_RX_DV/L1RXDB2	FCC2_UT_TXSOC	AC5
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	AC4
PC0/DREQ1/BRGO7/SMSYN2/ L1CLKOA2		AB26
PC1/DREQ2/BRGO6/L1RQA2		AD29
PC2/FCC3_CD/DONE2	FCC2_UT8_TXD3	AE29
PC3/FCC3_CTS/DACK2/CTS4	FCC2_UT8_TXD2	AE27
PC4/SI2_L1ST4/FCC2_CD	FCC2_UTM_RXENB/ FCC2_UTS_RXENB	AF27
PC5/SI2_L1ST3/FCC2_CTS	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AF24
PC6/FCC1_CD	L1CLKOC1/FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AJ26
PC7/FCC1_CTS	L1RQC1/FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AJ25
PC8/CD4/RENA4/SI2_L1ST2/CTS3	FCC1_UT16_TXD0	AF22
PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2	FCC1_UT16_TXD1	AE21
PC10/CD3/RENA3	FCC1_UT16_TXD2/SI1_L1ST4/ FCC2_UT8_RXD3	AF20
PC11/CTS3/CLSN3/L1TXD3A2	L1CLKOD1/FCC2_UT8_RXD2	AE19
PC12/CD2/RENA2	SI1_L1ST3/FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	AE18

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
PC13/CTS2/CLSN2	L1RQD1/FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	AH18
PC14/CD1/RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	AH17
PC15/CTS1/CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	AG16
PC16/CLK16/TIN4		AF15
PC17/CLK15/TIN3/BRGO8		AJ15
PC18/CLK14/TGATE2		AH14
PC19/CLK13/BRGO7		AG13
PC20/CLK12/TGATE1		AH12
PC21/CLK11/BRGO6		AJ11
PC22/CLK10/DONE1		AG10
PC23/CLK9/BRGO5/DACK1		AE10
PC24/CLK8/TOUT4	FCC2_UT8_TXD3	AF9
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	AE8
PC26/CLK6/TOUT3/TMCLK		AJ6
PC27/FCC3_TXD/FCC3_TXD0/CLK5/ BRGO3		AG2
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2		AF3
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		AF2
PC30/CLK2/TOUT1	FCC2_UT8_TXD3	AE1
PC31/CLK1/BRGO1		AD1
PD4/BRGO8/FCC3_RTS/SMRXD2	L1TSYNCD1/L1GNTD1	AC28
PD5/DONE1	FCC1_UT16_TXD3	AD27
PD6/DACK1	FCC1_UT16_TXD4	AF29
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3	AF28
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AG25
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	AH26
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1/L1RSYNCB1	AJ27
PD11/L1RQB2	FCC2_UT8_RXD0/L1TSYNCB1/ L1GNTB1	AJ23
PD12	SI1_L1ST2/L1RXDB1	AG23
PD13	SI1_L1ST1/L1TXDB1	AJ22
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	AE20

Pinout

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	AJ20
PD16/SPIMISO	FCC1_UT_TXPRTY/L1TSYNCC1/ L1GNTC1	AG18
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	AG17
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3	AF16
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3	AH15
PD20/RTS4/TENA4/L1RSYNCA2	FCC1_UT16_RXD2	AJ14
PD21/TXD4/L1RXD0A2/L1RXDA2	FCC1_UT16_RXD3	AH13
PD22/RXD4/L1TXD0A2/L1TXDA2	FCC1_UT16_TXD5	AJ12
PD23/RTS3/TENA3	FCC1_UT16_RXD4/L1RSYNCD1	AE12
PD24/TXD3	FCC1_UT16_RXD5/L1RXDD1	AF10
PD25/RXD3	FCC1_UT16_TXD6/L1TXDD1	AG9
PD26/RTS2/TENA2	FCC1_UT16_RXD6/L1RSYNCC1	AH8
PD27/TXD2	FCC1_UT16_RXD7/L1RXDC1	AG7
PD28/RXD2	FCC1_UT16_TXD7/L1TXDC1	AE4
PD29/RTS1/TENA1	FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2	AG1
PD30/TXD1	FCC2_UTM_TXENB/ FCC2_UTS_TXENB	AD4
PD31/RXD1		AD2
VCCSYN		AB3
VCCSYN1		B9
CLKIN2		AE11
SPARE4 ¹		U5
PCI_MODE ²		AF25
SPARE6 ¹		V4
THERMAL0 ³		AA1
THERMAL1 ³		AG4

Table 19. MPC8280 and MPC8270 Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only (UTOPIA Pins)	
I/O power		AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power		U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground		AA5, AB1 ⁴ , AB2 ⁵ , AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

¹ Must be pulled down or left floating.

² If PCI is not desired, must be pulled up or left floating.

³ For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* (AN2271/D).

⁴ GNDSYN (AB1): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the MPC8280. New designs must connect AB1 to GND and follow the suggestions in Section 1.2.2.1, "Layout Practices." Old designs in which the MPC8280 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.

⁵ XFC (AB2) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8280 because there is no need for external capacitor to operate the PLL. New designs should connect AB2 (XFC) pin to GND. Old designs in which the MPC8280 is used as a drop-in replacement can leave the pin connected to the current capacitor.

Symbols used in Table 19 are described in Table 20.

Table 20. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as \overline{TA} , are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

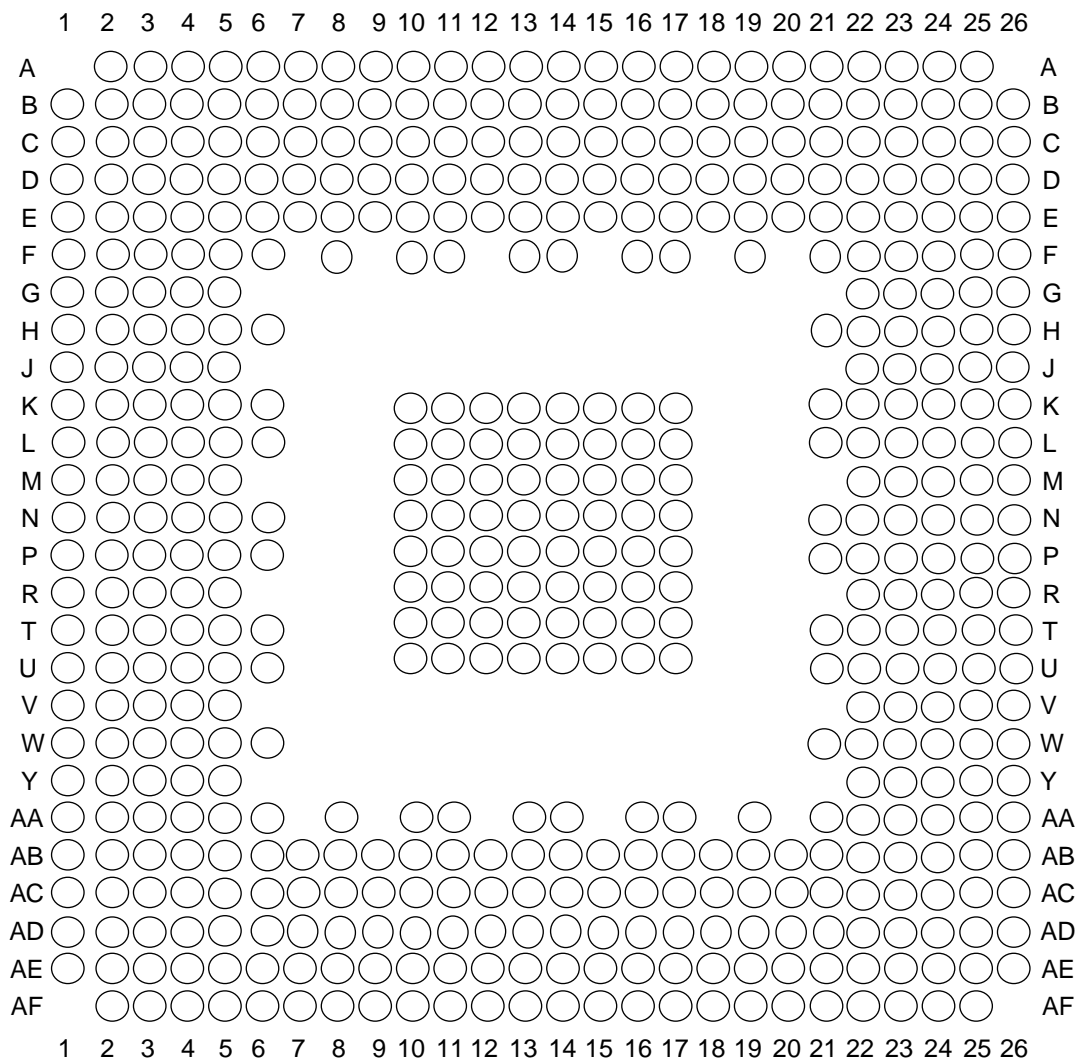
1.4.2 VR Package—MPC8275VR and MPC8270VR

The following figures and table represent the alternate 516 PBGA package. For information on the standard package for the MPC8280 and the MPC8270, refer to Section 1.4.1, "ZU Package—MPC8280 and MPC8270" on page 35.

Pinout

1.4.2.1 VR Pin Assignments

Figure 14 shows the pinout of the VR package as viewed from the top surface.



Not to Scale

Figure 14. Pinout of the 516 PBGA Package (View from Top)

Figure 15 shows the side profile of the PBGA package to indicate the direction of the top surface view.

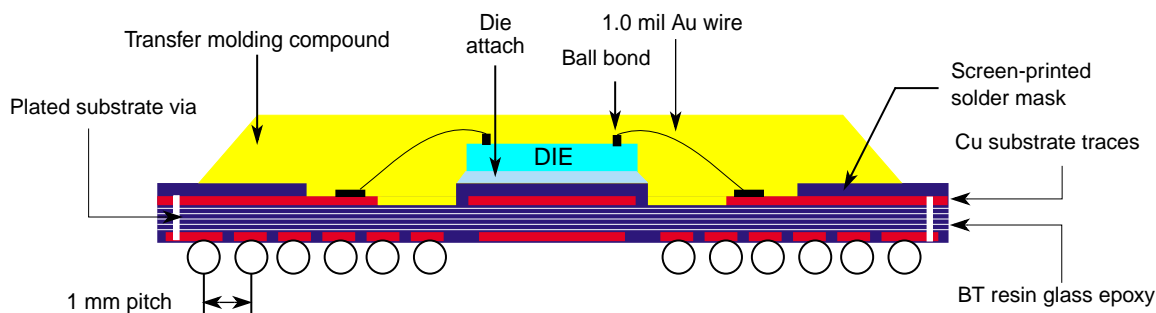


Figure 15. Side View of the PBGA Package

Table 21 shows the pinout list of the MPC8275VR and MPC8270VR. Table 20 defines conventions and acronyms used in Table 21.

Table 21. MPC8275VR and MPC8270VR Pinout List

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
$\overline{\text{BR}}$		C16
$\overline{\text{BG}}$		D2
$\overline{\text{ABB/IRQ2}}$		C1
$\overline{\text{TS}}$		D1
A0		D5
A1		E8
A2		C4
A3		B4
A4		A4
A5		D7
A6		D8
A7		C6
A8		B5
A9		B6
A10		C7
A11		C8
A12		A6
A13		D9
A14		F11
A15		B7
A16		B8
A17		C9
A18		A7
A19		B9
A20		E11
A21		A8
A22		D11
A23		B10
A24		C11
A25		A9
A26		B11
A27		C12

Pinout

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
A28		D12
A29		A10
A30		B12
A31		B13
TT0		E7
TT1		B3
TT2		F8
TT3		A3
TT4		C3
TBST		F5
TSIZ0		E3
TSIZ1		E2
TSIZ2		E1
TSIZ3		E4
AACK		D3
ARTRY		C2
DBG		A14
DBB/IRQ3		C15
D0		W4
D1		Y1
D2		V1
D3		P4
D4		N3
D5		K5
D6		J4
D7		G1
D8		AB1
D9		U4
D10		U2
D11		N6
D12		N1
D13		L1
D14		J5
D15		G3

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
D16		AA2
D17		W1
D18		T3
D19		T1
D20		M2
D21		K2
D22		J1
D23		G4
D24		U5
D25		T5
D26		P5
D27		P3
D28		M3
D29		K3
D30		H2
D31		G5
D32		AA1
D33		V2
D34		U1
D35		P2
D36		M4
D37		K4
D38		H3
D39		F2
D40		Y2
D41		U3
D42		T2
D43		N2
D44		M5
D45		K1
D46		H4
D47		F1
D48		W2
D49		T4

Pinout

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
D50		R3
D51		N4
D52		M1
D53		J2
D54		H5
D55		F3
D56		V3
D57		R5
D58		R2
D59		N5
D60		L2
D61		J3
D62		H1
D63		F4
DP0/RSRV/EXT_BR2		AB3
IRQ1/DP1/EXT_BG2		W5
IRQ2/DP2/TLBISYNC/EXT_DBG2		AC2
IRQ3/DP3/CKSTP_OUT/EXT_BR3		AA3
IRQ4/DP4/CORE_SRESET/EXT_BG3		AD1
IRQ5/DP5/TBEN/EXT_DBG3		AC1
IRQ6/DP6/CSE0		AB2
IRQ7/DP7/CSE1		Y3
PSDVAL		D15
TA		Y4
TEA		D16
GBL/IRQ1		E15
CI/BADDR29/IRQ2		D14
WT/BADDR30/IRQ3		E14
L2_HIT/IRQ4		A17
CPU_BG/BADDR31/IRQ5		B14
CPU_DBG		F13
CPU_BR		B17
CS0		AC6
CS1		AD6

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
CS2		AE6
CS3		AB7
CS4		AF7
CS5		AC7
CS6		AD7
CS7		AF8
CS8		AE8
CS9		AD8
CS10/BCTL1		AC8
CS11/AP0		AB8
BADDR27		C13
BADDR28		A12
ALE		D13
BCTL0		AF4
PWE0/PSDDQM0/PBS0		AA5
PWE1/PSDDQM1/PBS1		AE4
PWE2/PSDDQM2/PBS2		AD4
PWE3/PSDDQM3/PBS3		AF3
PWE4/PSDDQM4/PBS4		AB4
PWE5/PSDDQM5/PBS5		AE3
PWE6/PSDDQM6/PBS6		AF2
PWE7/PSDDQM7/PBS7		AD3
PSDA10/PGPL0		AE2
PSDWE/PGPL1		AD2
POE/PSDRAS/PGPL2		AE1
PSDCAS/PGPL3		AC3
PGTA/PUPMWAIT/PGPL4/PPBS		W6
PSDAMUX/PGPL5		AA4
LWE0/LSDDQM0/LBS0/PCI_CFG0		AC9
LWE1/LSDDQM1/LBS1/PCI_CFG1		AD9
LWE2/LSDDQM2/LBS2/PCI_CFG2		AE9
LWE3/LSDDQM3/LBS3/PCI_CFG3		AF9
LSDA10/LGPL0/PCI_MODCKH0		AB6
LSDWE/LGPL1/PCI_MODCKH1		AF5

Pinout

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
LOE/LSDRAS/LGPL2/PCI_MODCKH2		AE5
LSDCAS/LGPL3/PCI_MODCKH3		AD5
LGTA/LUPMWAIT/LGPL4/LPBS		AC5
LGPL5/LSDAMUX/PCI_MODCK		AB5
LWR		AF6
L_A14/PAR		AE13
L_A15/FRAME/SMI		AD15
L_A16/TRDY		AF16
L_A17/IRDY/CKSTP_OUT		AF15
L_A18/STOP		AE15
L_A19/DEVSEL		AE14
L_A20/IDSEL		AC17
L_A21/PERR		AD14
L_A22/SERR		AF13
L_A23/REQ0		AE20
L_A24/REQ1/HSEJSW		AC14
L_A25/GNT0		AC19
L_A26/GNT1/HSLED		AD13
L_A27/GNT2/HSENUM		AF21
L_A28/RST/CORE_SRESET		AF22
L_A29/INTA		AE21
L_A30/REQ2		AB14
L_A31/DLLOUT		AD20
LCL_D0/AD0		AB9
LCL_D1/AD1		AB10
LCL_D2/AD2		AC10
LCL_D3/AD3		AD10
LCL_D4/AD4		AE10
LCL_D5/AD5		AF10
LCL_D6/AD6		AF11
LCL_D7/AD7		AB12
LCL_D8/AD8		AB11
LCL_D9/AD9		AF12
LCL_D10/AD10		AE11

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
LCL_D11/AD11		AC13
LCL_D12/AD12		AC12
LCL_D13/AD13		AB13
LCL_D14/AD14		AD12
LCL_D15/AD15		AF14
LCL_D16/AD16		AF17
LCL_D17/AD17		AE16
LCL_D18/AD18		AD16
LCL_D19/AD19		AC16
LCL_D20/AD20		AB16
LCL_D21/AD21		AF18
LCL_D22/AD22		AE17
LCL_D23/AD23		AD17
LCL_D24/AD24		AB17
LCL_D25/AD25		AE18
LCL_D26/AD26		AD18
LCL_D27/AD27		AC18
LCL_D28/AD28		AE19
LCL_D29/AD29		AF20
LCL_D30/AD30		AD19
LCL_D31/AD31		AB18
LCL_DP0/C0/ $\overline{\text{BE}}_0$		AE12
LCL_DP1/C1/ $\overline{\text{BE}}_1$		AA13
LCL_DP2/C2/ $\overline{\text{BE}}_2$		AC15
LCL_DP3/C3/ $\overline{\text{BE}}_3$		AF19
IRQ0/NMI_OUT		A11
IRQ7/INT_OUT/APE		E5
TRST		F22
TCK		A24
TMS		C24
TDI		A25
TDO		B24
TRIS		C19
PORESET		B25

Pinout

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
HRESET		D24
SRESET		E23
QREQ		D18
RSTCONF		E24
MODCK1/AP1/TC0/BNKSEL0		B16
MODCK2/AP2/TC1/BNKSEL1		F16
MODCK3/AP3/TC2/BNKSEL2		A15
CLKIN1		G22
PA0/RESTART1/DREQ3	FCC2_UTM_TXADDR2	AC20
PA1/REJECT1/DONE3	FCC2_UTM_TXADDR1	AC21
PA2/CLK20/DACK3	FCC2_UTM_TXADDR0	AF25
PA3/CLK19/DACK4/L1RXD1A2	FCC2_UTM_RXADDR0	AE24
PA4/REJECT2/DONE4	FCC2_UTM_RXADDR1	AA21
PA5/RESTART2/DREQ4	FCC2_UTM_RXADDR2	AD25
PA6	L1RSYNCA1	AC24
PA7/SMSYN2	L1TSYNCA1/L1GNTA1	AA22
PA8/SMRXD2	L1RXD0A1/L1RXDA1	AA23
PA9/SMTXD2	L1TXD0A1	Y26
PA10/MSNUM5	FCC1_UT8_RXD0/FCC1_UT16_RXD8	W22
PA11/MSNUM4	FCC1_UT8_RXD1/FCC1_UT16_RXD9	W23
PA12/MSNUM3	FCC1_UT8_RXD2/ FCC1_UT16_RXD10	V26
PA13/MSNUM2	FCC1_UT8_RXD3/ FCC1_UT16_RXD11	V25
PA14/FCC1_RXD3	FCC1_UT8_RXD4/ FCC1_UT16_RXD12	T22
PA15/FCC1_RXD2	/FCC1_UT8_RXD5/ FCC1_UT16_RXD13	T25
PA16/FCC1_RXD1	FCC1_UT8_RXD6/ FCC1_UT16_RXD14	R24
PA17/FCC1_RXD0/FCC1_RXD	FCC1_UT8_RXD7/ FCC1_UT16_RXD15	P22
PA18/FCC1_TXD0/FCC1_TXD	FCC1_UT8_TXD7/FCC1_UT16_TXD15	N26
PA19/FCC1_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	N23
PA20/FCC1_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	K26
PA21/FCC1_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	L23

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	K23
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	H26
PA24/MSNUM1	/FCC1_UT8_TXD1/FCC1_UT16_TXD9	F25
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	D26
PA26/FCC1_MII_RX_ER	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	D25
PA27/FCC1_MII_RX_DV	FCC1_UT_RXSOC	C25
PA28/FCC1_MII_TX_EN	FCC1_UTM_RXENB/ FCC1_UTS_RXENB	C22
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	B21
PA30/FCC1_MII_CRD/FCC1_RTS	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	A20
PA31/FCC1_MII_COL	FCC1_UTM_TXENB/ FCC1_UTS_TXENB	A19
PB4/FCC3_TXD3/L1RSYNCA2/ FCC3_RTS	FCC2_UT8_RXD0	AD21
PB5/FCC3_TXD2/L1TSYNCA2/ L1GNTA2	FCC2_UT8_RXD1	AD22
PB6/FCC3_TXD1/L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AC22
PB7/FCC3_TXD0/FCC3_TXD/ L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26
PB8/FCC3_RXD0/FCC3_RXD/TXD3	FCC2_UT8_TXD3/L1RSYNCD1	AB23
PB9/FCC3_RXD1/L1TXD2A2	FCC2_UT8_TXD2/L1TSYNCD1/ L1GNTD1	AC26
PB10/FCC3_RXD2	FCC2_UT8_TXD1/L1RXDD1	AB26
PB11/FCC3_RXD3	FCC2_UT8_TXD0/L1TXDD1	AA25
PB12/FCC3_MII_CRD/TXD2	L1CLKOB1/L1RSYNCC1	W26
PB13/FCC3_MII_COL/L1TXD1A2	L1RQB1/L1TSYNCC1/L1GNTC1	W25
PB14/FCC3_MII_TX_EN/RXD3	L1RXDC1	V24
PB15/FCC3_MII_TX_ER/RXD2	L1TXDC1	U24
PB16/FCC3_MII_RX_ER/CLK18	L1CLKOA1	R22
PB17/FCC3_MII_RX_DV/CLK17	L1RQA1	R23
PB18/FCC2_RXD3/L1CLKOD2/ L1RXD2A2	FCC2_UT8_RXD4	M23
PB19/FCC2_RXD2/L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	L24
PB20/FCC2_RXD1/L1RSYNCD2/ L1TXD1A1	FCC2_UT8_RXD6	K24

Pinout

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
PB21/FCC2_RXD0/FCC2_RXD/ L1TSYNCD2/L1GNTD2	FCC2_UT8_RXD7/L1TXD2A1	L21
PB22/FCC2_TXD0/FCC2_TXD/ L1RXDD2	FCC2_UT8_TXD7/L1RXD1A1	P25
PB23/FCC2_TXD1/L1TXDD2	FCC2_UT8_TXD6/L1RXD2A1	N25
PB24/FCC2_TXD2/L1RSYNCC2	FCC2_UT8_TXD5/L1RXD3A1	E26
PB25/FCC2_TXD3/L1TSYNCC2/ L1GNTC2	FCC2_UT8_TXD4/L1TXD3A1	H23
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	C26
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	B26
PB28/FCC2_MII_RX_ER/FCC2_RTS/ L1TSYNCB2/L1GNTB2/TXD1		A22
PB29/L1RSYNCB2/ FCC2_MII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	A21
PB30/FCC2_MII_RX_DV/L1RXDB2	FCC2_UT_TXSOC	E20
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	C20
PC0/DREQ1/BRGO7/SMSYN2/ L1CLKOA2		AE22
PC1/DREQ2/BRGO6/L1RQA2		AA19
PC2/FCC3_CD/DONE2	FCC2_UT8_TXD3	AF24
PC3/FCC3_CTS/DACK2/CTS4	FCC2_UT8_TXD2	AE25
PC4/SI2_L1ST4/FCC2_CD	FCC2_UTM_RXENB/ FCC2_UTS_RXENB	AB22
PC5/SI2_L1ST3/FCC2_CTS	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AC25
PC6/FCC1_CD	L1CLKOC1/FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AB25
PC7/FCC1_CTS	L1RQC1/FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AA24
PC8/CD4/RENA4/SI2_L1ST2/CTS3	FCC1_UT16_TXD0	Y24
PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GN2A2	FCC1_UT16_TXD1	U22
PC10/CD3/RENA3	FCC1_UT16_TXD2/SI1_L1ST4/ FCC2_UT8_RXD3	V23
PC11/CTS3/CLSN3/L1TXD3A2	L1CLKOD1/FCC2_UT8_RXD2	U23
PC12/CD2/RENA2	SI1_L1ST3/FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	T26

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
PC13/ $\overline{\text{CTS2}}$ /CLSN2	L1RQD1/FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	R26
PC14/ $\overline{\text{CD1}}$ /RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	P26
PC15/ $\overline{\text{CTS1}}$ /CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	P24
PC16/CLK16/TIN4		M26
PC17/CLK15/TIN3/BRGO8		L26
PC18/CLK14/ $\overline{\text{TGATE2}}$		M24
PC19/CLK13/BRGO7		L22
PC20/CLK12/ $\overline{\text{TGATE1}}$		K25
PC21/CLK11/BRGO6		J25
PC22/CLK10/ $\overline{\text{DONE1}}$		G26
PC23/CLK9/BRGO5/ $\overline{\text{DACK1}}$		F26
PC24/CLK8/ $\overline{\text{TOUT4}}$	FCC2_UT8_TXD3	G24
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	E25
PC26/CLK6/ $\overline{\text{TOUT3}}$ /TMCLK		G23
PC27/FCC3_TXD/FCC3_TXD0/CLK5/ BRGO3		B23
PC28/CLK4/TIN1/ $\overline{\text{TOUT2}}$ /CTS2/CLSN2		E22
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		E21
PC30/CLK2/ $\overline{\text{TOUT1}}$	FCC2_UT8_TXD3	D21
PC31/CLK1/BRGO1		B20
PD4/BRGO8/ $\overline{\text{FCC3_RTS}}$ /SMRXD2	L1TSYNCD1/L1GNTD1	AF23
PD5/ $\overline{\text{DONE1}}$	FCC1_UT16_TXD3	AE23
PD6/ $\overline{\text{DACK1}}$	FCC1_UT16_TXD4	AB21
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3	AD23
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AD26
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	Y22
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1/L1RSYNCB1	AB24
PD11/ $\overline{\text{L1RQB2}}$	FCC2_UT8_RXD0/L1TSYNCB1/ L1GNTB1	Y23
PD12	SI1_L1ST2/L1RXDB1	AA26
PD13	SI1_L1ST1/L1TXDB1	W24
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	V22

Pinout

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	U26
PD16/SPIMISO	FCC1_UT_TXPRTY/L1TSYNCC1/ L1GNTC1	T23
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	R25
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3	P23
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3	N22
PD20/RTS4/TENA4/L1RSYNCA2	FCC1_UT16_RXD2	M25
PD21/TXD4/L1RXD0A2/L1RXDA2	FCC1_UT16_RXD3	L25
PD22/RXD4/L1TXD0A2/L1TXDA2	FCC1_UT16_TXD5	J26
PD23/RTS3/TENA3	FCC1_UT16_RXD4/L1RSYNCD1	K22
PD24/TXD3	FCC1_UT16_RXD5/L1RXDD1	G25
PD25/RXD3	FCC1_UT16_TXD6/L1TXDD1	H24
PD26/RTS2/TENA2	FCC1_UT16_RXD6/L1RSYNCC1	F24
PD27/TXD2	FCC1_UT16_RXD7/L1RXDC1	H22
PD28/RXD2	FCC1_UT16_TXD7/L1TXDC1	B22
PD29/RTS1/TENA1	FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2	D22
PD30/TXD1	FCC2_UTM_TXENB/ FCC2_UTS_TXENB	C21
PD31/RXD1		E19
VCCSYN		D19
VCCSYN1		K6
CLKIN2		K21
SPARE4 ¹		C14
PCI_MODE ²		AD24
SPARE6 ¹		B15
THERMAL0 ³		E17
THERMAL1 ³		C23
I/O power		E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9

Table 21. MPC8275VR and MPC8270VR Pinout List (Continued)

Pin Name		Ball
MPC8275VR/MPC8270VR	MPC8275VR only (UTOPIA Pins)	
Core Power		L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10
Ground		B18 ⁴ , A18 ⁵ , A2, B1, B2, A5, C5, C18, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17

¹ Must be pulled down or left floating.

² If PCI is not desired, must be pulled up or left floating.

³ For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* (AN2271/D).

⁴ GNDSYN (B18): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the MPC8275VR/MPC8270VR. New designs must connect B18 to GND and follow the suggestions in Section 1.2.2.1, "Layout Practices." Old designs in which the MPC8275VR/MPC8270VR is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.

⁵ XFC (A18) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8275VR/MPC8270VR because there is no need for external capacitor to operate the PLL. New designs should connect A18 (XFC) pin to GND. Old designs in which the MPC8275VR/MPC8270VR is used as a drop-in replacement can leave the pin connected to the current capacitor.

1.5 Package Description

The following sections provide the package parameters and mechanical dimensions.

1.5.1 Package Parameters

Package parameters are provided in Table 22.

Table 22. Package Parameters

Package	Devices	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
ZU	MPC8280 MPC8270	37.5 x 37.5	TBGA	480	1.27	1.55
VR	MPC8275VR MPC8270VR)	27 x 27	PBGA	516	1	2.25

Package Description

1.5.2 Mechanical Dimensions

1.5.2.1 ZU Package Dimensions

Figure 16 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.

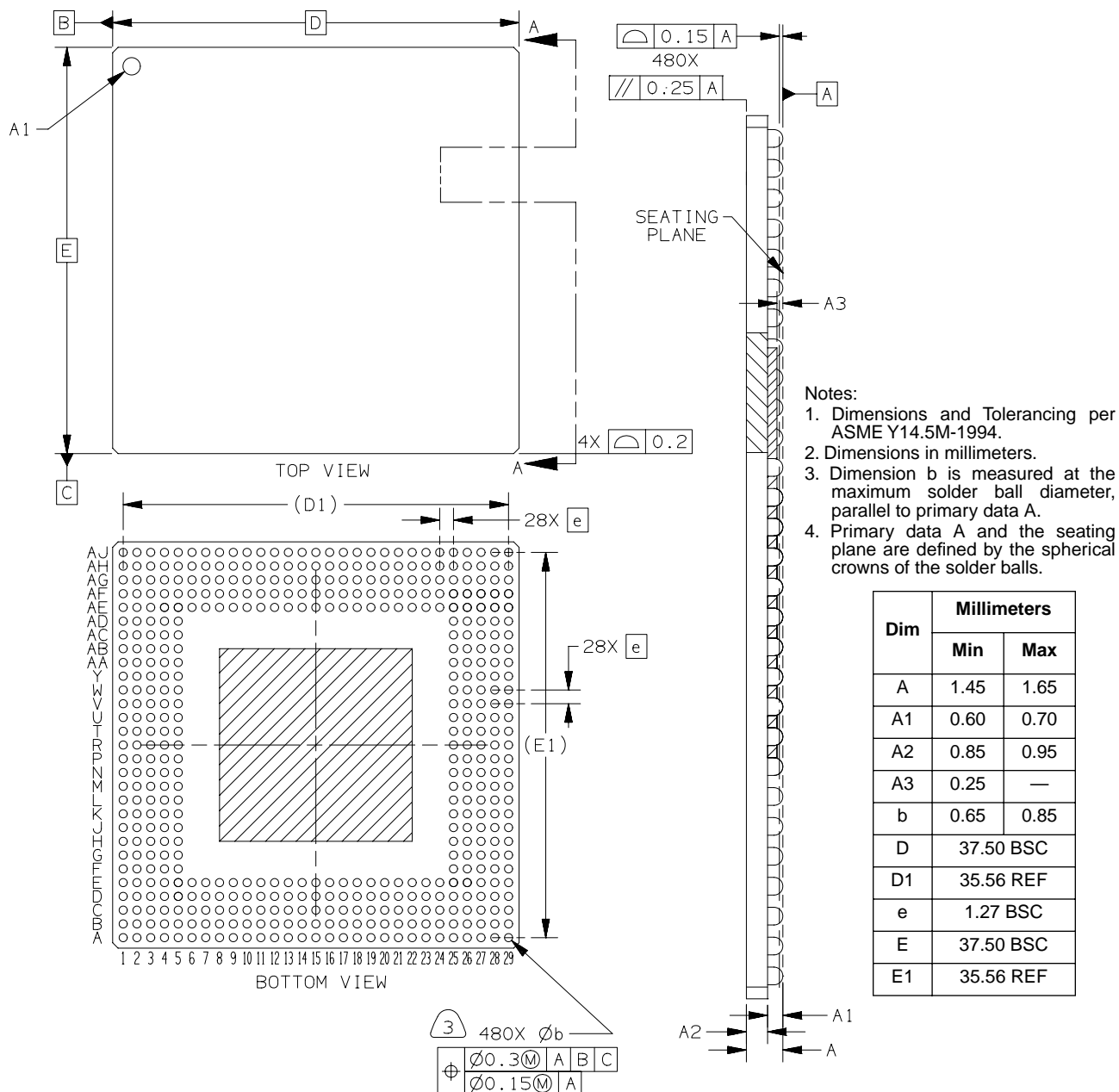


Figure 16. Mechanical Dimensions and Bottom Surface Nomenclature—480 TBGA

1.5.2.2 VR Package Dimensions

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

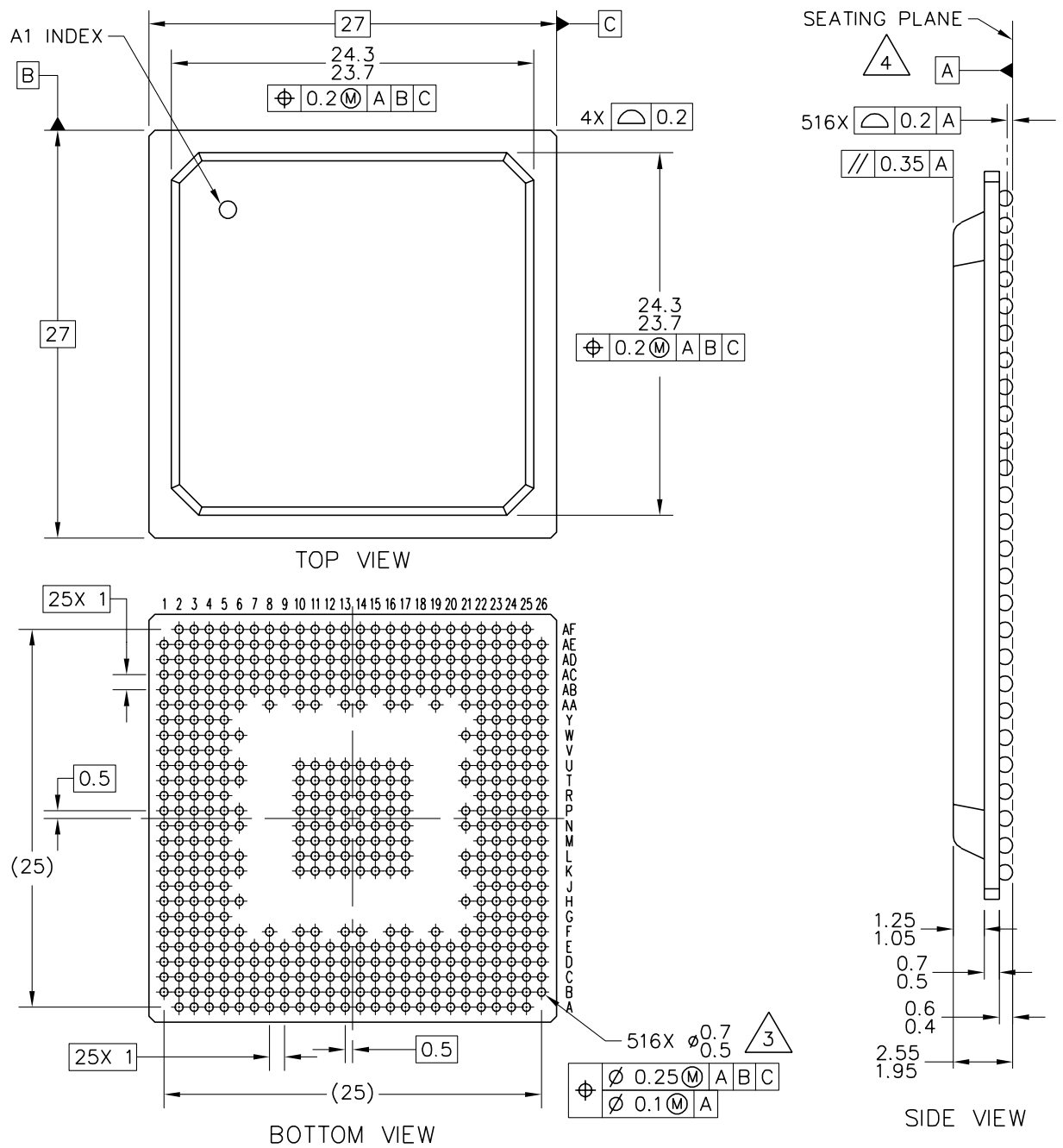


Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA

Ordering Information

1.6 Ordering Information

Figure 18 provides an example of the Motorola part numbering nomenclature for the MPC8280. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Motorola sales office.

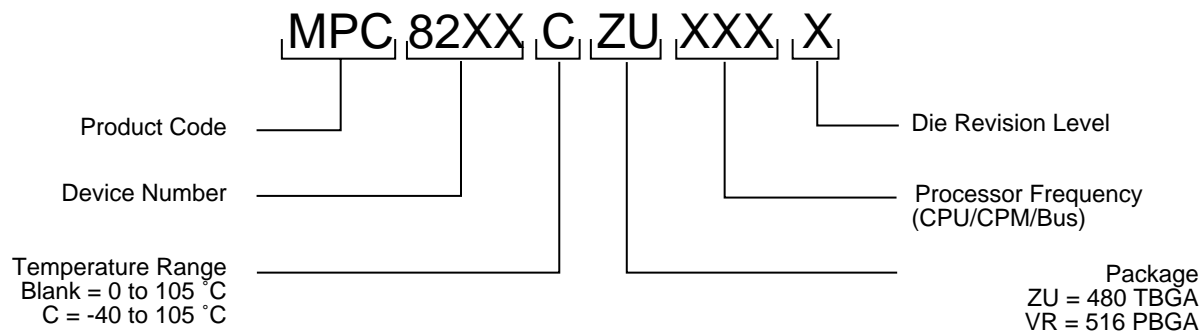


Figure 18. Motorola Part Number Key

Table 23. Document Revision History

Document Revision	Substantive Changes
0	—
0.1	Initial public release
0.2	Table 21, "VR Pinout": Addition of C18 to the Ground (GND) pin list (page 63)

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