

DATA SHEET



TDA8020HL Dual smart card interface

Product specification
Supersedes data of 2001 May 29
File under Integrated Circuits, IC02

2001 Aug 15

Dual smart card interface

TDA8020HL

FEATURES

- Two independent 6 contacts smart card interfaces
- Supply voltage to the cards; $V_{CC} = 5$ or $3\text{ V} \pm 5\%$; I_{CC} up to 65 mA
- Integrated DC/DC converter (doubler, tripler or follower) for allowing power supply from 2.5 to 6.5 V
- Independent supply voltage for interface signals (from 1.5 to 6.5 V)
- Control and status via the I²C-bus
- Four possible devices in parallel due to two I²C-bus address pins
- Electrical specifications according to ISO 7816 or EMV norms
- Automatic activation and deactivation sequences by means of integrated sequencers
- Automatic clock count and reset toggling during warm or cold reset
- Interrupt request output to the controller
- 6 kV ESD protection on cards contacts
- Automatic emergency deactivation in the event of supply drop-out, overload, overheating or card take-off
- Current limitation on pins CLK, RST, I/O and V_{CC}
- Integrated voltage supervisor for power-on reset and drop-out detection
- Power-down mode with several wake-up events.



APPLICATIONS

- Set top boxes
- Banking terminals
- Internet terminals.

GENERAL DESCRIPTION

The TDA8020HL is a one-chip dual smart card interface. Controlled by the I²C-bus, it guarantees conformity to ISO 7816 or EMV norms with very few external components.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|----------------|---------|--|----------|
| | NAME | DESCRIPTION | VERSION |
| TDA8020HL | LQFP32 | plastic low profile quad flat package; 32 leads; body $7 \times 7 \times 1.4$ mm | SOT358-1 |

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QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------|---|--|------|------|----------|--------------|
| V_{DD} | supply voltage on pins V_{DD} and V_{DDA} | | 2.5 | – | 6.5 | V |
| V_{DDI} | supply voltage for interface signals | | 1.5 | – | V_{DD} | V |
| I_{DD} | supply current (I_{DD} and I_{DDA}) | $V_{DD} = 3.3$ V; inactive mode | – | – | 150 | μ A |
| | | $V_{DD} = 3.3$ V; Power-down mode; 2 cards activated; $V_{CC1} = V_{CC2} = 5$ V; $I_{CC1} = I_{CC2} = 100$ μ A; CLK1 and CLK2 stopped | – | – | 2 | mA |
| | | $V_{DD} = 3.3$ V; active mode; $V_{CC1} = V_{CC2} = 5$ V; $I_{CC1} + I_{CC2} = 80$ mA; CLK1 = CLK2 = 5 MHz | – | – | 400 | mA |
| | | $V_{DD} = 3.3$ V; active mode; $V_{CC1} = V_{CC2} = 3$ V; $I_{CC1} = I_{CC2} = 10$ mA; CLK1 = CLK2 = 5 MHz | – | – | 80 | mA |
| V_{CC1}, V_{CC2} | supply voltage for card 1 and 2 5 V card 3 V card | note 1 | 4.75 | – | 5.25 | V |
| | | | 2.80 | – | 3.20 | V |
| I_{CC1}, I_{CC2} | supply current for card 1 and 2 | | 0 | – | 55 | mA |
| V_{th1} | threshold voltage for the supervisor on V_{DD} | | 2.1 | – | 2.4 | V |
| V_{hys1} | hysteresis on V_{th1} | | 50 | – | 100 | mV |
| T_{amb} | ambient temperature | | –25 | – | +85 | $^{\circ}$ C |

Note

- Both cards are not allowed to operate at maximum current at the same time at minimum supply voltage.

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BLOCK DIAGRAM

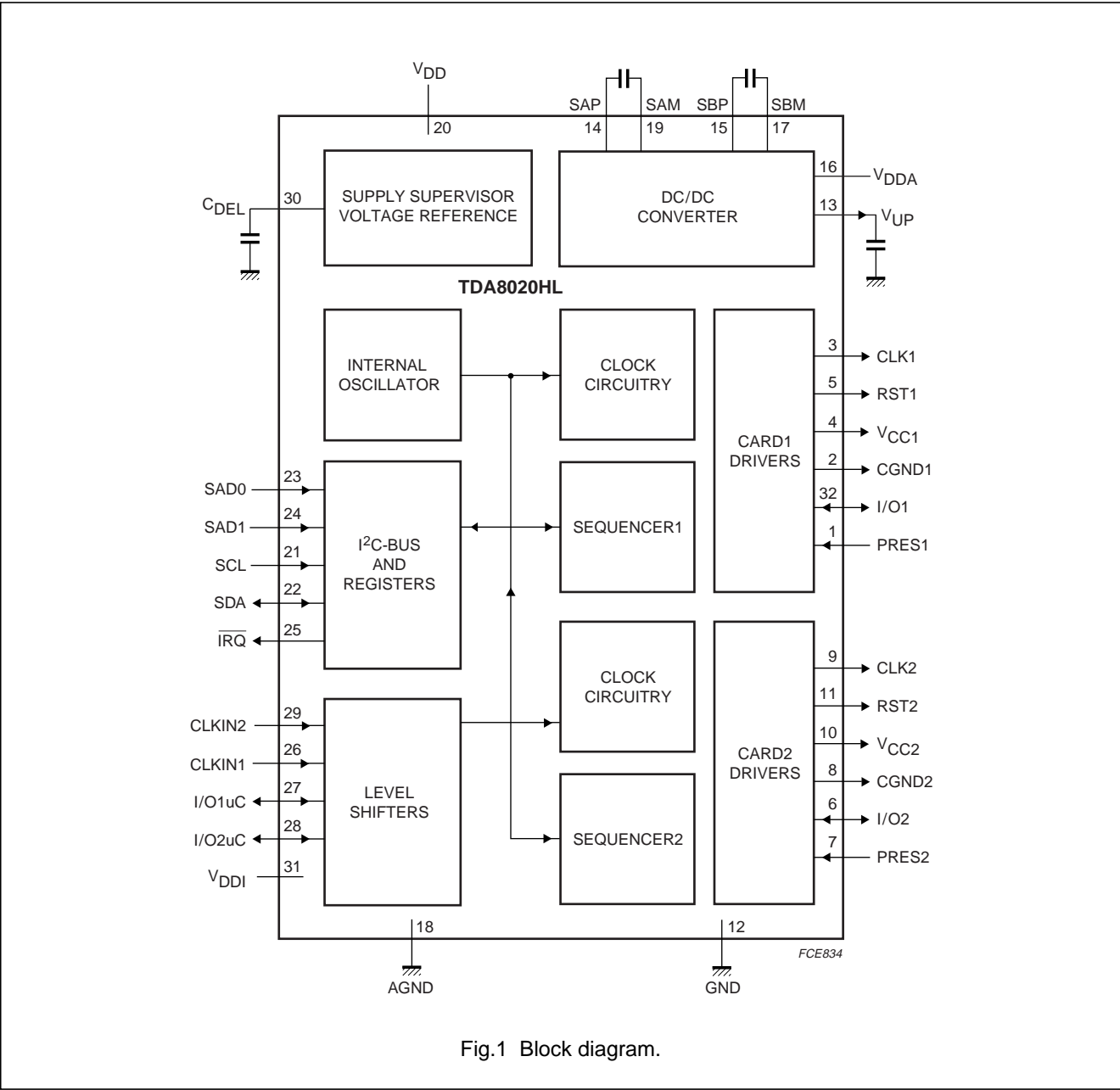


Fig.1 Block diagram.

Dual smart card interface

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PINNING

| SYMBOL | PIN | DESCRIPTION |
|------------------|-----|--|
| PRES1 | 1 | card 1 presence contact input (active HIGH) |
| CGND1 | 2 | ground connection output to card 1 (C5 contact) |
| CLK1 | 3 | clock output to card 1 (C3 contact) |
| V _{CC1} | 4 | supply voltage output to card 1 (C1 contact); decouple to pin CGND1 with 2×100 nF capacitors with ESR < 100 mΩ |
| RST1 | 5 | reset output to card 1 (C2 contact) |
| I/O2 | 6 | I/O contact to card 2 (C7 contact); internal 15 kΩ pull-up resistance to pin V _{CC2} |
| PRES2 | 7 | card 2 presence contact input (active HIGH) |
| CGND2 | 8 | ground connection output to card 2 (C5 contact) |
| CLK2 | 9 | clock output to card 2 (C3 contact) |
| V _{CC2} | 10 | supply voltage output to card 2 (C1 contact); decouple to pin CGND2 with 2×100 nF capacitors with ESR < 100 mΩ |
| RST2 | 11 | reset output to card 2 (C2 contact) |
| GND | 12 | ground connection |
| V _{UP} | 13 | output of DC/DC converter; a 220 nF capacitor with ESR < 100 mΩ must be connected to pin AGND |
| SAP | 14 | capacitors connection for the DC/DC converter; a 220 nF capacitor with ESR < 100 mΩ must be connected between pins SAP and SAM |
| SBP | 15 | capacitors connection for the DC/DC converter; a 220 nF capacitor with ESR < 100 mΩ must be connected between pins SBP and SBM |
| V _{DDA} | 16 | analog supply voltage for the DC/DC converter |
| SBM | 17 | capacitors connection for the DC/DC converter; a 220 nF capacitor with ESR < 100 mΩ must be connected between pins SBP and SBM |
| AGND | 18 | analog ground connection for the DC/DC converter |
| SAM | 19 | capacitors connection for the DC/DC converter; a 220 nF capacitor with ESR < 100 mΩ must be connected between pins SAP and SAM |
| V _{DD} | 20 | power supply voltage |
| SCL | 21 | serial clock input of the I ² C-bus (open drain) |
| SDA | 22 | serial data input/output of the I ² C-bus (open drain) |
| SAD0 | 23 | I ² C-bus address selection input 0 |
| SAD1 | 24 | I ² C-bus address selection input 1 |
| IRQ | 25 | interrupt request output to host (open drain; active LOW) |
| CLKIN1 | 26 | external clock input for card 1 |
| I/O1uC | 27 | I/O connection to host for card 1; internal 22 kΩ pull-up resistor to V _{DDI} |
| I/O2uC | 28 | I/O connection to host for card 2; internal 22 kΩ pull-up resistor to V _{DDI} |
| CLKIN2 | 29 | external clock input for card 2 |
| C _{DEL} | 30 | delay capacitor connection for the voltage supervisor (1 ms per 2 nF) |
| V _{DDI} | 31 | interface signals reference supply voltage |
| I/O1 | 32 | I/O contact to card 1 (C7 contact); internal 15 kΩ pull-up resistor to V _{CC1} |

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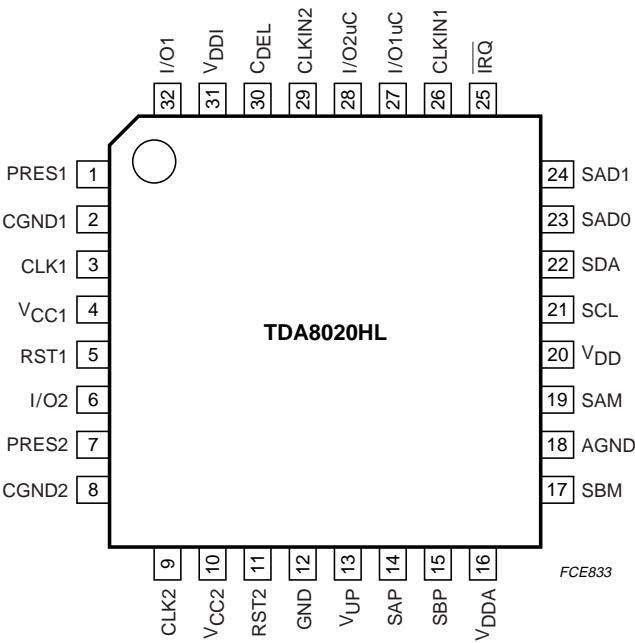


Fig.2 Pin configuration.

Dual smart card interface

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FUNCTIONAL DESCRIPTION

Throughout this specification, it is assumed that the reader is familiar with ISO 7816 norm terminology.

Supply

The TDA8020HL operates with a supply voltage from 2.5 to 6.5 V. An integrated voltage supervisor ensures that no spike appears on cards contacts during power-on or off. The supervisor also initializes the device, and forces an automatic emergency deactivation of the contacts in the event of a supply drop-out.

As long as the supply voltage is below the threshold voltage V_{th1} , the capacitor C_{DEL} remains uncharged. When the supply voltage reaches V_{th1} and V_{hys1} , then C_{DEL} is charged with a small current source of approximately 2 μ A. When the voltage on C_{DEL} reaches V_{th2} , then the supervisor is no longer active. As long as the supervisor is active (pin \overline{IRQ} is LOW), bit SUPL in the status register is set. When pin \overline{IRQ} goes HIGH the supervisor becomes inactive (see Fig.3).

Separate supply pins are used for the DC/DC converter, allowing specific decoupling for counteracting the noise the switching transistors may induce on the supply.

A specific reference supply voltage, V_{DDI} , is used for the interface signals CLKIN1, CLKIN2, I/O1uC, I/O2uC, SAD0, SAD1, SCL, SDA and \overline{IRQ} , which can be lower than V_{DD} (minimum 1.5 V), thus allowing direct control with a low voltage supplied device.

Pins SCL, SDA and \overline{IRQ} are open-drain outputs, and may be externally pulled up to a voltage higher than V_{DD} .

I²C-bus

A 400 kHz I²C-bus slave interface is used for configuring the device and reading the status. The bus has 2 addresses, one for each card. 4 devices may be used in parallel due to the address selection pins SAD0 and SAD1 (see Table 1).

Table 1 Proposed addresses

| PIN SAD1 | PIN SAD0 | CARD 1 | CARD 2 |
|----------|----------|--------|--------|
| LOW | LOW | 40H | 48H |
| LOW | HIGH | 42H | 4AH |
| HIGH | LOW | 44H | 4CH |
| HIGH | HIGH | 46H | 4EH |

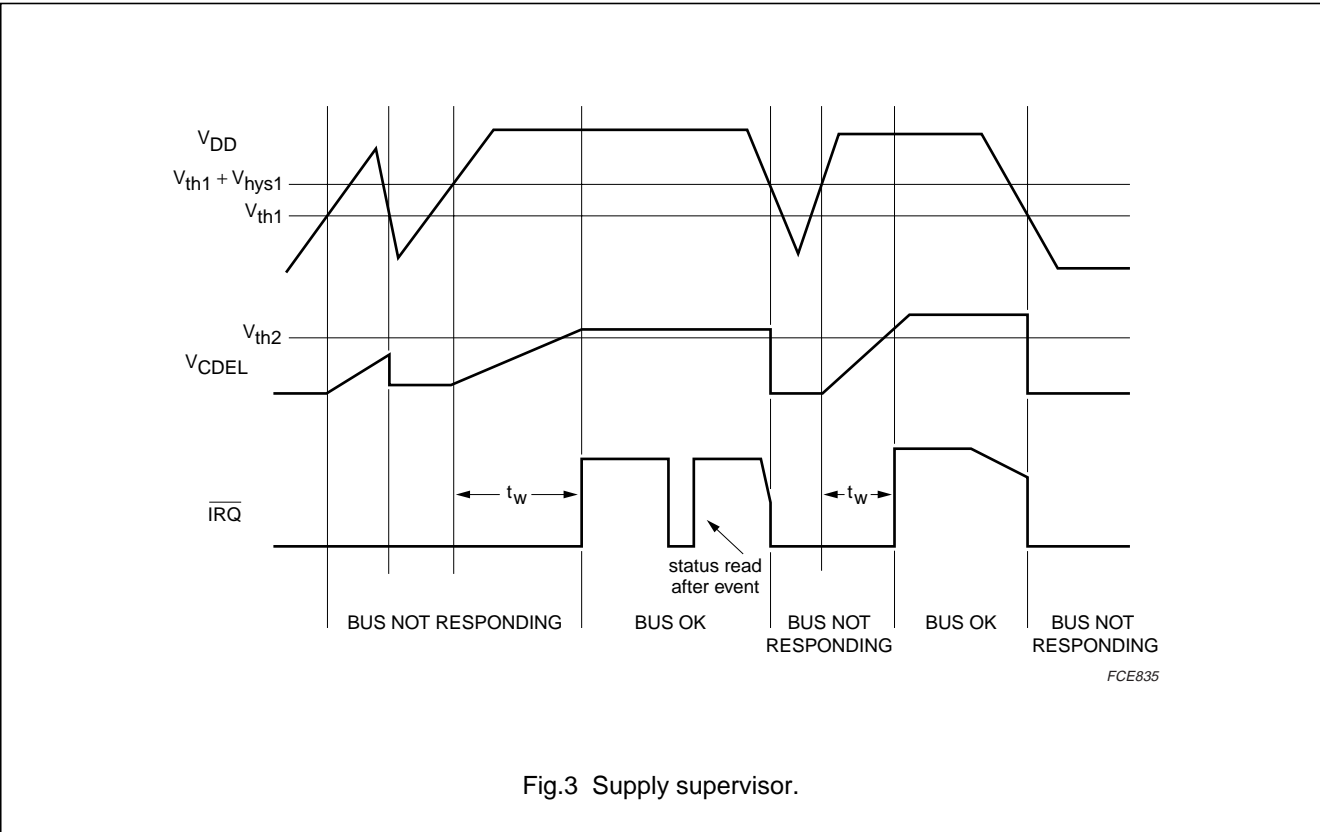


Fig.3 Supply supervisor.

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WRITING COMMANDS

START, ADDRESS, WRITE, CONTROL byte, STOP.

Table 2 CONTROL bits (all bits cleared after power-on)

| NAME | BIT | DESCRIPTION |
|------------|-----|---|
| START/STOP | 0 | when set, initiates an activation and a cold reset procedure; when reset, initiates a deactivation sequence |
| WARM | 1 | when set, initiates a warm reset procedure; automatically reset by hardware when the card starts answering or when the card is declared mute |
| 3 and 5 V | 2 | when set, $V_{CC} = 3\text{ V}$; when reset, $V_{CC} = 5\text{ V}$ |
| PDOWN | 3 | when set, the configuration defined by bit CLKPD is applied on pin CLK, and the circuit enters the Power-down mode; when reset, the circuit goes back to normal (active) mode |
| CLKPD | 4 | when set, CLK is stopped HIGH during Power-down mode; when reset, CLK is stopped LOW in Power-down mode |
| CLKSEL1 | 5 | bits 5 and 6 determine the clock to the card in normal mode according to Table 3 |
| CLKSEL2 | 6 | |
| I/OEN | 7 | when set, I/O is transferred on I/OuC; when reset, I/O to I/OuC is high-impedance |

When deactivating the card, by resetting the START bit, only bit 0 must be changed.

The clock to the cards in active mode is selected with bits CLKSEL1 and CLKSEL2; see Table 3.

Table 3 Selecting the card clock.

| BIT CLKSEL2 | BIT CLKSEL1 | CLOCK OUTPUT |
|-------------|-------------|--------------|
| 0 | 0 | CLKIN/8 |
| 0 | 1 | CLKIN/4 |
| 1 | 0 | CLKIN/2 |
| 1 | 1 | CLKIN |

All frequency changes are synchronous, thus ensuring that no pulse is shorter than 45% of the smallest period. For cards power reduction modes, CLKIN may be stopped after switching to STOP LOW or STOP HIGH. CLKIN should be restarted before leaving this mode.

A correct duty factor can not be guaranteed in the CLKIN configuration, as it depends on the duty factor of the CLKIN signal.

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READING STATUS

START, ADDRESS, READ, STATUS byte, STOP.

Table 4 STATUS bits (all bits cleared after power-on, except SUPL and PRES)

| NAME | BIT | DESCRIPTION |
|--------|-----|---|
| PRES | 0 | set when the card is present; reset when the card is not present |
| PRESL | 1 | set when the card has been inserted or extracted; reset when the status has been read |
| I/O | 2 | set when I/O is HIGH and reset if I/O is LOW |
| SUPL | 3 | set when the supervisor has signalled a fault; reset when the status has been read |
| PROT | 4 | set when an overload or an overheating has occurred during a session; reset when the status has been read |
| MUTE | 5 | set during ATR when the selected card has not answered during the ISO 7816 time slots |
| EARLY | 6 | set during ATR when the selected card has answered too early |
| ACTIVE | 7 | set if the card is active; reset if the card is inactive |

When one of the bits PRES, MUTE, EARLY and PROT is set, then pin $\overline{\text{IRQ}}$ goes LOW until the status byte has been read. After power-on, bit SUPL is set until the status byte has been read, and pin $\overline{\text{IRQ}}$ is LOW until the supervisor becomes inactive.

DC/DC converter

V_{CC1} is the supply voltage for card 1 contacts, V_{CC2} for card 2 contacts. Card 1 and card 2 may be independently powered-down, powered at 5 V or powered at 3 V. A capacitor type step-up converter is used for generating these voltages. This step-up converter acts either as a doubler, tripler or follower.

If V_{CC} is the maximum value of V_{CC1} and V_{CC2} , then there are 4 possible situations:

- $V_{DD} = 3 \text{ V}$ and $V_{CC} = 3 \text{ V}$: in this case, the DC/DC converter acts as a doubler with a regulation of approximately 4.0 V
- $V_{DD} = 3 \text{ V}$ and $V_{CC} = 5 \text{ V}$: in this case, the DC/DC converter acts as a tripler with a regulation of approximately 5.5 V
- $V_{DD} = 5 \text{ V}$ and $V_{CC} = 3 \text{ V}$: in this case, the DC/DC converter acts as a follower: V_{DD} is applied on V_{UP}
- $V_{DD} = 5 \text{ V}$ and $V_{CC} = 5 \text{ V}$: in this case, the DC/DC converter acts as a doubler with a regulation of approximately 5.5 V.

The switch between the modes is automatically executed when V_{DD} is approximately 3.4 V.

Each card may independently draw a current up to 65 mA, also during activation, with a supply voltage from 2.5 V up to 6.5 V provided the sum of I_{CC1} and I_{CC2} does not exceed 80 mA.

If $V_{DD} > 3 \text{ V}$, for 5 V cards, then both cards can draw up to 55 mA at the same time.

If $V_{DD} > 3.3 \text{ V}$, for 3 V cards, then both cards can draw up to 50 mA at the same time.

The DC/DC converter is powered with specific pins (V_{DDA} and AGND) to enable separate decoupling.

The output voltage, V_{UP} , is internally fed to the V_{CC} generators. V_{CC1} , V_{CC2} and CGND1, CGND2 are used as a reference for all other cards contacts.

Sequencers and clock counter

Two sequencers are used to ensure activation and deactivation sequences according to ISO 7816 and EMV norms, even in the event of an emergency (card removal during transaction, supply drop-out and hardware problem).

The sequencers are clocked by the internal oscillator.

The activation of a card is initiated by setting the card select bit and the start bit within the control register. This is only possible if the card is present and if the voltage supervisor is not active.

During activation the DC/DC converter is initiated (except if another card is already powered up or if $V_{DD} = 5 \text{ V}$ and $V_{CC} = 3 \text{ V}$). V_{CC} then goes high to the selected voltage (3 or 5 V), the I/O lines are then enabled and the clock is started with RST LOW.

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If a start bit is detected on the I/O during the first 200 CLK pulses, then it is omitted. If a start bit is detected between 200 and 352 CLK pulses, then bit EARLY is set in the status register. If the card starts answering before 41950 CLK pulses, then RST remains LOW level. If not, after 41950 CLK pulses, RST is toggled HIGH. If, again, a start bit is detected within 352 CLK pulses, bit EARLY is set in the status register. If the card does not answer before 41950 new CLK pulses, then bit MUTE is set in the status register. If the card answers within the correct window, then the CLK count is stopped and the system controller may send commands to the card.

Deactivation is initiated either by the system controller (reset bit START), or automatically in the event of a hardware problem or supply drop-out. With a supply drop-out both cards are deactivated at the same time.

During deactivation, RST goes LOW, the clock is stopped and the I/O lines go LOW. V_{CC} then goes low with a controlled slope and the DC/DC converter is stopped if no card is active.

Outside a session, cards contacts are forced low impedance to CGND.

Activation sequence

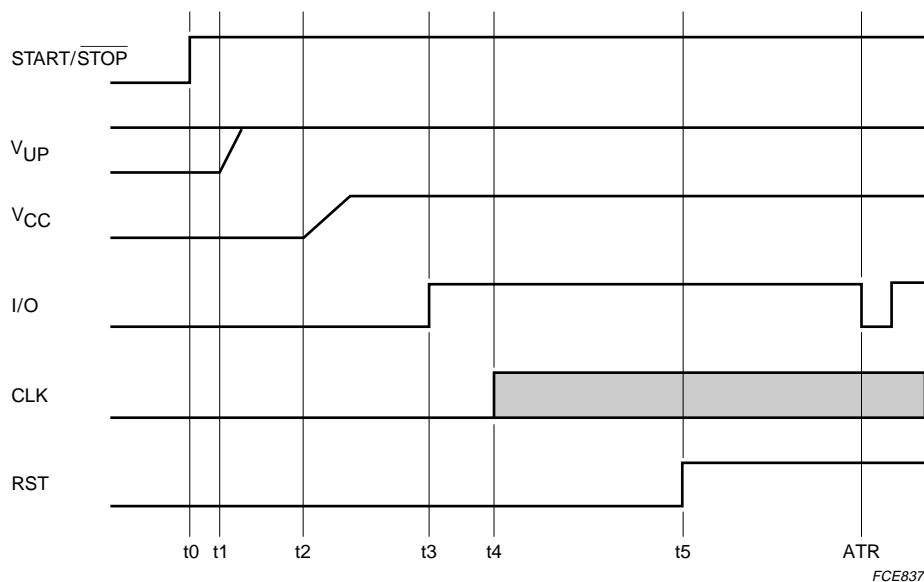
When the cards are inactive, V_{CC} , CLK, RST and I/O are LOW, with low impedance with respect to CGND. The DC/DC converter is stopped.

When everything is satisfactory (voltage supply, card present and no hardware problems), the system controller may initiate an activation sequence of a present card (see Fig.4):

- The DC/DC converter is started (t_1). If one card was already active, then the DC/DC converter was already on, and nothing more occurs at this step
- V_{CC} starts rising from 0 to 5 or 3 V with a controlled rise time of 0.14 V/ μ s typical (t_2)
- I/O rises to V_{CC} (t_3); internal 10 k Ω pull-up resistors to V_{CC}
- CLK is sent to the card and RST is enabled ($t_4 = t_{act}$).

If the card does not answer within the first 41950 CLK cycles, then RST is raised HIGH (t_5).

The sequencer is clocked by $f_{int}/64$ which leads to a time interval T of 25 μ s typical. Thus $t_1 = 0$ to $T/64$; $t_2 = t_1 + 3T/2$; $t_3 = t_1 + 7T/2$ and $t_4 = t_1 + 4T$.



$t_4 = t_{act}$.

Fig.4 Activation sequence.

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Deactivation sequence

When the session is completed, the microcontroller resets bit START/ $\overline{\text{STOP}}$ to logic 0 (t10). The circuit then executes an automatic deactivation sequence (see Fig.5):

- Card reset (RST falls LOW) (t11)
- CLK is stopped (t12)
- I/O falls to 0 V (t13)
- V_{CC} falls to 0 V with typical 0.14 V/ μs slew rate (t14)
- The DC/DC converter is stopped (if both cards are inactive) and CLK, RST, V_{CC} and I/O become low impedance to CGND (t15).

$$t11 = t10 + T/64; t12 = t11 + T/2; t13 = t11 + T; \\ t14 = t11 + 3T/2; t15 = t11 + 7T/2.$$

The deactivation time t_{de} is the time that V_{CC} needs to drop below 0.4 V from START/ $\overline{\text{STOP}}$ to logic 0 (t10).

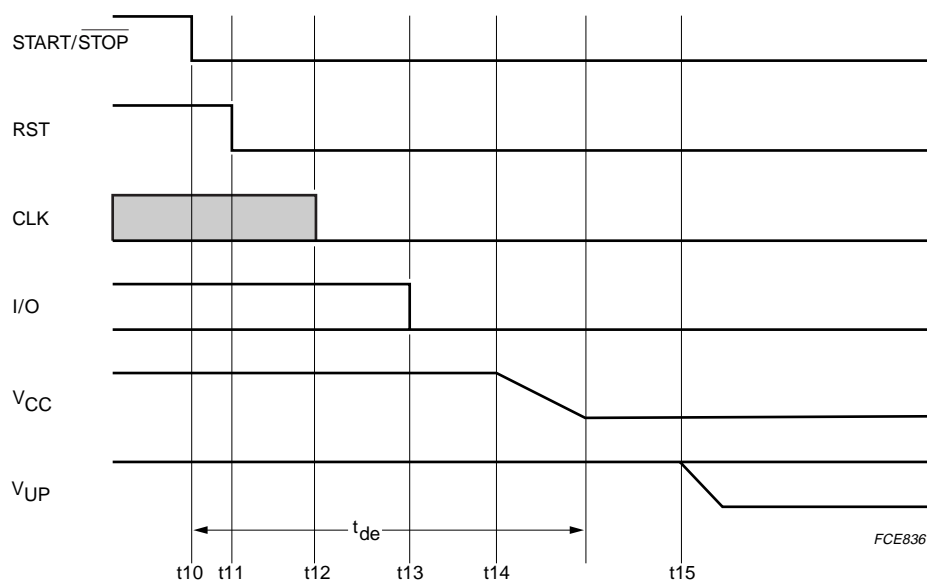


Fig.5 Deactivation sequence.

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Protections

The current on pin CLK is limited to ± 70 mA.

The current on pin RST is limited to ± 20 mA; if the current reaches this value with RST LOW, then an emergency deactivation sequence is performed, $\overline{\text{IRQ}}$ is pulled LOW and bit PROT is set in the status register.

The current on pins I/O is limited to $+15$ and -15 mA.

The current on V_{CC} is limited to 90 mA; if I_{CC} reaches this value, then an emergency deactivation sequence is performed, $\overline{\text{IRQ}}$ is pulled LOW and bit PROT is set in the status register.

In the event of overcurrent on V_{CC} , card take-off during a session, overheating, or overcurrent on RST, then the TDA8020HL performs an automatic emergency deactivation sequence on the corresponding card, resets bit START/STOP and pulls pin $\overline{\text{IRQ}}$ LOW.

In the event of overheating or supply drop-out, the TDA8020HL performs an automatic emergency deactivation sequence on both cards, resets both bits START/STOP and pulls pin $\overline{\text{IRQ}}$ LOW.

Clock inputs and data inputs/outputs to the system controller

CLKIN1 is the input clock for card 1, CLKIN2 for card 2. They may be driven separately from the system controller, or be tied together externally and driven with the same signal.

An RC filter is needed on these lines in order to limit the influence of possible fast transitions.

I/O1uC is the data signal to or from card 1, I/O2uC to or from card 2. They can be driven separately from the system controller, in which case both bits I/OEN may be set to logic 1. They can also be driven by the same signal, in which event they have to be tied together externally, but each bit I/OEN has to be set or reset according to the addressed card.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|---|-----------------------------|------|----------------|------|
| V_{DD} | supply voltage on pins V_{DD} and V_{DDA} | | -0.5 | +6.5 | V |
| V_{DDI} | supply voltage for interface signals | | -0.5 | +6.5 | V |
| V_n | input voltage on pins SAP, SAM, SBP, SBM and V_{UP} on all other pins | | -0.5 | +7.5 | V |
| | | | -0.5 | $V_{DD} + 0.5$ | V |
| I_n | DC current from or to pins SAP, SAM, SBP, SBM and V_{UP} from or to all other pins | | -200 | +200 | mA |
| | | | -5 | +5 | mA |
| P_{tot} | total power dissipation | $T_{amb} = -20$ to $+85$ °C | — | 460 | mW |
| T_{stg} | storage temperature | | -55 | +150 | °C |
| T_j | junction temperature | | — | 125 | °C |
| V_{es} | electrostatic discharge voltage on pins I/O1, V_{CC1} , RST1, CLK1, CGND1, PRES1, I/O2, V_{CC2} , RST2, CLK2, CGND2 and PRES2 on all other pins | | -6 | +6 | kV |
| | | | -2 | +2 | kV |

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THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---------------|---|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 80 | K/W |

CHARACTERISTICS

$V_{DD} = 3.3\text{ V}$; $V_{DDI} = 1.5\text{ V}$; $f_{CLKIN1} = f_{CLKIN2} = 10\text{ MHz}$; $GND = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|------------------------|---|--|------|------|----------------|------|
| Temperature | | | | | | |
| T_{amb} | ambient temperature | | -25 | – | +85 | °C |
| Supply | | | | | | |
| V_{DD} | supply voltage on pins V_{DD} and V_{DDA} | | 2.5 | – | 6.5 | V |
| I_{DD} | supply current (I_{DD} and I_{DDA}) | inactive mode | – | – | 150 | μA |
| | | Power-down mode; 2 cards activated; $V_{CC1} = V_{CC2} = 5\text{ V}$; $I_{CC1} = I_{CC2} = 100\text{ μA}$; CLK1 and CLK2 stopped | – | – | 2.5 | mA |
| | | active mode; $V_{CC1} = V_{CC2} = 5\text{ V}$; $I_{CC1} + I_{CC2} = 80\text{ mA}$; CLK1 = CLK2 = 5 MHz | – | – | 400 | mA |
| | | active mode; $V_{CC1} = V_{CC2} = 3\text{ V}$; $I_{CC1} = I_{CC2} = 10\text{ mA}$; CLK1 = CLK2 = 5 MHz | – | – | 80 | mA |
| V_{DDI} | supply voltage for interface signals | | 1.5 | – | V_{DD} | V |
| I_{DDI} | supply current for interface signals | | – | – | 120 | μA |
| V_{th1} | threshold voltage on V_{DD} | falling | 2.1 | – | 2.4 | V |
| V_{hys1} | hysteresis on V_{th1} | | 50 | – | 100 | mV |
| V_{th2} | threshold voltage on pin C_{DEL} | | – | 1.38 | – | V |
| V_{CDEL} | voltage on pin C_{DEL} | | – | – | $V_{DD} + 0.3$ | V |
| I_{CDEL} | output current at pin C_{DEL} | pin grounded (charge) | – | –2 | – | μA |
| | | $V_{CDEL} = V_{DD}$ (discharge) | – | 5 | – | mA |
| t_W | width of the internal ALARM pulse | $C_{DEL} = 22\text{ nF}$ | – | 10 | – | ms |
| DC/DC converter | | | | | | |
| f_{int} | internal oscillator frequency | | 2 | 2.5 | 3 | MHz |
| V_{UP} | voltage on pin V_{UP} | at least one 5 V card | – | 5.5 | – | V |
| | | both cards 3 V | – | 4 | – | V |
| V_{dt} | detection voltage for doubler, tripler and follower selection | | – | 3.4 | – | V |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|--|-----------------------|------|-----------------|------|
| Card supply voltages (pins V_{CC1} and V_{CC2}); note 1 | | | | | | |
| V _{o(inactive)} | output voltage in inactive mode | no load | 0 | – | 0.1 | V |
| | | I _{inactive} = 1 mA | 0 | – | 0.3 | V |
| I _{inactive} | current from V _{CC} when inactive | pin grounded | – | – | –1 | mA |
| V _{CC(ripple)} | output voltage including ripple | active mode; I _{CC} < 65 mA; 5 V card; I _{CC1} + I _{CC2} < 80 mA; 2.5 V < V _{DD} < 6.5 V | 4.75 | 5 | 5.25 | V |
| | | active mode; I _{CC} < 65 mA; 3 V card; I _{CC1} + I _{CC2} < 80 mA; 2.5 V < V _{DD} < 6.5 V | 2.8 | 3 | 3.2 | V |
| | | active mode; current pulses of 40 nAs with I < 200 mA and t < 400 ns; f < 20 MHz; 5 V card | 4.6 | – | 5.4 | V |
| | | active mode; current pulses of 24 nAs with I < 200 mA and t < 400 ns; f < 20 MHz; 3 V card | 2.76 | – | 3.24 | V |
| V _{CC(load)} | output voltage when both slots fully loaded | active mode; V _{DD} > 3 V; I _{CC1} < 55 mA; I _{CC2} < 55 mA; 5 V cards | 4.6 | – | 5.4 | V |
| | | active mode; V _{DD} > 3.3 V; I _{CC} < 50 mA; I _{CC2} < 50 mA; 3 V cards | 2.76 | – | 3.24 | V |
| I _{CC} | output current | from 0 to 5 V (5 V card); the other card at full load; V _{DD} > 3 V | – | – | –55 | mA |
| | | from 0 to 3 V (3 V card); the other card at full load; V _{DD} > 3.3 V | – | – | –50 | mA |
| | | V _{CC} shorted to GND | – | – | –100 | mA |
| V _{ripple(p-p)} | ripple voltage (peak-to-peak value) | from 20 kHz to 200 MHz | – | – | 350 | mV |
| SR | slew rate | up or down (maximum capacitance is 300 nF) | 0.08 | 0.14 | 0.20 | V/μs |
| Reset output to the cards (pins RST1 and RST2) | | | | | | |
| V _{o(inactive)} | output voltage in inactive mode | no load | 0 | – | 0.1 | V |
| | | I _{inactive} = 1 mA | 0 | – | 0.3 | V |
| I _{inactive} | current from pin RST when inactive | pin grounded | 0 | – | –1 | mA |
| V _{OL} | LOW-level output voltage | I _{OL} = 200 μA | 0 | – | 0.3 | V |
| V _{OH} | HIGH-level output voltage | I _{OH} < –200 μA | V _{CC} – 0.5 | – | V _{CC} | V |
| t _r | rise time | C _L = 30 pF | – | – | 0.1 | μs |
| t _f | fall time | C _L = 30 pF | – | – | 0.1 | μs |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|--|----------------|------|----------------|---------------|
| Clock output to the cards (pins CLK1 and CLK2) | | | | | | |
| $V_{O(inactive)}$ | output voltage in inactive mode | no load | 0 | – | 0.1 | V |
| | | $I_{inactive} = 1 \text{ mA}$ | 0 | – | 0.3 | V |
| $I_{inactive}$ | current from pin CLK when inactive | pin grounded | 0 | – | –1 | mA |
| V_{OL} | LOW-level output voltage | $I_{OL} = 200 \text{ } \mu\text{A}$ | 0 | – | 0.3 | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} < -200 \text{ } \mu\text{A}$ | $V_{CC} - 0.5$ | – | V_{CC} | V |
| t_r | rise time | $C_L = 30 \text{ pF}$ | – | – | 8 | ns |
| t_f | fall time | $C_L = 30 \text{ pF}$ | – | – | 8 | ns |
| f_{clk} | clock frequency | 1 MHz Idle configuration | 1 | – | 1.5 | MHz |
| | | operational | 0 | – | 10 | MHz |
| δ | duty factor | $C_L = 30 \text{ pF}$ | 45 | – | 55 | % |
| SR | slew rate (rise and fall) | $C_L = 30 \text{ pF}$ | 0.2 | – | – | V/ns |
| Data lines (pins I/O1 and I/O2); note 2 | | | | | | |
| $V_{O(inactive)}$ | output voltage in inactive mode | no load | 0 | – | 0.1 | V |
| | | $I_{inactive} = 1 \text{ mA}$ | – | – | 0.3 | V |
| $I_{inactive}$ | current from pin I/O when inactive | pin grounded | – | – | –1 | mA |
| V_{OL} | LOW-level output voltage | $I_{OL} = 1 \text{ mA}$ | 0 | – | 0.3 | V |
| V_{OH} | HIGH-level output voltage | no DC load | $0.9V_{CC}$ | – | $V_{CC} + 0.1$ | V |
| | | $I_{OH} < -20 \text{ } \mu\text{A}$ | $0.8V_{CC}$ | – | $V_{CC} + 0.1$ | V |
| | | $I_{OH} < -40 \text{ } \mu\text{A}$ | $0.75V_{CC}$ | – | $V_{CC} + 0.1$ | V |
| I_{edge} | current from pins I/O1 and I/O2 when active pull-up | $V_{OH} = 0.9V_{CC}$; $C_L = 80 \text{ pF}$ | –1 | – | – | mA |
| $t_{d(edge)}$ | delay between falling edge on pins I/O1, I/O2, I/O1uC, I/O2uC and width of active pull-up pulse | | – | 500 | 650 | ns |
| V_{IL} | LOW-level input voltage | | –0.3 | – | +0.8 | V |
| V_{IH} | HIGH-level input voltage | | 1.5 | – | V_{CC} | V |
| I_{IL} | LOW-level input current on pin I/O | $V_{IL} = 0$ | – | – | 600 | μA |
| I_{LIH} | HIGH-level input leakage current on pin I/O | $V_{IH} = V_{CC}$ | – | – | 10 | μA |
| $t_{i(r)}, t_{i(f)}$ | input transition times | from $V_{IL(max)}$ to $V_{IH(min)}$ | – | – | 1.5 | μs |
| $t_{o(r)}, t_{o(f)}$ | output transition times | $C_L < 80 \text{ pF}$; no DC load; 10% to 90% from 0 to V_{CC1} and V_{CC2} | – | – | 0.1 | μs |
| C_i | input capacitance on pins I/O1 and I/O2 | | – | – | 10 | pF |
| $R_{pu(int)}$ | internal pull-up resistance between pin I/O and V_{CC} | | 12 | 15 | 18 | k Ω |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|--|--|---------------|------|-----------------|--------------------|
| f_{\max} | maximum frequency on pins I/O1 and I/O2 | | – | – | 500 | kHz |
| Data lines (pins I/O1uC and I/O2uC); note 3 | | | | | | |
| V_{OL} | LOW-level output voltage | $I_{OL} = 1 \text{ mA}$ | 0 | – | 0.4 | V |
| V_{OH} | HIGH-level output voltage | no DC load | $0.9V_{DDI}$ | – | $V_{DDI} + 0.2$ | V |
| | | $I_{OH} < -10 \mu\text{A}$ | $0.75V_{DDI}$ | – | $V_{DDI} + 0.2$ | V |
| V_{IL} | LOW-level input voltage | | –0.3 | – | $0.25V_{DDI}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DDI}$ | – | $V_{DDI} + 0.3$ | V |
| I_{IL} | LOW-level input current | $V_{IL} = 0$ | – | – | 600 | μA |
| I_{LIH} | HIGH-level input leakage current | $V_{IH} = V_{DDI}$ | – | – | 10 | μA |
| $t_{i(r)}, t_{i(f)}$ | input transition times | from $V_{IL(\max)}$ to $V_{IH(\min)}$ | – | – | 1 | μs |
| $t_{o(r)}, t_{o(f)}$ | output transition times | $C_L < 30 \text{ pF}$; 10% to 90% from 0 to V_{DDI} | – | – | 0.1 | μs |
| $R_{pu(int)}$ | internal pull-up resistance | between I/O1uC, I/O2uC and V_{DDI} | 15 | 22 | 30 | $\text{k}\Omega$ |
| Timing | | | | | | |
| t_{act} | activation sequence duration | | – | – | 135 | μs |
| t_{de} | deactivation sequence duration | | – | – | 110 | μs |
| Protections and limitations | | | | | | |
| $I_{CC(sd)}$ | shutdown and limitation current at V_{CC1} and V_{CC2} | | – | –90 | – | mA |
| $I_{I/O(lim)}$ | limitation current on pins I/O1 and I/O2 | | –15 | – | +15 | mA |
| $I_{CLK(lim)}$ | limitation current on pins CLK1 and CLK2 | | –70 | – | +70 | mA |
| $I_{RST(sd)}$ | shutdown and limitation current on pins RST1 and RST2 | | –20 | – | +20 | mA |
| $T_{j(sd)}$ | shutdown die temperature | | – | 150 | – | $^{\circ}\text{C}$ |
| Card presence inputs (pins PRES1 and PRES2) | | | | | | |
| V_{IL} | LOW-level input voltage | | – | – | $0.3V_{DD}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD}$ | – | – | V |
| I_{LIL} | LOW-level input leakage current | $V_I = 0$ | – | – | ± 20 | μA |
| I_{LIH} | HIGH-level input leakage current | $V_I = V_{DD}$ | – | – | ± 20 | μA |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|-----------------------------------|---------------------|------|------------------------|---------------|
| Clock inputs (pins CLKIN1 and CLKIN2) | | | | | | |
| f_{ext} | external frequency applied on CLKIN1 and CLKIN2 | | 0 | – | 25 | MHz |
| V_{IL} | LOW-level input voltage | | 0 | – | $0.25V_{\text{DDI}}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{\text{DDI}}$ | – | $V_{\text{DDI}} + 0.3$ | V |
| $t_{\text{i(r)}}, t_{\text{i(f)}}$ | input transition times | | – | – | 100 | ns |
| Logic inputs (pins SAD0 and SAD1) | | | | | | |
| V_{IL} | LOW-level input voltage | | –0.3 | – | $0.25V_{\text{DDI}}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{\text{DDI}}$ | – | $V_{\text{DDI}} + 0.3$ | V |
| I_{LIL} | LOW-level input leakage current | | – | – | ± 20 | μA |
| I_{LIH} | HIGH-level input leakage current | | – | – | ± 20 | μA |
| C_{i} | input capacitance | | – | – | 10 | pF |
| Interrupt line (pin $\overline{\text{IRQ}}$; open-drain; active LOW output) | | | | | | |
| V_{OL} | LOW-level output voltage | $I_{\text{o}} = 2 \text{ mA}$ | – | – | 0.3 | V |
| I_{LH} | HIGH-level leakage current | | – | – | 10 | μA |
| Serial data input/output (pin SDA; open-drain) | | | | | | |
| V_{IL} | LOW-level input voltage | | –0.3 | – | $0.25V_{\text{DDI}}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{\text{DDI}}$ | – | $V_{\text{DDI}} + 0.3$ | V |
| I_{LH} | HIGH-level leakage current | | – | – | 1 | μA |
| I_{IL} | LOW-level input current | depends on the pull-up resistance | – | – | – | |
| V_{OL} | LOW-level output voltage | $I_{\text{OL}} = 3 \text{ mA}$ | – | – | 0.3 | V |
| Serial clock input (pin SCL; open-drain) | | | | | | |
| V_{IL} | LOW-level input voltage | | –0.3 | – | $0.25V_{\text{DDI}}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{\text{DDI}}$ | – | $V_{\text{DDI}} + 0.3$ | V |
| I_{LH} | HIGH-level leakage current | | – | – | 1 | μA |
| I_{IL} | LOW-level input current | depends on the pull-up resistance | – | – | – | |

Notes

- Two ceramic multilayer capacitors of minimum 100 nF with low ESR should be used in order to meet these specifications.
- Pin I/O1 has an internal 15 k Ω pull-up resistor to V_{CC1} and pin I/O2 has an internal 15 k Ω pull-up resistor to V_{CC2} .
- Pins I/O1uC and I/O2uC have an internal 22 k Ω pull-up resistor to V_{DDI} .

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APPLICATION INFORMATION

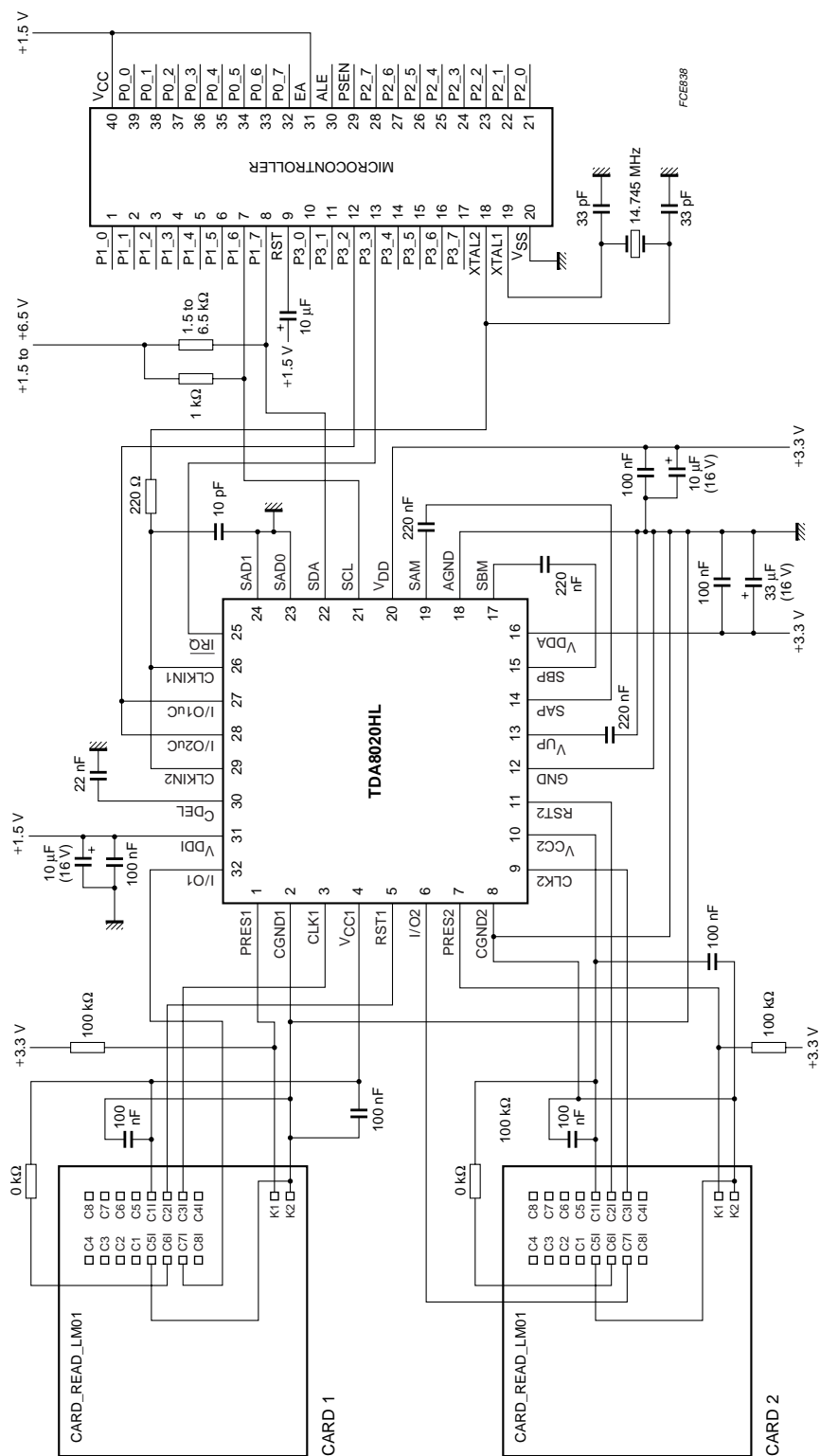


Fig.6 Application diagram.

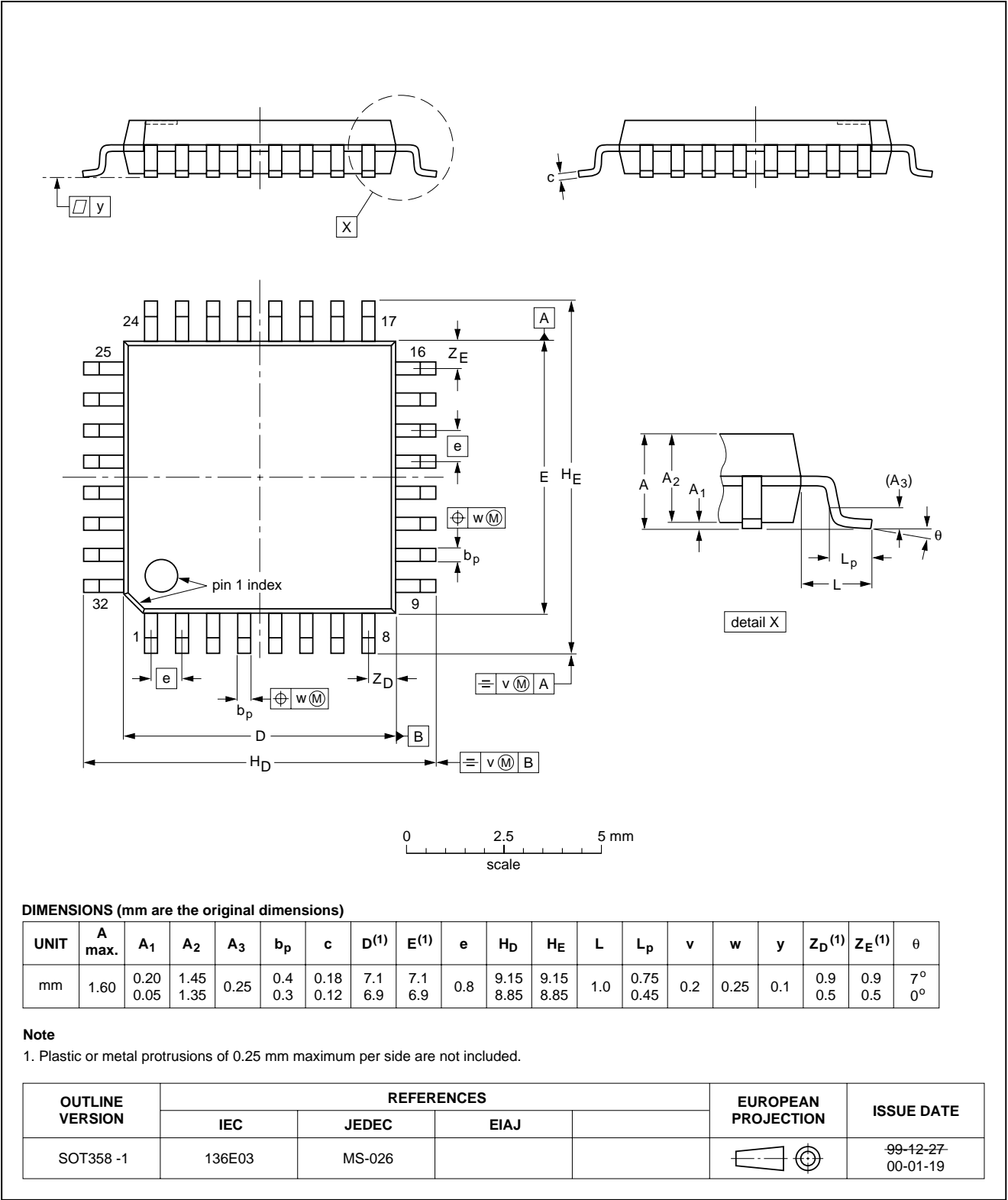
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PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm

SOT358-1



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SOLDERING**Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|---|-----------------------------------|-----------------------|
| | WAVE | REFLOW ⁽¹⁾ |
| BGA, HBGA, LFBGA, SQFP, TFBGA | not suitable | suitable |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS | not suitable ⁽²⁾ | suitable |
| PLCC ⁽³⁾ , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ⁽³⁾⁽⁴⁾ | suitable |
| SSOP, TSSOP, VSO | not recommended ⁽⁵⁾ | suitable |

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

| DATA SHEET STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾ | DEFINITIONS |
|----------------------------------|-------------------------------|--|
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Notes

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NOTES

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