

Transistors

RSR015P03

Silicon P-channel MOS FET

- 1) Low On-resistance
- 2) Space saving—small surface mount package (TSMT3)
- 3) 4V drive

Switching

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	3000
RSR015P03		○

Technical drawing of a TSMT3 package showing top and side views with dimensions.

Top View Dimensions:

- Overall width: 2.9
- Distance from top edge to center of pin 1: 0.4
- Pin 1 diameter: (3)
- Distance from center of pin 1 to center of pin 2: (1)
- Distance from center of pin 2 to center of pin 3: (2)
- Pin 2 diameter: 0.95
- Pin 3 diameter: 0.95
- Distance from center of pin 3 to right edge: 1.9
- Distance from center of pin 1 to right edge: 2.8

Side View Dimensions:

- Maximum height: 1.0MAX
- Height of top layer: 0.85
- Height of middle layer: 0.7
- Distance from top layer to middle layer: 0.1
- Distance from middle layer to bottom layer: 0.3-0.6
- Bottom layer thickness: 0.16

Legend:

- (1) Gate
- (2) Source
- (3) Drain

Notes:

- Each lead has same dimensions
- Abbreviated symbol : SM

(1) Gate
(2) Source
(3) Drain

*1 ESD PROTECTION DIODE
*2 BODY DIODE

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DS}	-30	V
Gate-source voltage		V_{GS}	± 20	V
Drain current	Continuous	I_D	± 1.5	A
	Pulsed	I_{DP}^{*1}	± 6	A
Source current (Body diode)	Continuous	I_S	-0.5	A
	Pulsed	I_{SP}^{*1}	-6	A
Total power dissipation		P_D^{*2}	1	W
Channel temperature		T_{ch}	150	$^{\circ}\text{C}$
Range of storage temperature		T_{stg}	-55 to +150	$^{\circ}\text{C}$

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$
 *2 Mounted on a ceramic board

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}^*$	125	°C/W

* Mounted on a ceramic board



Transistors

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	-30	—	—	V	$I_D = -1mA$, $V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30V$, $V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	-1.0	—	-2.5	V	$V_{DS} = -10V$, $I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	—	170	235	m Ω	$I_D = -1.5A$, $V_{GS} = -10V$
		—	270	375	m Ω	$I_D = -0.8A$, $V_{GS} = -4.5V$
		—	320	440	m Ω	$I_D = -0.8A$, $V_{GS} = -4V$
Forward transfer admittance	$ Y_{fs} ^*$	0.9	—	—	S	$V_{DS} = -10V$, $I_D = -0.8A$
Input capacitance	C_{iss}	—	190	—	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	—	45	—	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	—	30	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}^*$	—	6	—	ns	$V_{DD} \doteq -15V$ $I_D = -0.8A$
Rise time	t_r^*	—	8	—	ns	$V_{GS} = -10V$
Turn-off delay time	$t_{d(off)}^*$	—	22	—	ns	$R_L = 19\Omega$
Fall time	t_f^*	—	6	—	ns	$R_G = 10\Omega$
Total gate charge	Q_g^*	—	2.6	—	nC	$V_{DD} \doteq -15V$ $V_{GS} = -5V$
Gate-source charge	Q_{gs}^*	—	1.0	—	nC	$I_D = -1.5A$
Gate-drain charge	Q_{gd}^*	—	0.7	—	nC	$R_L = 10\Omega$ $R_G = 10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	—	—	-1.2	V	$I_S = -0.5A$, $V_{GS} = 0V$

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