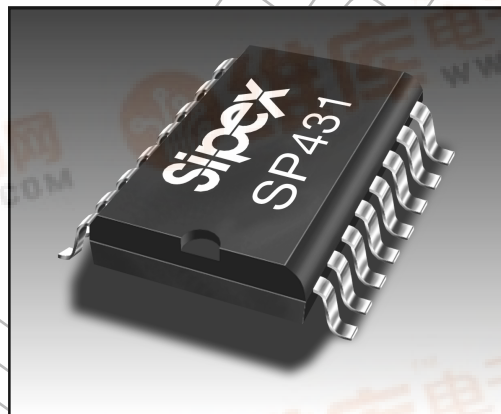




**SP431**

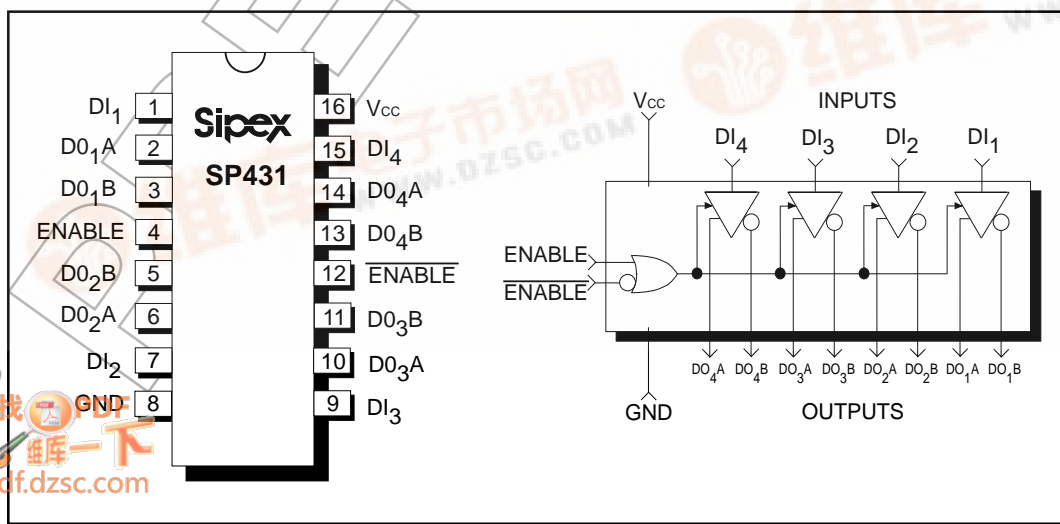
## High Speed, +3.3V Quad RS-422 Differential Line Driver

- Compatible with the EIA standard for RS-422 serial protocol
- Quad Differential Line Drivers
- Tri-state Output Control
- At Least 60Mbps Transmission Rates
- 6.0ns Typical Driver Propagation Delays
- Less than 1ns Typical Output Skew
- Single +3.3V Supply Operation
- Common Driver Enable Control
- Compatibility with the industry standard 26LV31



### DESCRIPTION

The **SP431** is a quad differential line driver that meets the specifications of the EIA standard RS-422 serial protocol. The **SP431** features Sipex's BiCMOS process allowing low power operational characteristics of CMOS technology while meeting all of the demands of the RS-422 serial protocol over 60Mbps under load. The RS-422 protocol allows up to 10 receivers to be connected to a multipoint bus transmission line. The **SP431** features a driver enable control common to all four drivers and a tri-state output. Since the cabling can be as long as 4,000 feet, the RS-422 drivers of the **SP431** are equipped with a wide common-mode output voltage range to accommodate ground potential differences.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

$V_{CC}$ .....	0.5V to 7.0V
$V_{IN}$ (DC Input Voltage).....	-1.5V to ( $V_{CC}$ + 1.5V)
$V_{OUT}$ (DC Output Voltage).....	-0.5V to 7V
$I_{IK}, I_{OK}$ (Clamp Diode Current).....	$\pm 20\text{mA}$
$I_{OUT}$ (DC Output Current, per pin).....	$\pm 150\text{mA}$
$I_{CC}$ (DC $V_{CC}$ or GND Current, per pin).....	$\pm 150\text{mA}$
$T_{STG}$ (Storage Temperature Range).....	-65°C to +150°C
Storage Temperature.....	-65°C to +150°C
<b>Power Dissipation Per Package</b>	
16-pin PDIP (derate 14.3mW/°C above +70°C).....	1150mW
16-pin NSOIC (derate 13.6mW/°C above +70°C).....	1100mW

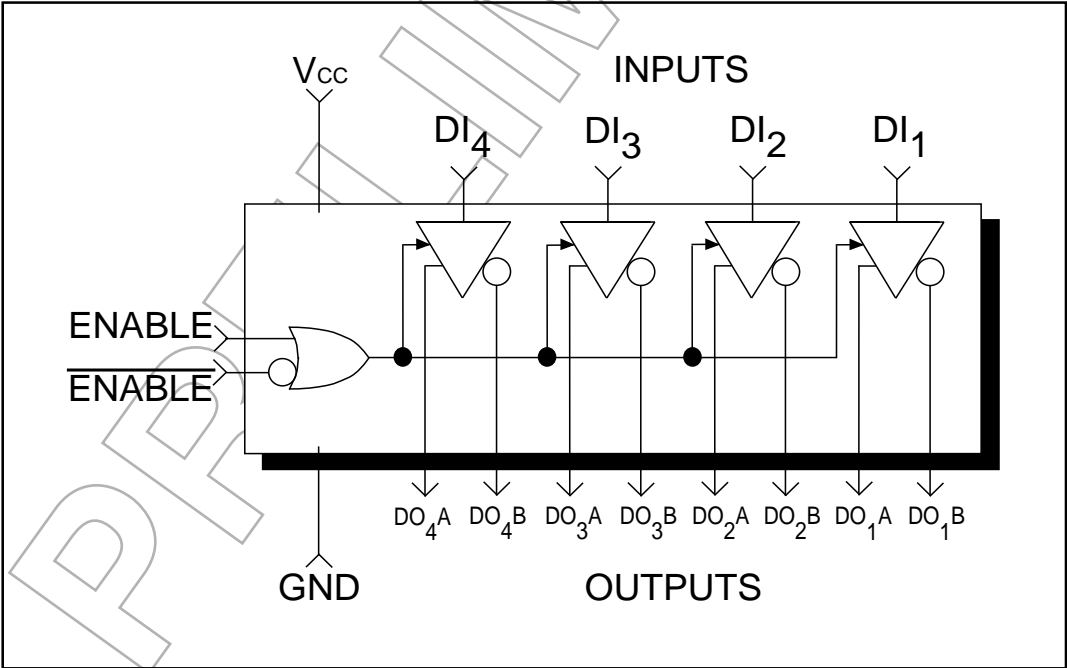
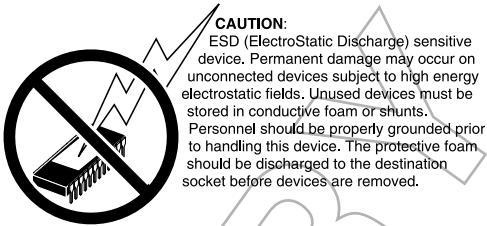


Figure 1. SP431 Block Diagram

## SPECIFICATIONS

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0V$  to  $+3.6V$  with  $T_{amb} = 25^{\circ}C$  and all MIN and MAX limits apply across the recommended operating temperature range.

DC PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Supply Voltage, $V_{CC}$	3.0		3.6	V	
DC Input or Output Voltage, $V_{IN}$ or $V_{OUT}$			$V_{CC}$	V	
<b>Input Electrical Characteristics</b>					
Input Rise or Fall Times, $t_r$ or $t_f$		3		ns	
HIGH Level Input Voltage, $V_{IH}$	2.0			V	
LOW Level Input Voltage, $V_{IL}$			0.8	V	
<b>Output Electrical Characteristics</b>					
HIGH Level Output Voltage, $V_{OH}$	2.5	2.9		V	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OUT} = -20mA$
LOW Level Output Voltage, $V_{OL}$		0.2	0.5	V	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OUT} = 20mA$
Differential Output Voltage, $V_T$	2.0	2.7		V	$R_L = 100\Omega$ , Note 1
Difference in Differential Output, $ V_{T1}  -  V_{T2} $			0.4	V	$R_L = 100\Omega$ , Note 1
Common Mode Output Voltage, $V_{OS}$			3.0	V	$R_L = 100\Omega$ , Note 1
Difference in Common Mode Output, $ V_{OS1} - V_{OS2} $			0.4	V	$R_L = 100\Omega$ , Note 1
Quiescent Supply Current					
$I_{CC}$			100	$\mu A$	$V_{IN} = V_{CC}$ or GND, Note 2
Tri-state Output Leakage Current, $I_{OZ}$		$\pm 2.0$		$\mu A$	$V_{OUT} = V_{CC}$ or GND, ENABLE = $V_{IL}$ , ENABLE = $V_{IH}$
Output Short Circuit Current, $I_{SC}$	-30		-150	mA	$V_{IN} = V_{CC}$ or GND, Notes 1 and 3
Output Leakage Current Power Off					
$I_{OFF}$			100	$\mu A$	$V_{CC} = 0V$ , $V_{OUT} = 6V$ , Note 1
$I_{OFF}$			-100	$\mu A$	$V_{CC} = 0V$ , $V_{OUT} = -0.25V$ , Note 1

**NOTE 1:** Refer to EIA specifications for RS-422 serial protocol for exact test conditions.

**NOTE 2:** Measured per input. All other inputs at  $V_{CC}$  or GND.

**NOTE 3:** This is the current sourced when a high output is shorted to GND. Only one output at a time should be shorted.

## SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0V$  to  $+3.6V$ ,  $T_{amb} = 25^{\circ}C$ ,  $t_r \leq 6ns$ ,  $t_f \leq 6ns$ , and all MIN and MAX limits apply across the recommended operating temperature range.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>SWITCHING CHARACTERISTICS</b>					
Propagation Delays, $t_{PLHD}$ , $t_{PHLD}$		5		ns	Figure 3
Skew		0.5		ns	Figure 3, Note 4
Differential Output Rise and Fall Times, $t_{TLH}$ , $t_{PHL}$		3		ns	Figure 3
Output Enable Time, $t_{PZH}$		13		ns	Figure 5
Output Enable Time, $t_{PZL}$		8		ns	Figure 5
Output Disable Time, $t_{PHZ}$		8		ns	Figure 5, Note 5
Output Disable Time, $t_{PLZ}$		6		ns	Figure 5, Note 5
Power dissipation Capacitance, $C_{PD}$		50		pF	Note 6
Input Capacitance, $C_{IN}$		6		pF	

**NOTE 4:** Skew is defined as the difference in propagation delays between complementary outputs at the 50% input.

**NOTE 5:** Output disable time is the delay from ENABLE or ~~ENABLE~~ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

**NOTE 6:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = (C_{PD} V_{CC}^2 f) + (I_{CC} V_{CC})$ , and the no load dynamic current consumption,  $I_S = (C_{PD} V_{CC} f) + I_{CC}$ .

## AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS

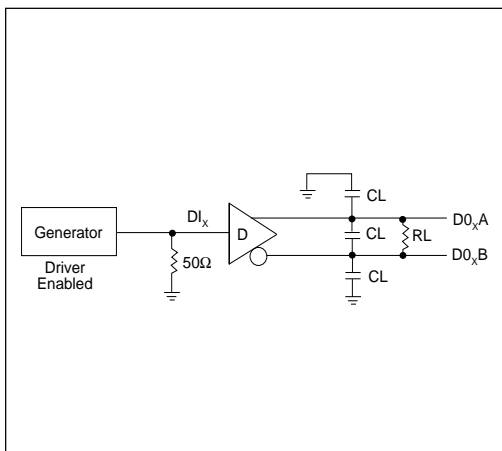


Figure 2. AC Test Circuit

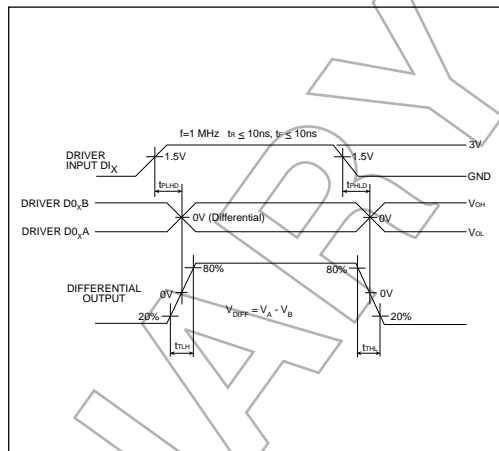


Figure 3. Propagation Delays

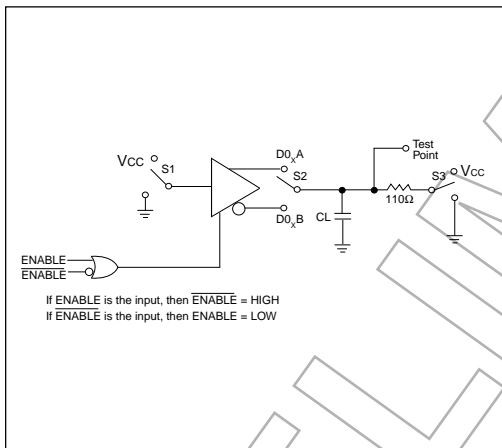


Figure 4. Driver Single-Ended TRI-STATE Test Circuit

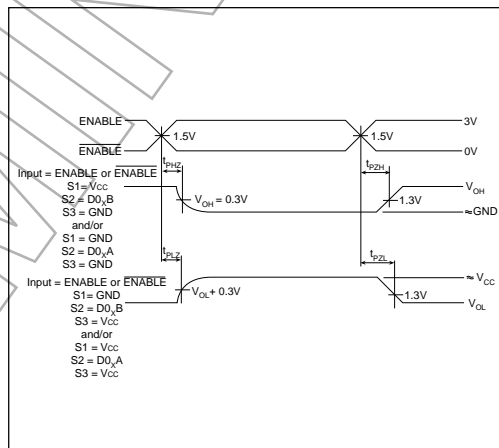


Figure 5. Driver Single-Ended TRI-STATE Waveforms

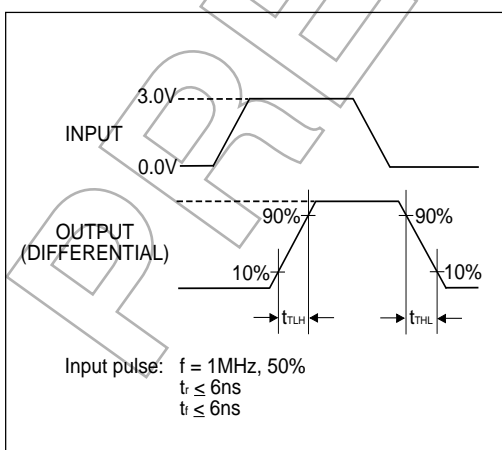


Figure 6. Differential Rise and Fall Times

### DESCRIPTION

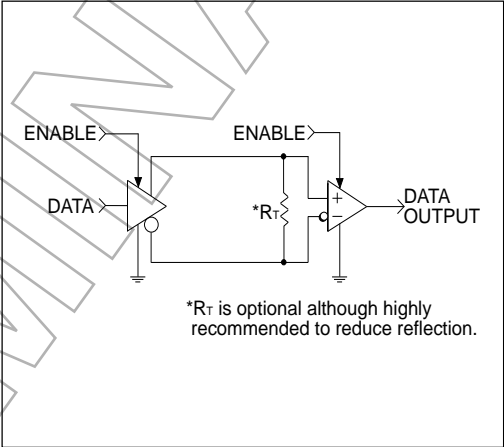
The **SP431** is a low-power quad differential line driver designed for digital data transmission meeting the specifications of the EIA standard RS-422 serial protocol. The **SP431** features Sipex's BiCMOS process allowing low power operational characteristics of CMOS technology while meeting all of the demands of the RS-422 serial protocol up to 60Mbps under load in harsh environments.

The RS-422 standard is ideal for multi-drop applications and for long-distance communication. The RS-422 protocol allows up to 10 drivers to be connected to a data bus, making it an ideal choice for multi-drop applications. Since the cabling can be as long as 4,000 feet, RS-422 drivers are equipped with a wide common mode output range to accommodate ground potential differences. Because the RS-422 is a differential interface, data is virtually immune to noise in the transmission line.

The **SP431** accepts TTL or CMOS input levels and translates these to RS-422 output levels. The **SP431** features active HIGH and active LOW driver enable controls common to all four driver channels see *Figure 8*. A logic HIGH on the **ENABLE** pin (pin 4) or a logic LOW on the **ENABLE** pin (pin 12) will enable the differential driver outputs. A logic LOW on the **ENABLE** pin (pin 4) or a logic HIGH on the **ENABLE** pin (pin 12) will tri-state the driver outputs.

The RS-422 line driver outputs feature high source and sink current capability. All drivers are internally protected against short circuits on their outputs. The driver outputs are short-circuit limited to 150mA. The driver output skew times are typically 0.5ns.

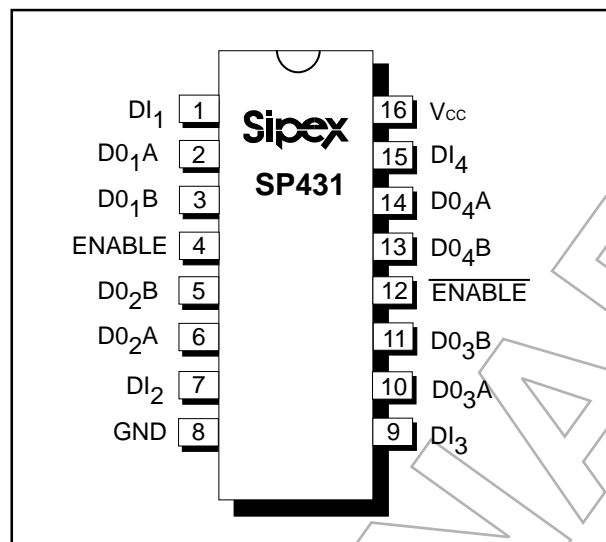
To minimize reflections, the multipoint bus transmission line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.



*Figure 7. Two-Wire Balanced System, RS-422*

ENABLE	$\overline{\text{ENABLE}}$	Input	Non-Inverting Output	Inverting Output
LOW	HIGH	don't care	tri-state	tri-state
HIGH	don't care	LOW	LOW	HIGH
don't care	LOW	HIGH	HIGH	LOW

*Figure 8. Truth Table, Enable / Disable Function Common to All Four RS-422 Drivers*



**PINOUT**

## PIN ASSIGNMENTS

- |   |  |
|---|--|
| Pin 1 — $DI_1$ — Driver 1 TTL input.                  | Pin 10 — $D0_3A$ — Non-inverted driver output.                   |
| Pin 2 — $D0_1A$ — Non-inverted driver output.         | Pin 11 — $D0_3B$ — Inverted driver output.                       |
| Pin 3 — $D0_1B$ — Inverted driver output.             | Pin 12 — $\overline{ENABLE}$ — Driver output enable, active LOW. |
| Pin 4 — $ENABLE$ — Driver output enable, active HIGH. | Pin 13 — $D0_4B$ — Inverted driver output.                       |
| Pin 5 — $D0_2B$ — Inverted driver output.             | Pin 14 — $D0_4A$ — Non-inverted driver output.                   |
| Pin 6 — $D0_2A$ — Non-inverted driver output.         | Pin 15 — $DI_4$ — Driver 4 TTL input.                            |
| Pin 7 — $DI_2$ — Driver 2 TTL input.                  | Pin 16 — $V_{CC}$ — +3.0V to +3.6V power supply.                 |
| Pin 8 — $GND$ — Ground.                               |  |
| Pin 9 — $DI_3$ — Driver 3 TTL input.                  |  |

TYPICAL PERFORMANCE CHARACTERISTICS

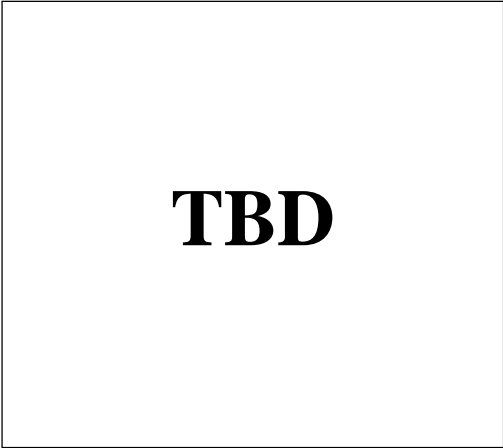


Figure 9. Differential Propagation Delay Vs. Temperature

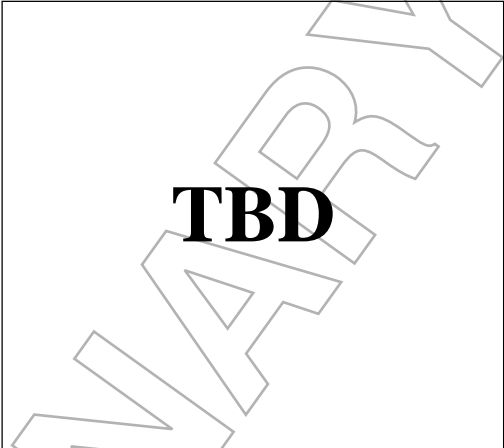


Figure 10. Differential Propagation Delay Vs. Temperature

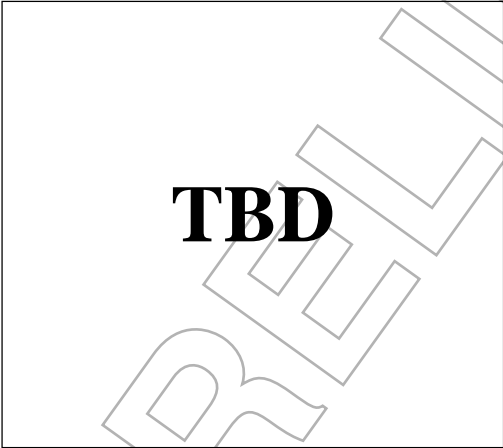


Figure 11. Differential Skew Vs. Temperature

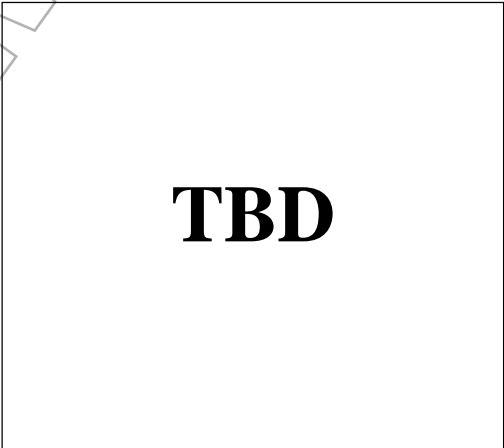


Figure 12. Differential Skew Vs. Power Supply Voltage



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

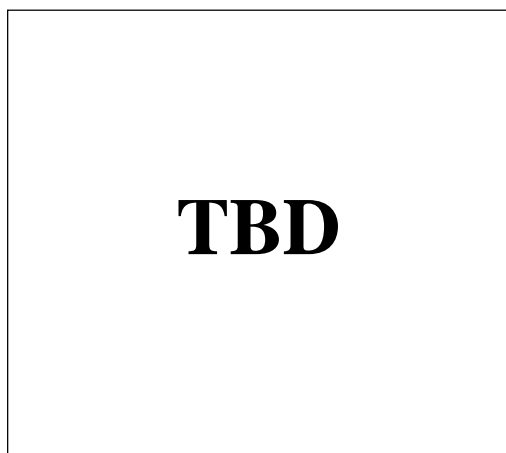


Figure 13. Differential Transition Time Vs. Temperature

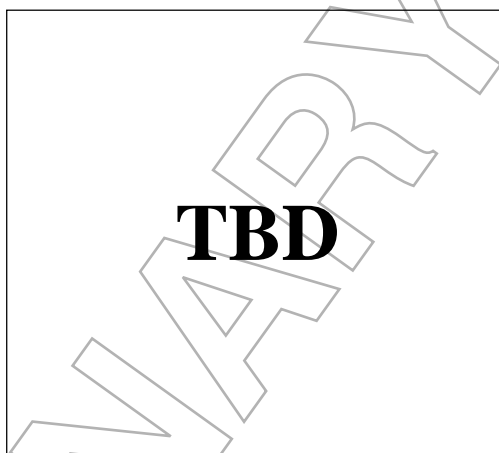


Figure 14. Differential Transition Time Vs. Power Supply Voltage

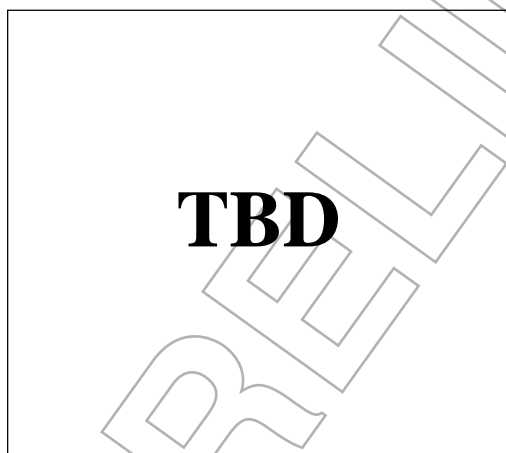


Figure 15. Complementary Skew Vs. Temperature

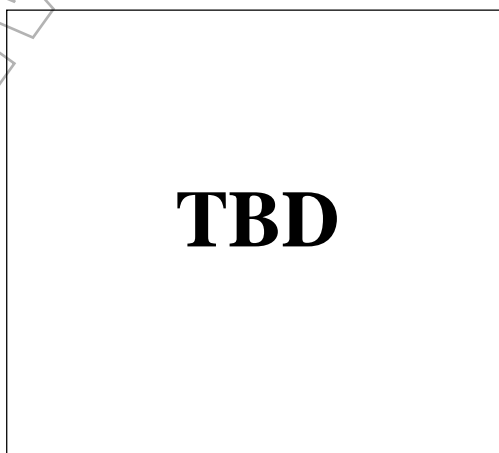


Figure 16. Complementary Skew Vs. Power Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

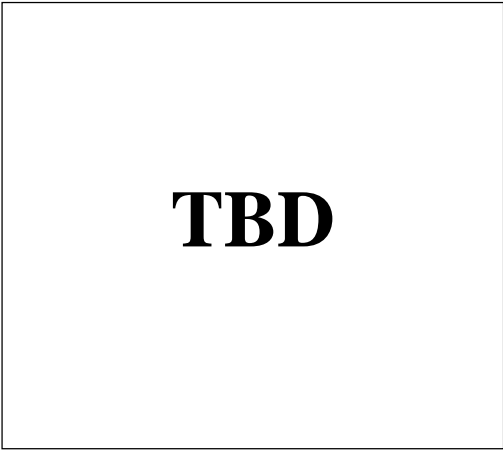


Figure 17. Differential Output Voltage Vs. Output Current

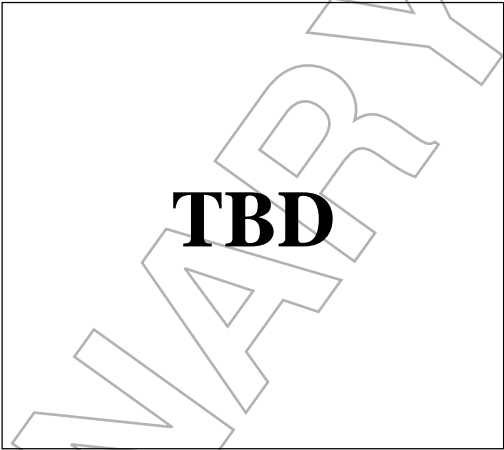


Figure 18. Differential Output Voltage Vs. Output Current

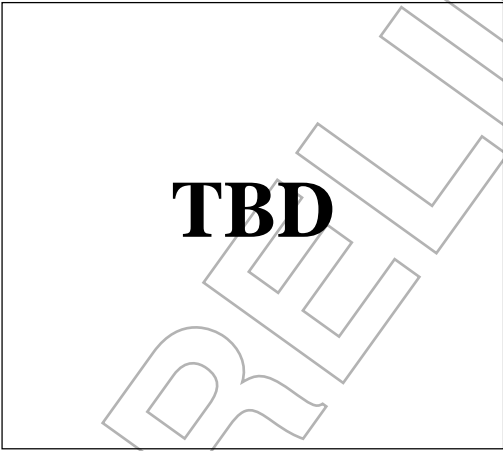


Figure 19. Output High Voltage Vs. Output High Current

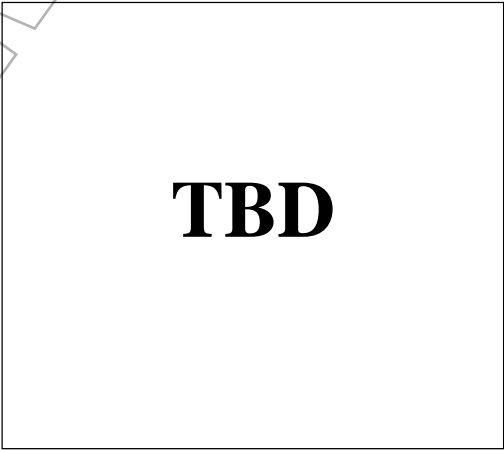


Figure 20. Output High Voltage Vs. Output High Current

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

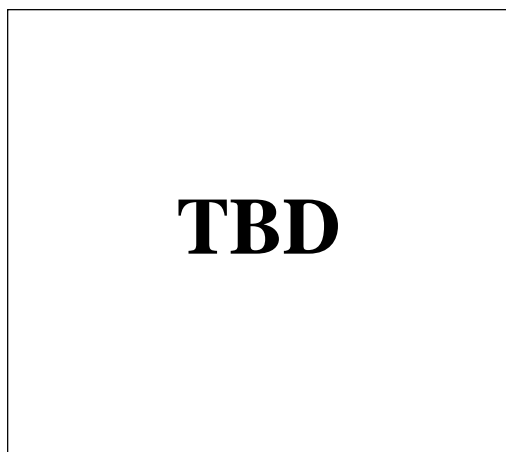


Figure 21. Output Low Voltage Vs. Output Low Current

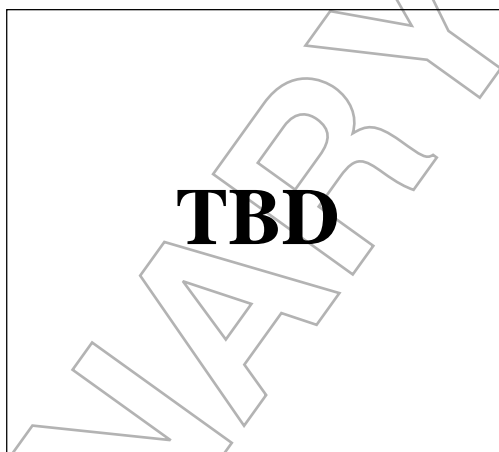


Figure 22. Output Low Voltage Vs. Output Low Current

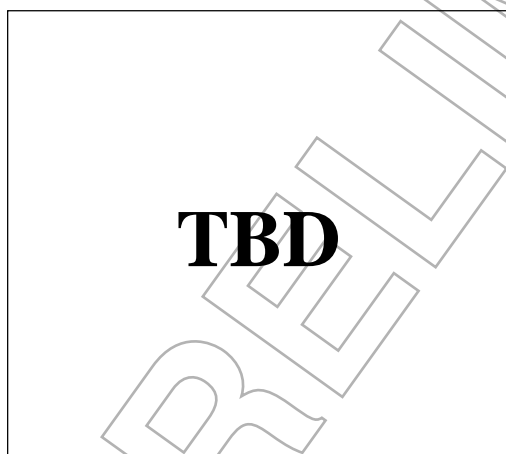


Figure 23. Supply Current Vs. Temperature

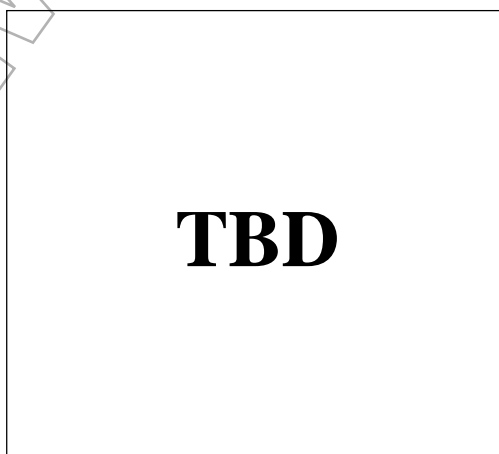


Figure 24. Supply Current Vs. Power Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

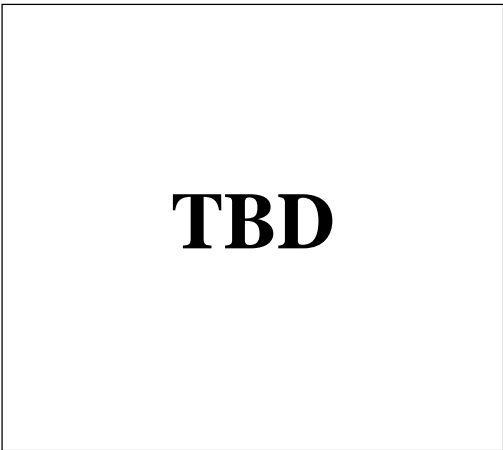


Figure 25. No Load Supply Current Vs. Data Rate

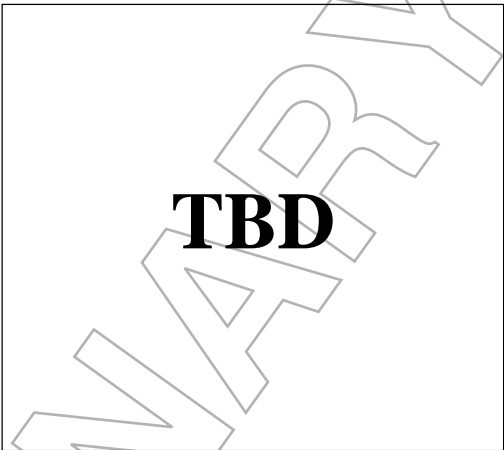


Figure 26. Loaded Supply Current Vs. Data Rate

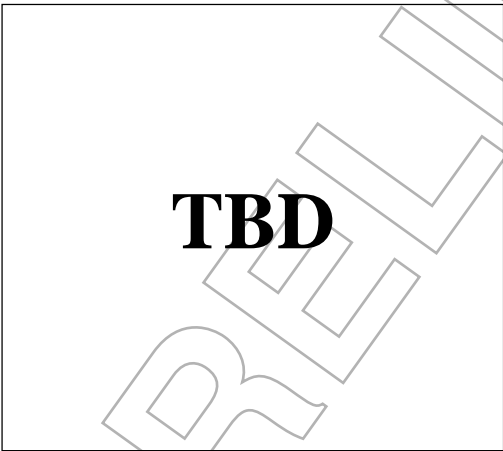


Figure 27. Output Short Circuit Current Vs. Temperature

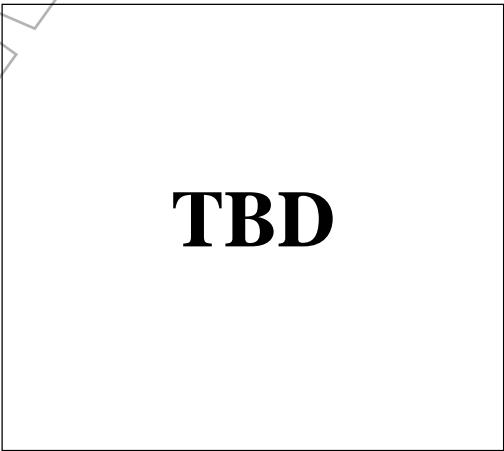
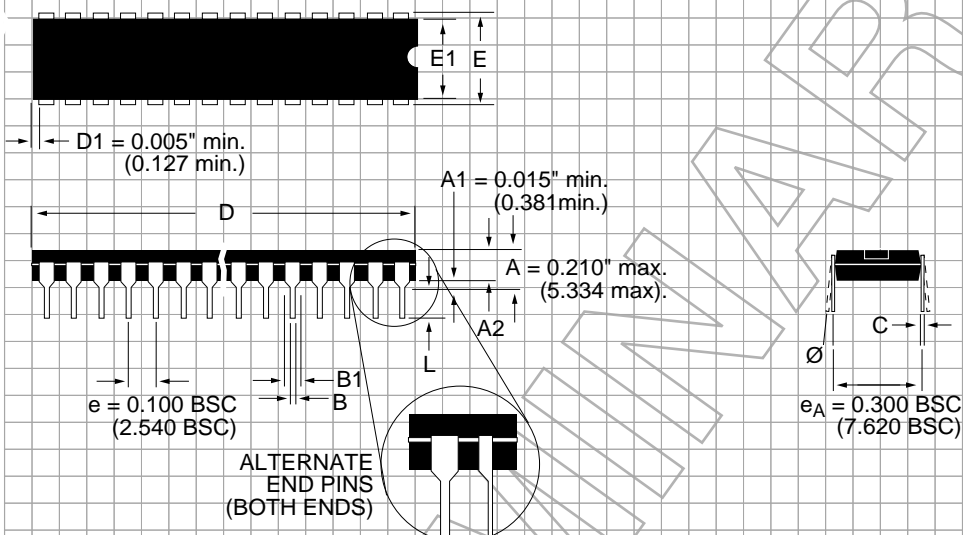


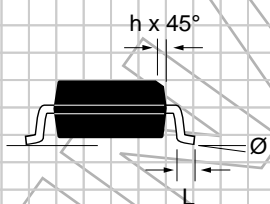
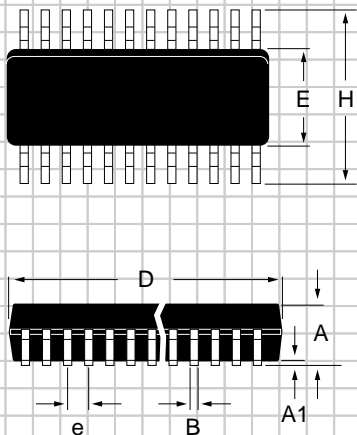
Figure 28. Output Short Circuit Current Vs. Power Supply Voltage

**PACKAGE: PLASTIC  
DUAL-IN-LINE  
(NARROW)**



DIMENSIONS (Inches)	
Minimum/Maximum (mm)	16-PIN
A2	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)
D	0.780/0.800 (19.812/20.320)
E	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)
$\emptyset$	0°/15° (0°/15°)

**PACKAGE: PLASTIC  
SMALL OUTLINE (SOIC)  
(NARROW)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	16-PIN
A	0.053/0.069 (1.346/1.748)
A1	0.004/0.010 (0.102/0.249)
B	0.013/0.020 (0.330/0.508)
D	0.386/0.394 (9.802/10.000)
E	0.150/0.157 (3.802/3.988)
e	0.050 BSC (1.270 BSC)
H	0.228/0.244 (5.801/6.198)
h	0.010/0.020 (0.254/0.498)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

## ORDERING INFORMATION

Model .....	Temperature Range .....	Package .....
SP431CP .....	0°C to +70°C .....	16-pin Plastic DIP .....
SP431CN .....	0°C to +70°C .....	16-pin Narrow SOIC .....

Please consult the factory for pricing and availability on a Tape-On-Reel option.



SIGNAL PROCESSING EXCELLENCE

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