

International  
**IR** Rectifier

**PRELIMINARY**

Data Sheet No. PD60247revD

# IRS2136D/IRS21362D/IRS21363D/IRS21365D/ IRS21366D/IRS21367D/IRS21368D (J&S) PBF

## 3-PHASE BRIDGE DRIVER

### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V (IRS2136D/IRS21368D), 11.5 V to 20 V (IRS21362D), or 12 V to 20 V (IRS21363D/IRS21365D/IRS21366D/IRS21367D)
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Cross-conduction prevention logic
- Integrated bootstrap diode function
- Low side output out of phase with inputs. High side outputs out of phase (IRS213(6,63, 65, 66, 67, 68)D), or in phase (IRS21362D) with inputs
- 3.3 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Externally programmable delay for automatic fault clear
- All parts are LEAD-FREE

### Packages



### Applications:

- \*Motor Control
- \*Air Conditioners/ Washing Machines
- \*General Purpose Inverters
- \*Micro/Mini Inverter Drives

### Description

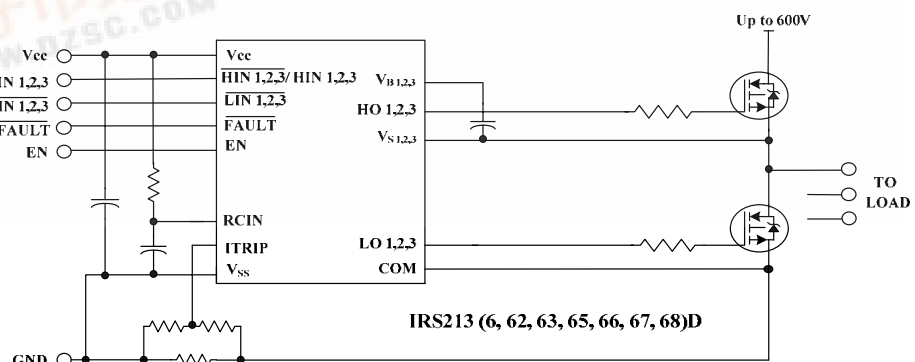
The IRS2136xD (J&S) are high voltage, high speed power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V.

### Feature Comparison: IRS2136xD

Part	IRS2136D	IRS21362D	IRS21363D	IRS21365D	IRS21366D	IRS21367D	IRS21368D
Input Logic	HIN, LIN	HIN, LIN	HIN, LIN	HIN, LIN	HIN, LIN	HIN, LIN	HIN, LIN
$t_{on}$ (typ.)	530 ns	530 ns	530 ns	530 ns	200 ns	200 ns	530 ns
$t_{off}$ (typ.)	530 ns	530 ns	530 ns	530 ns	200 ns	200 ns	530 ns
$V_{IH}$ (min.)	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V
$V_{IL}$ (max.)	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V
$V_{ITRIP+}$	0.46 V	0.46 V	0.46 V	4.3 V	0.46 V	4.3 V	4.3 V
$V_{COV+}/V_{BSUV+}$	8.9 V	10.4 V	11.1 V	11.1 V	11.1 V	11.1 V	8.9 V
$V_{COV-}/V_{BSUV-}$	8.2 V	9.4 V	10.9 V	10.9 V	10.9 V	10.9 V	8.2 V

### Typical Connection

(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.



## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage

Symbol	Definition		Min.	Max.	Units
V <sub>S</sub>	High side offset voltage		V <sub>B 1,2,3</sub> - 20	V <sub>B 1,2,3</sub> + 0.3	V
V <sub>B</sub>	High side floating supply voltage		-0.3	620	
V <sub>HO1,2,3</sub>	High side floating output voltage		V <sub>S1,2,3</sub> - 0.3	V <sub>B 1,2,3</sub> + 0.3	
V <sub>CC</sub>	Low side and logic fixed supply voltage		-0.3	20	
V <sub>SS</sub>	Logic ground		V <sub>CC</sub> - 20	V <sub>CC</sub> + 0.3	
V <sub>LO1,2,3</sub>	Low side output voltage		-0.3	V <sub>CC</sub> + 0.3	
V <sub>IN</sub>	Input voltage LIN, HIN, ITRIP, EN, RCIN		V <sub>SS</sub> -0.3	V <sub>CC</sub> + 0.3	
V <sub>FLT</sub>	FAULT output voltage		V <sub>SS</sub> -0.3	V <sub>CC</sub> + 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25 °C	(28 lead PDIP)	—	1.5	W
		(28 lead SOIC)	—	1.6	
		(44 lead PLCC)	—	2.0	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(28 lead PDIP)	—	83	°C/W
		(28 lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T <sub>J</sub>	Junction temperature		—	150	°C
T <sub>S</sub>	Storage temperature		-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)		—	300	

parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

## Recommended Operating Conditions

The input/output logic-timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The  $V_S$  &  $V_{SS}$  offset ratings are tested with all supplies biased at a 15 V differential.

With all supplies biased at a 10 V differential.					
Symbol	Definition		Min.	Max.	Units
V <sub>B1,2,3</sub>	High side floating supply voltage	IRS213(6,68)D	V <sub>S1,2,3</sub> +10	V <sub>S1,2,3</sub> + 20	V
		IRS21362D	V <sub>S1,2,3</sub> +11.5	V <sub>S1,2,3</sub> + 20	
		IRS213(6,63,65,66,67)D	V <sub>S1,2,3</sub> +12	V <sub>S1,2,3</sub> + 20	
V <sub>S 1,2,3</sub>	High side floating supply voltage		Note 1	600	
V <sub>CC</sub>	Low side supply voltage	IRS213(6,68)D	10	20	
		IRS21362D	11.5	20	
		IRS213(6,63,65,66,67)D	12	20	
V <sub>HO 1,2,3</sub>	High side output voltage		V <sub>S1,2,3</sub>	V <sub>B1,2,3</sub>	
V <sub>LO1,2,3</sub>	Low side output voltage		0	V <sub>CC</sub>	
V <sub>SS</sub>	Logic ground		-5	5	
V <sub>FLT</sub>	FAULT output voltage		V <sub>SS</sub>	V <sub>CC</sub>	
V <sub>RCIN</sub>	RCIN input voltage		V <sub>SS</sub>	V <sub>CC</sub>	

**Note 1:** Logic operational for  $V_S$  of (COM - 8 V) to (COM + 600 V). Logic state held for  $V_S$  of (COM - 8 V) to (COM -  $V_{BS}$ ). (Please refer to the Design Tip DT97-3 for more details).

## Recommended Operating Conditions - (Continued)

The input/output logic-timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The  $V_S$  &  $V_{SS}$  offset ratings are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
$V_{ITRIP}$	ITRIP input voltage	$V_{SS}$	$V_{SS} + 5$	V
$V_{IN}$	Logic input voltage LIN, HIN (IRS213(6,63,65,66,67,68)D), LIN, HIN (IRS21362D), EN	$V_{SS}$	$V_{SS} + 5$	
$T_A$	Ambient temperature	-40	125	°C

**Note 1:** HIN, LIN, EN and the ITRIP pin are internally clamped with a 5.2 V zener diode.

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS1,2,3}$ ) = 15 V unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all six channels (HIN1,2,3/HIN1,2,3 and LIN1,2,3). The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_{S1,2,3}$  and are applicable to the respective output leads: LO1,2,3 and HO1,2,3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "0" input voltage LIN1,2,3, HIN1,2,3 IRS213(6,63,65)D	2.5	—	—	V	
	Logic "1" input voltage HIN1,2,3 IRS21362D	2.5	—	—		
$V_{IL}$	Logic "0" input voltage LIN1,2,3, HIN1,2,3 IRS213(66,67,68)D	—	—	0.8		
	Logic "1" input voltage LIN1,2,3, HIN1,2,3 IRS213(6,63,65)D	—	—	0.8		
$V_{IN,TH+}$	Input positive going threshold	—	1.9	—		
$V_{IN,TH-}$	Input negative going threshold	—	1	—		
$V_{EN,TH+}$	Enable positive going threshold	—	—	2.5		
$V_{EN,TH-}$	Enable negative going threshold	0.8	—	—		
$V_{IT,TH+}$ (6,62,63,66)	ITRIP positive going threshold	0.37	0.46	0.55		
$V_{IT,HYS}$ (6,62,63,66)	ITRIP hysteresis	—	0.07	—		
$V_{IT,TH+}$ (65,67,68)	ITRIP positive going threshold	3.85	4.3	4.75		
$V_{IT,HYS}$ (65,67,68)	ITRIP hysteresis	—	0.15	—		
$V_{RCIN,TH+}$	RCIN positive going threshold	—	8	—		
$V_{RCIN,HYS}$	RCIN hysteresis	—	3	—		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	0.9	1.4		Io = 20 mA
$V_{OL}$	Low level output voltage, $V_O$	—	0.4	0.6		
$V_{CCUV+}$ (6,68)	$V_{CC}$ supply undervoltage positive going threshold	8	8.9	9.8		
$V_{CCUV-}$ (6,68)	$V_{CC}$ supply undervoltage negative going threshold	7.4	8.2	9		
$V_{CCUVHY}$ (6,68)	$V_{CC}$ supply undervoltage hysteresis	0.3	0.7	—		
$V_{BSUV+}$ (6,68)	$V_{BS}$ supply undervoltage positive going threshold	8	8.9	9.8		

### Static Electrical Characteristics - (Continued)

$V_{BIAS}$  ( $V_{CC}, V_{BS1,2,3}$ ) = 15 V unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all six channels (HIN1,2,3/ HIN1,2,3 and LIN1,2,3). The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_{S1,2,3}$  and are applicable to the respective output leads: LO1,2,3 and HO1,2,3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{BSUV-}$ (6,68)	$V_{BS}$ supply undervoltage negative going threshold	7.4	8.2	9	V	
$V_{BSUVHY}$ (6,68)	$V_{BS}$ supply undervoltage hysteresis	0.3	0.7	—		
$V_{CCUV+}$ (62)	$V_{CC}$ supply undervoltage positive going threshold	9.6	10.4	11.2		
$V_{CCUV-}$ (62)	$V_{CC}$ supply undervoltage negative going threshold	8.6	9.4	10.2		
$V_{CCUVHY}$ (62)	$V_{CC}$ supply undervoltage hysteresis	0.5	1	—		
$V_{BSUV+}$ (62)	$V_{BS}$ supply undervoltage positive going threshold	9.6	10.4	11.2		
$V_{BSUV-}$ (62)	$V_{BS}$ supply undervoltage negative going threshold	8.6	9.4	10.2		
$V_{BSUVHY}$ (62)	$V_{BS}$ supply undervoltage hysteresis	0.5	1	—		
$V_{CCUV+}$ (63,65,66,67)	$V_{CC}$ supply undervoltage positive going threshold	10.4	11.1	11.6		
$V_{CCUV-}$ (63,65,66,67)	$V_{CC}$ supply undervoltage negative going threshold	10.2	10.9	11.4		
$V_{CCUVHY}$ (63,65,66,67)	$V_{CC}$ supply undervoltage hysteresis	—	0.2	—		
$V_{BSUV+}$ (63,65,66,67)	$V_{BS}$ supply undervoltage positive going threshold	10.4	11.1	11.6		
$V_{BSUV-}$ (63,65,66,67)	$V_{BS}$ supply undervoltage negative going threshold	10.2	10.9	11.4		
$V_{BSUVHY}$ (63,65,66,67)	$V_{BS}$ supply undervoltage hysteresis	—	0.2	—		
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu A$	$V_B = V_S = 600 V$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	70	120		all inputs @ logic 0 value
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	3	4		
$V_{IN,CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	4.8	5.2	5.65	V	$I_{IN} = 100 \mu A$
$I_{LIN+}$ (6,62,63,65)	Input bias current (LOUT = HI)	—	110	150	$\mu A$	$V_{IN} = 4 V$
$I_{LIN-}$ (6,62,63,65)	Input bias current (LOUT = LO)	—	150	200		$V_{IN} = 0 V$
$I_{LIN+}$ (66,67,68)	Input bias current (LOUT = HI)	—	—	3		$V_{IN} = 4 V$
$I_{LIN-}$ (66,67,68)	Input bias current (LOUT = LO)	—	—	3		$V_{IN} = 0 V$
$I_{HIN+}$ (6,63,65)	Input bias current (HOUT = HI)	—	110	150		$V_{IN} = 4 V$
$I_{HIN-}$ (6,63,65)	Input bias current (HOUT = LO)	—	150	200		$V_{IN} = 0 V$
$I_{HIN+}$ (62)	Input bias current (HOUT = HI)	—	5	20		$V_{IN} = 4 V$
$I_{HIN-}$ (62)	Input bias current (HOUT = LO)	—	—	3		$V_{IN} = 0 V$
$I_{HIN+}$ (66,67,68)	Input bias current (HOUT = HI)	—	—	3		$V_{IN} = 4 V$
$I_{HIN-}$ (66,67,68)	Input bias current (HOUT = LO)	—	—	3		$V_{IN} = 0 V$
$I_{ITRIP+}$	“High” ITRIP input bias current	—	5	40		$V_{IN} = 4 V$
$I_{ITRIP-}$	“Low” ITRIP input bias current	—	—	1		$V_{IN} = 0 V$
$I_{EN+}$	“High” ENABLE input bias current	—	5	40		$V_{IN} = 4 V$
$I_{EN-}$	“Low” ENABLE input bias current	—	—	1		$V_{IN} = 0 V$

## Static Electrical Characteristics - (Continued)

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS1,2,3}$ ) = 15 V unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all six channels (HIN1,2,3/HIN1,2,3 and LIN1,2,3). The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_{S1,2,3}$  and are applicable to the respective output leads: LO1,2,3 and HO1,2,3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$I_{RCIN}$	RCIN input bias current	—	—	1	$\mu A$	$V_{RCIN} = 0 V$ or 15 V
$I_{O+}$	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0 V$ , $PW \leq 10 \mu s$
$I_{O-}$	Output low short circuit pulsed current	250	350	—		$V_O = 15 V$ , $PW \leq 10 \mu s$
$R_{on\_RCIN}$	RCIN low on resistance	—	50	100	$\Omega$	$I = 1.5 mA$
$R_{on\_FAULT}$	FAULT low on resistance	—	50	100		
$R_{BS}$	Internal BS diode $R_{ON}$	—	200	—		

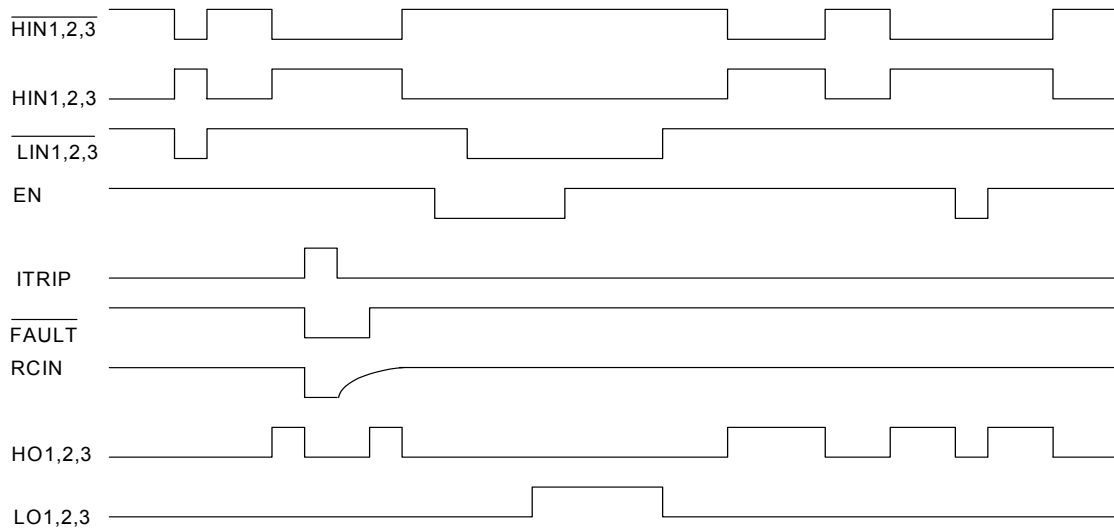
**Note 1:** Please refer to Feature Description section for integrated bootstrap functionality information.

## Dynamic Electrical Characteristics

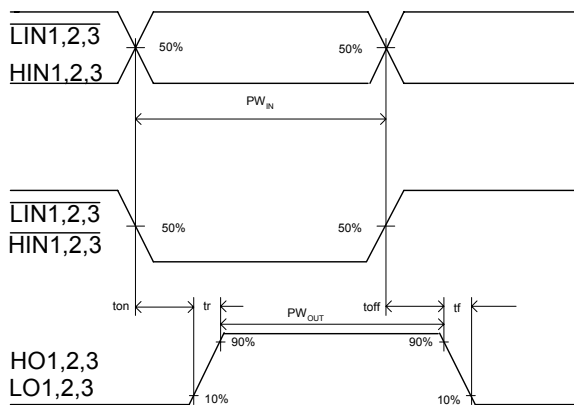
Dynamic Electrical Characteristics  $V_{CC} = V_{BS} = V_{BIAS} = 15 V$ ,  $V_{S1,2,3} = V_{SS} = COM$ ,  $T_A = 25^\circ C$  and  $CL = 1000 pF$  unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	400	530	750	ns	$V_{IN} = 0 V$ & 5 V
$t_{off}$	Turn-off propagation delay	400	530	750		
$t_{on}(66,67)$	Turn-on propagation delay	—	200	—		
$t_{off}(66,67)$	Turn-off propagation delay	—	200	—		
$t_r$	Turn-on rise time	—	125	190		
$t_f$	Turn-off fall time	—	50	75		
$t_{EN}$	ENABLE low to output shutdown propagation delay	350	460	650		$V_{IN}, V_{EN} = 0 V$ or 5 V
$t_{EN}(66,67)$	ENABLE low to output shutdown propagation delay	—	300	—		
$t_{ITRIP}$	ITRIP to output shutdown propagation delay	500	750	1200		$V_{ITRIP} = 5 V$
$t_{bl}$	ITRIP blanking time	—	400	—		$V_{IN} = 0 V$ or 5 V $V_{ITRIP} = 5 V$
$t_{FLT}$	ITRIP to FAULT propagation delay	400	600	950		$V_{IN} = 0 V$ & 5 V
$t_{FILIN}$	Input filter time (HIN, LIN) (IRS213(6,62,63,65,68)D only)	200	350	510		
$t_{filterEN}$	Enable input filter time (IRS213(6,62,63,65,68)D only)	100	200	—		
DT	Deadtime	190	290	420		$V_{IN} = 0 V$ & 5 V external dead time
MT	$t_{on}, t_{off}$ matching time (on all six channels)	—	—	50		External dead time >420 ns
MDT	DT matching (Hi->Lo & Lo->Hi on all channels)	—	—	60		External dead time 0 s
PM	Pulse width distortion (pwin-pwout)	—	—	75		PW input=10 $\mu s$
$t_{FLTCLR}$	FAULT clear time RCIN: R = 2 M $\Omega$ , C = 1 nF	1.3	1.65	2	ms	$V_{IN} = 0 V$ or 5 V $V_{ITRIP} = 0 V$

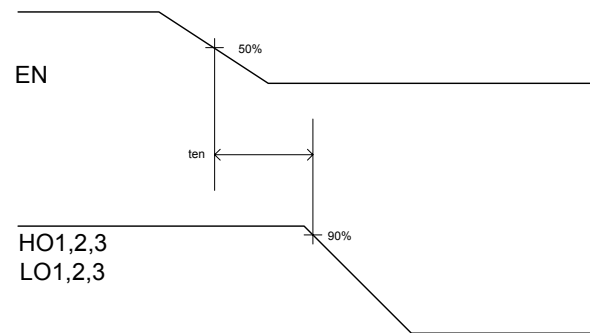
**Note 2:** For high side PWM, HIN pulse width must be  $\geq 500$  ns.



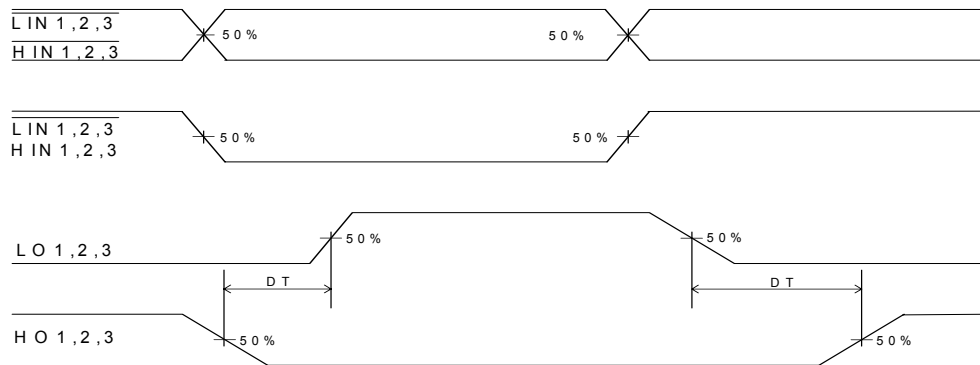
**Fig. 1. Input/Output Timing Diagram**



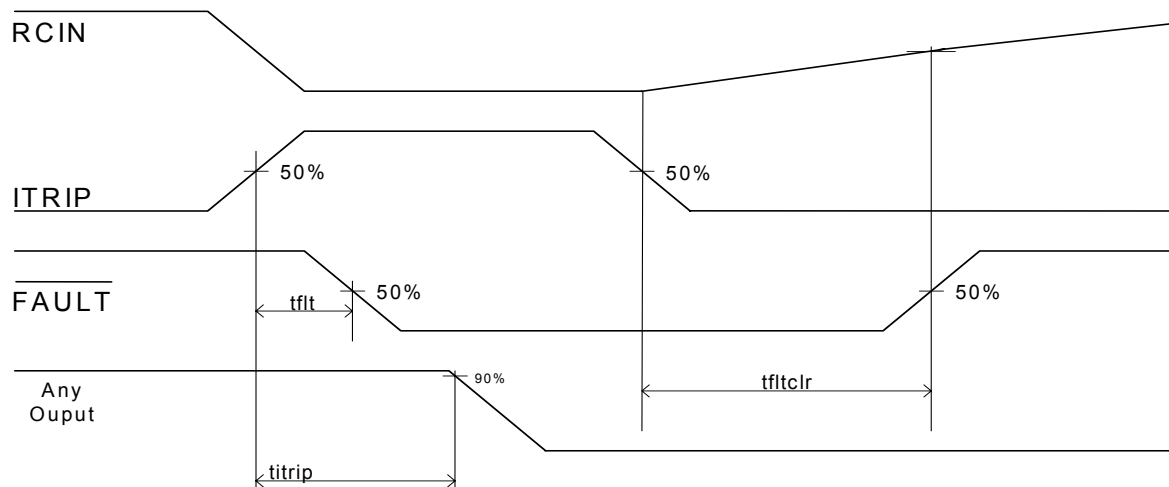
**Fig. 2. Switching Time Waveforms**



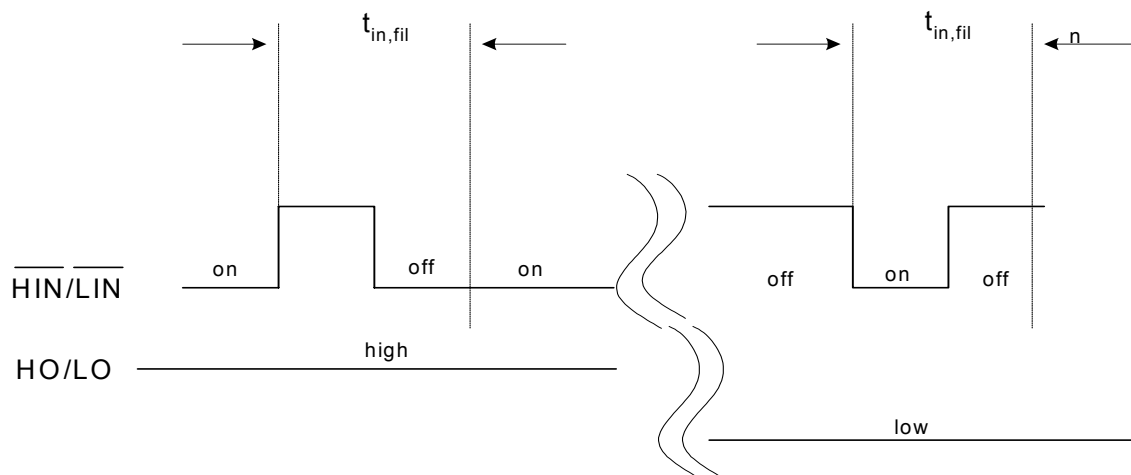
**Fig. 3. Output Enable Timing Waveform**



**Fig. 4. Internal Deadtime Timing Waveforms**



**Fig. 5. ITRIP/RCIN Timing Waveforms**



**Fig. 6. Input Filter Function**


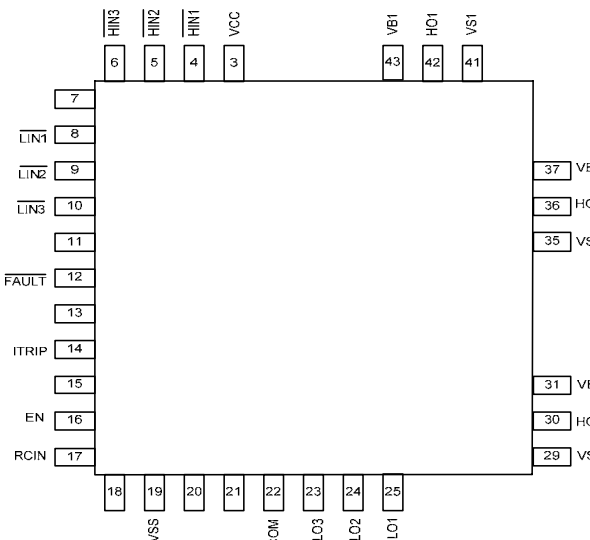

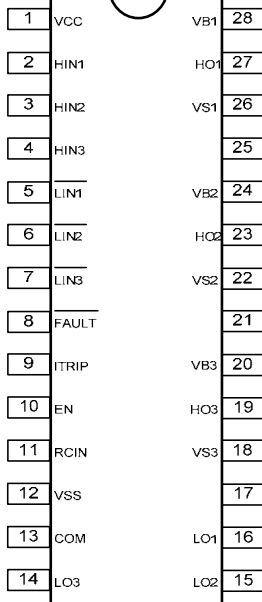
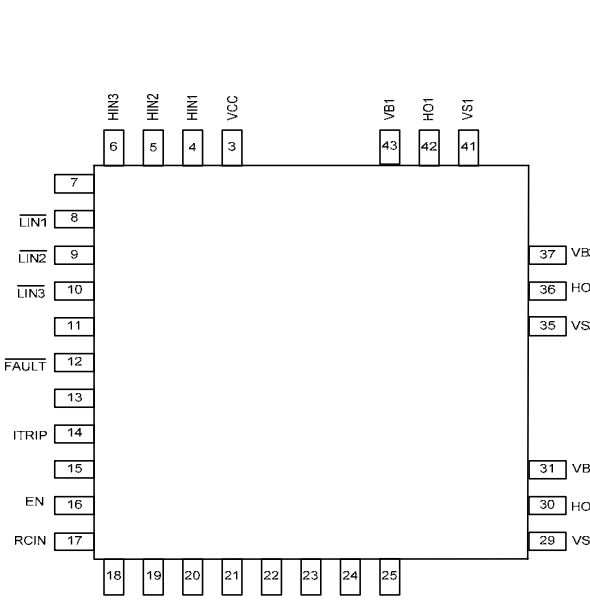
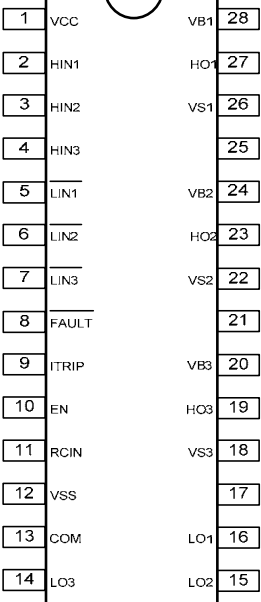
## Lead Definitions

Symbol	Description
<b>V<sub>CC</sub></b>	Low side supply voltage
<b>V<sub>SS</sub></b>	Logic ground
<b>HIN1,2,3</b> <b>HIN1,2,3</b>	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase [IRS213(6,63,65,66,67,68)D] Logic inputs for high side gate driver outputs (HO1,2,3), in phase (IRS21362D)
<b>LIN1,2,3</b>	Logic input for low side gate driver outputs (LO1,2,3), out of phase
<b>FAULT</b>	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output
<b>EN</b>	Logic input to enable I/O functionality. I/O logic functions when ENABLE is high (i.e., positive logic) No effect on <b>FAULT</b> and not latched
<b>ITRIP</b>	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates <b>FAULT</b> and RCIN low. When ITRIP becomes inactive, <b>FAULT</b> stays active low for an externally set time $T_{FLTCLR}$ , then automatically becomes inactive (open-drain high impedance).
<b>RCIN</b>	External RC network input used to define <b>FAULT</b> CLEAR delay, $T_{FLTCLR}$ , approximately equal to $R \cdot C$ When RCIN > 8 V, the <b>FAULT</b> pin goes back into open-drain high-impedance
<b>COM</b>	Low side gate drivers return
<b>V<sub>B1,2,3</sub></b>	High side floating supply
<b>HO1,2,3</b>	High side gate driver outputs
<b>V<sub>S1,2,3</sub></b>	High voltage floating supply return
<b>LO1,2,3</b>	Low side driver sourcing outputs

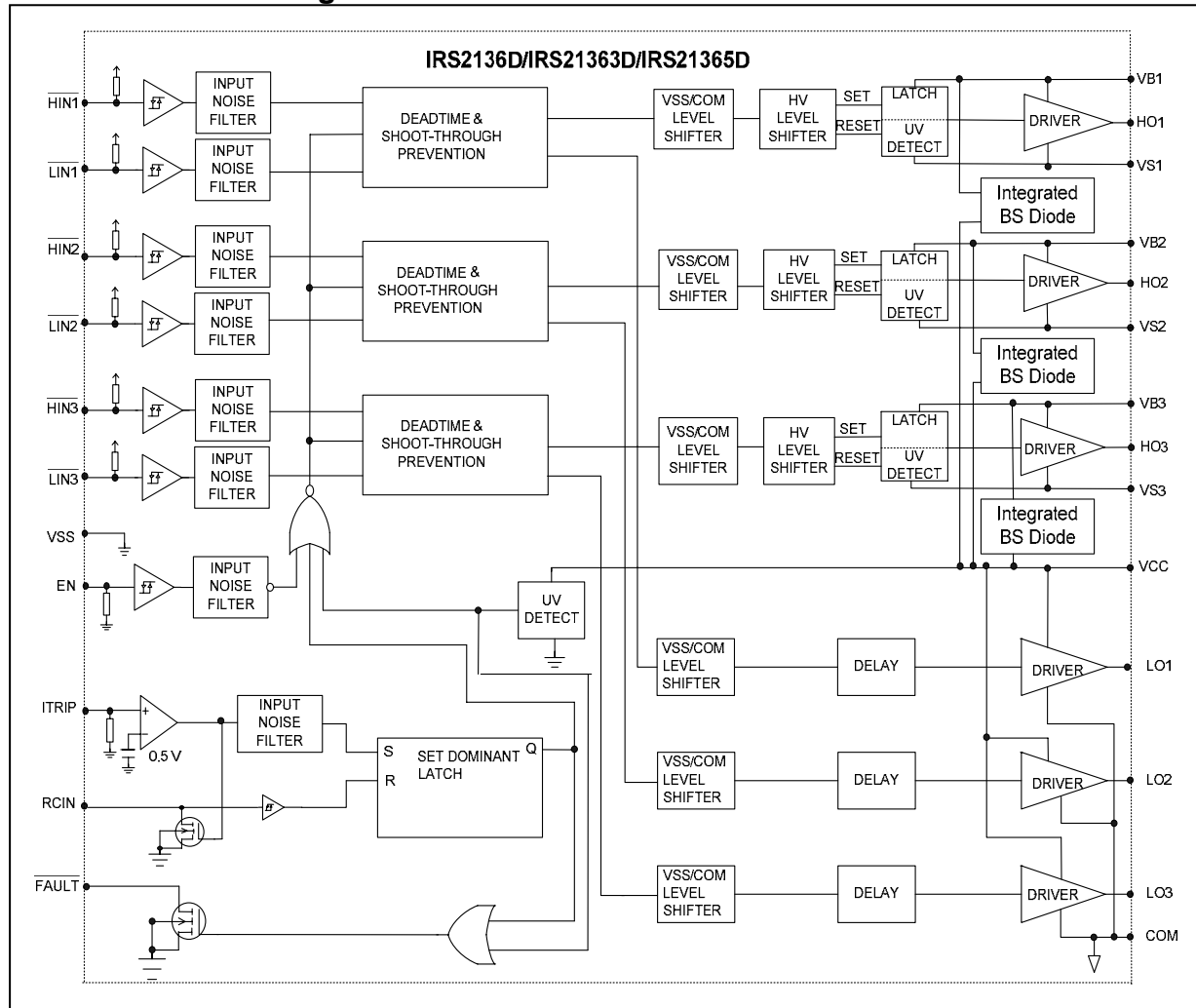
**Note:** LIN, HIN, EN, and ITRIP are internally clamped with a 5.2 V zener diode.



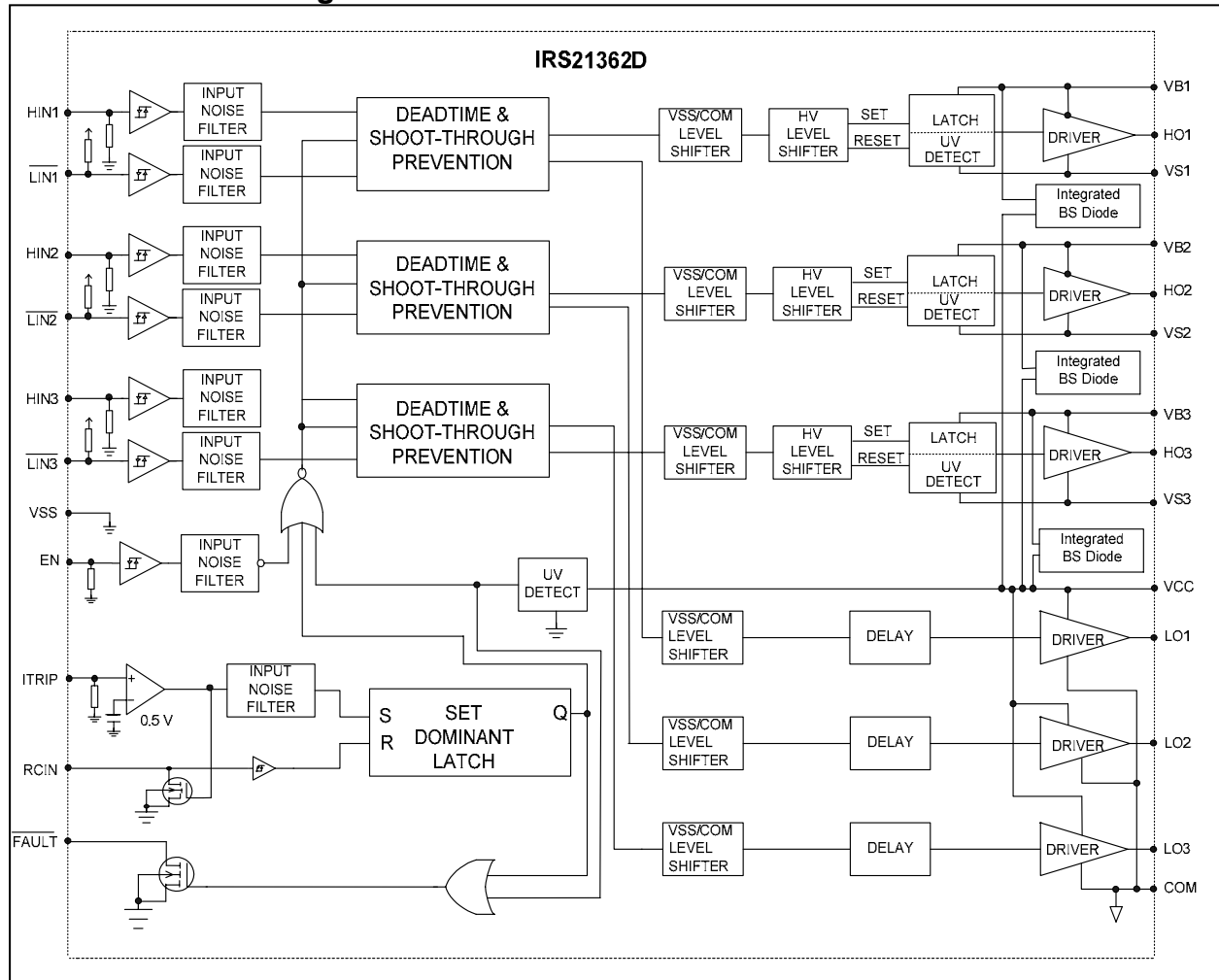
## Lead Assignments

 <p><b>28 Lead PDIP</b></p>	 <p><b>44 Lead PLCC w/o 12 leads</b></p>	 <p><b>28 Lead SOIC (wide body)</b></p>
<p><b>IRS213(6, 63, 65, 66, 67,68)D</b></p>	<p><b>IRS213(6, 63, 65, 66, 67,68)DJ</b></p>	<p><b>IRS213(6, 63, 65, 66, 67,68)DS</b></p>
 <p><b>28 Lead PDIP</b></p>	 <p><b>44 Lead PLCC w/o 12 leads</b></p>	 <p><b>28 Lead SOIC (wide body)</b></p>
<p><b>IRS21362D</b></p>	<p><b>IRS21362DJ</b></p>	<p><b>IRS21362DS</b></p>

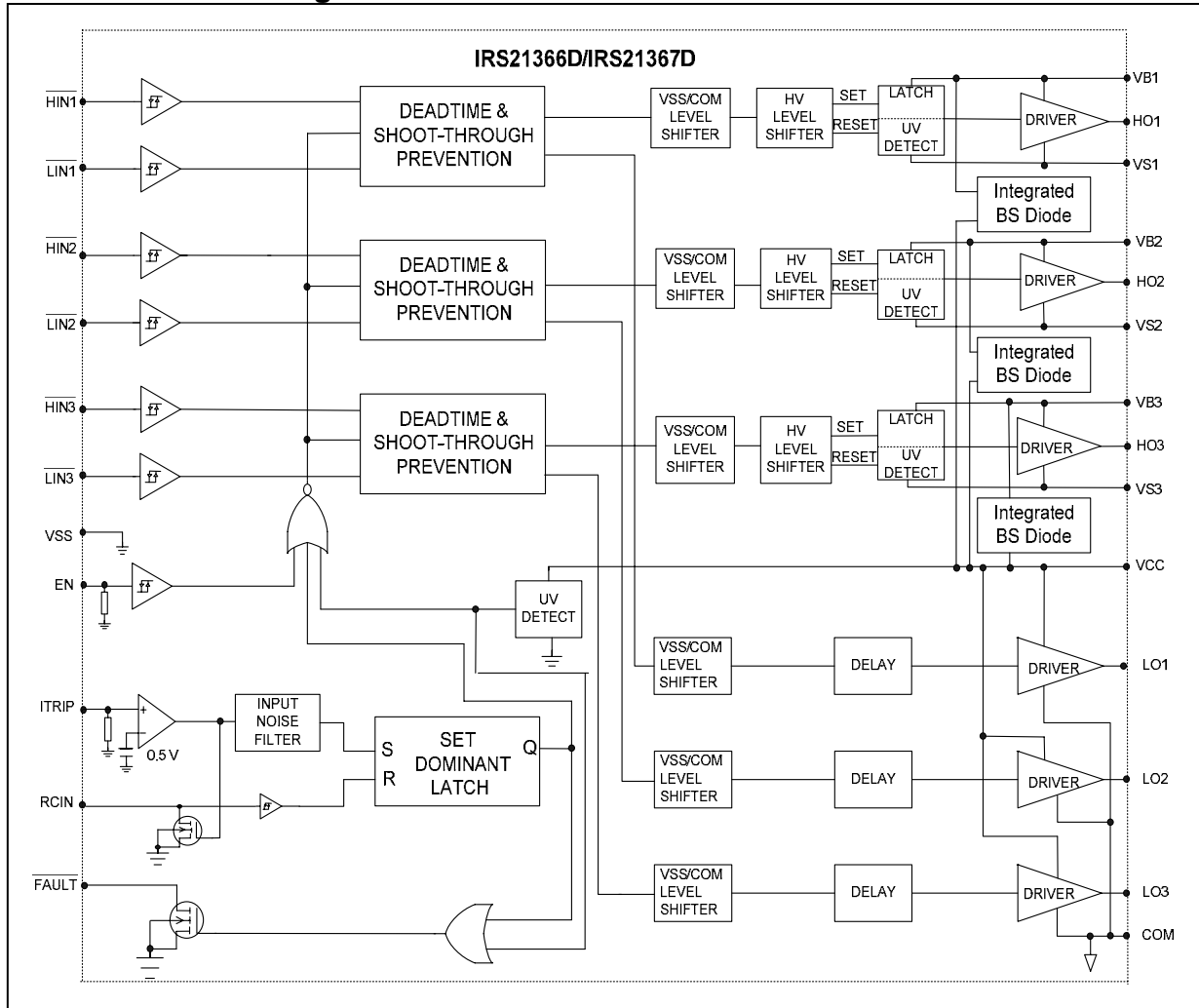
## Functional Block Diagram



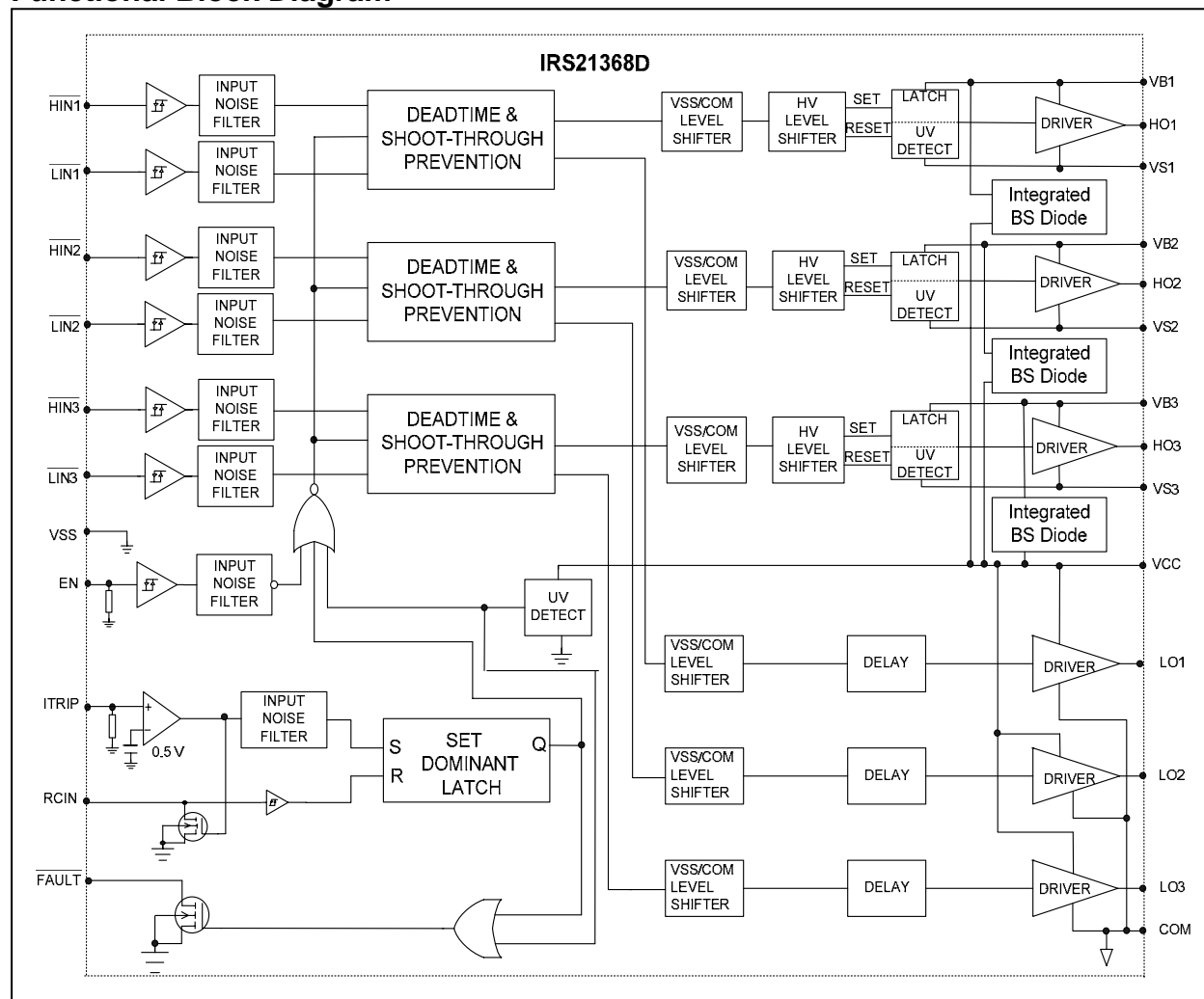
## Functional Block Diagram



## Functional Block Diagram



## Functional Block Diagram



VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<UVCC	X	X	X	0 (note 1)	0	0
15 V	<UVBS	0 V	5 V	high imp	LIN1,2,3	0 (note 2)
15 V	15 V	0 V	5 V	high imp	LIN1,2,3	HIN1,2,3
15 V	15 V	>V <sub>ITRIP</sub>	5 V	0 (note 3)	0	0
15 V	15 V	0 V	0 V	high imp	0	0

**Note 1:** A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.

**Note 2:** UVCC is not latched, when  $V_{CC} > UVCC$ ,  $\overline{FAULT}$  returns to high impedance.

**Note 3:** When  $V_{BS} < UVBS$ , HO goes low. After  $V_{BS}$  goes higher than UVBS, HO stays low until a new falling IRS213(6,63,65,66,67,68)D or rising IRS21362D transition of HIN.

**Note 4:** When  $ITRIP < V_{ITRIP}$ ,  $\overline{FAULT}$  returns to high-impedance after RCIN pin becomes greater than 8 V (@  $V_{CC} = 15$  V).

## 1 Features Description

### 1.1 Integrated Bootstrap Functionality

The IRS2136xD family embeds an integrated bootstrap FET that allows an alternative drive of the bootstrap supply for a wide range of applications.

There is one bootstrap FET for each channel and it is connected between each of the floating supply ( $V_{B1}$ ,  $V_{B2}$ ,  $V_{B3}$ ) and  $V_{CC}$  (see Fig. 7).

The bootstrap FET of each channel follows the state of the respective low side output stage (i.e., bootFet is ON when LO is high, it is OFF when LO is low), unless the  $V_B$  voltage is higher than approximately  $1.1(V_{CC})$ . In that case the bootstrap FET stays off until the  $V_B$  voltage returns below that threshold (see Fig. 8).

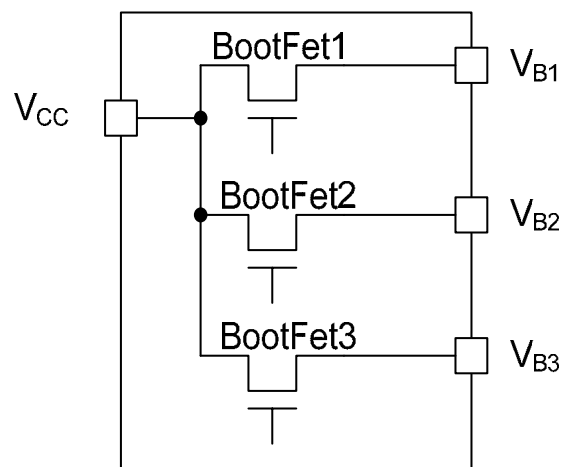


Fig. 7. Simplified BootFet Connection

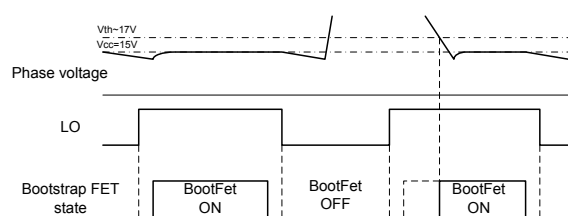


Fig. 8. State Diagram

Bootstrap FET is suitable for most PWM modulation schemes and can be used either in parallel with the external bootstrap network (diode+resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations in the following situations:

- when used in non-complementary PWM schemes (typically 6-step modulations)

- at a very high PWM duty cycle due to the bootstrap FET equivalent resistance ( $R_{BS}$ , see page 5).

In these cases, better performances can be achieved by using the IRS2136x non D version with an external bootstrap network.

## 2 PCB Layout Tips

### 2.1 Distance from H to L Voltage

The IRS2136xDJ package lacks some pins (see page 8) in order to maximizing the distance between the high voltage and low voltage pins. It's strongly recommended to place the components tied to the floating voltage in the respective high voltage portions of the device ( $V_{B1,2,3}$ ,  $V_{S1,2,3}$ ) side.

### 2.2 Ground Plane

To minimize noise coupling ground plane must not be placed under or near the high voltage floating side.

### 2.3 Gate Drive Loops

Current loops behave like an antenna able to receive and transmit EM noise (see Fig. 9). In order to reduce EM coupling and improve the power switch turn on/off performances, gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to develop a voltage across the gate-emitter increasing the possibility of self turn-on effect.

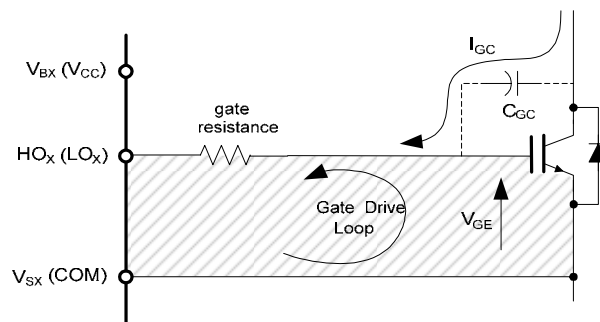


Fig. 9. Antenna Loops

### 2.4 Supply Capacitors

Supply capacitors must be placed as close as possible to the device pins ( $V_{CC}$  and  $V_{SS}$  for the ground tied supply,  $V_B$  and  $V_S$  for the floating supply) in order to minimize parasitic inductance/resistance.

## **2.5 Routing and Placement**

Power stage PCB parasitic may generate dangerous voltage transients for the gate driver and the control logic. In particular it's recommended to limit phase voltage negative transients.

In order to avoid such undervoltage it is highly recommended to minimize high side emitter to low side collector distance and low side emitter to negative bus rail stray inductance. See DT04-4 at [www.irf.com](http://www.irf.com) for more detailed information.

Figures 10-30 provide information on the experimental performance of the IRS2136DS HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples from multiple wafer lots were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

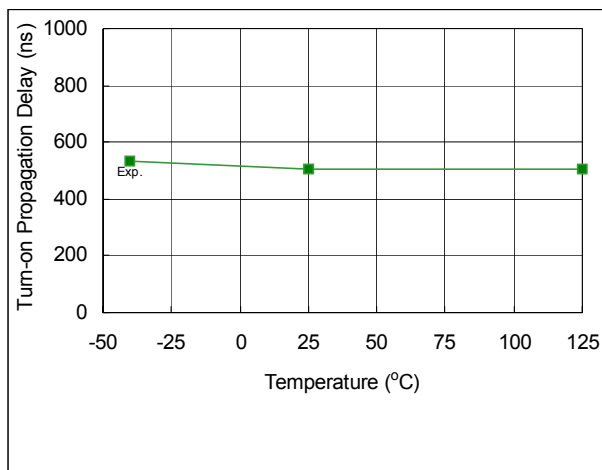


Fig. 10. Turn-On Propagation Delay vs. Temperature

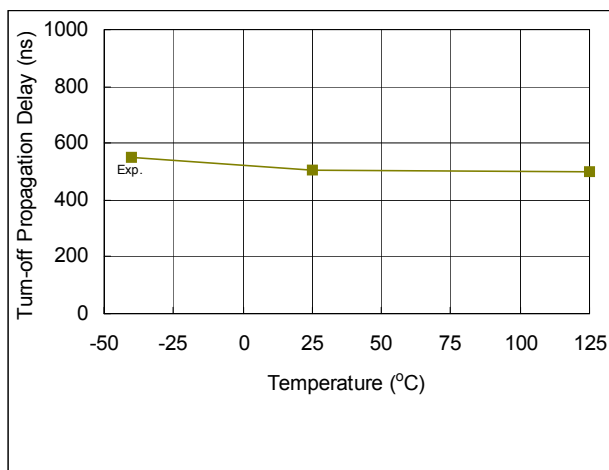


Fig. 11. Turn-Off Propagation Delay vs. Temperature

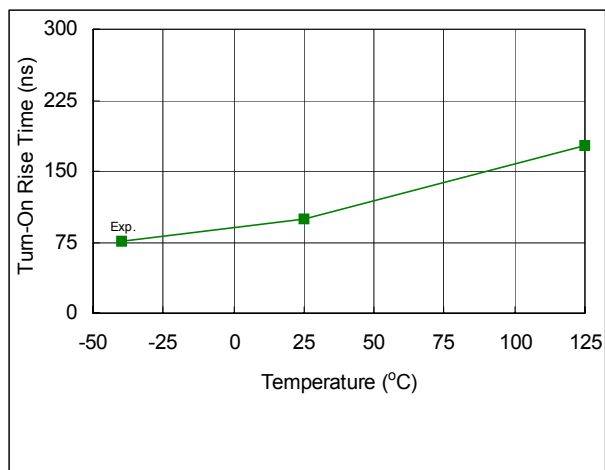


Fig. 12. Turn-On Rise Time vs. Temperature

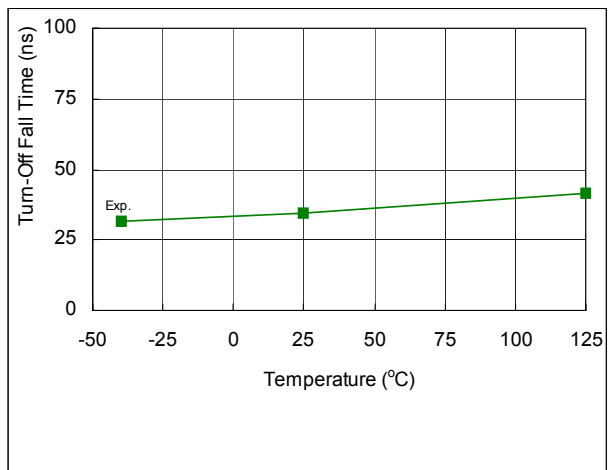


Fig. 13. Turn-Off Fall Time vs. Temperature



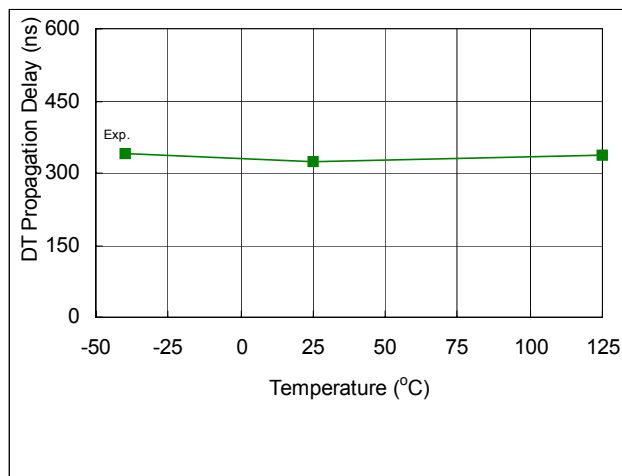


Fig. 14. DT Propagation Delay vs. Temperature

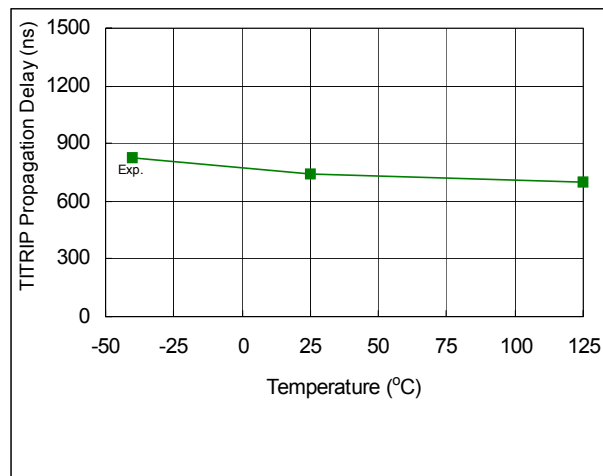


Fig. 15. TITRIP Propagation Delay vs. Temperature

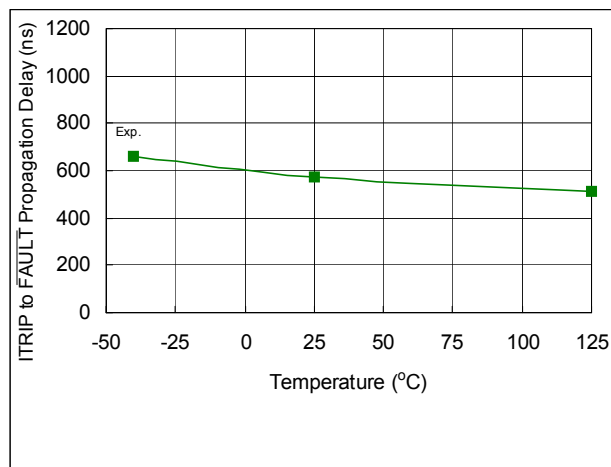


Fig. 16. ITRIP to FAULT Propagation Delay vs. Temperature

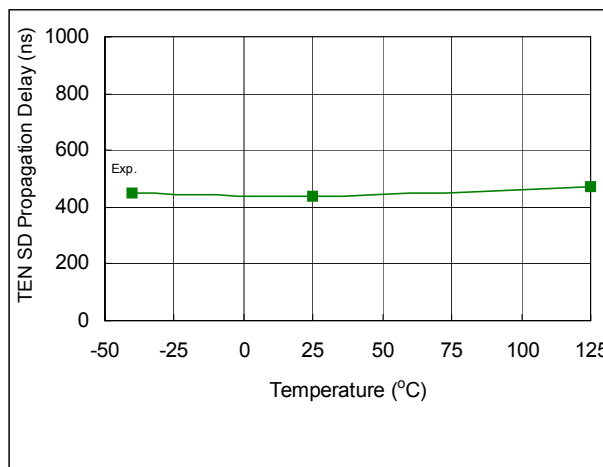


Fig. 17. TEN SD Propagation Delay vs. Temperature

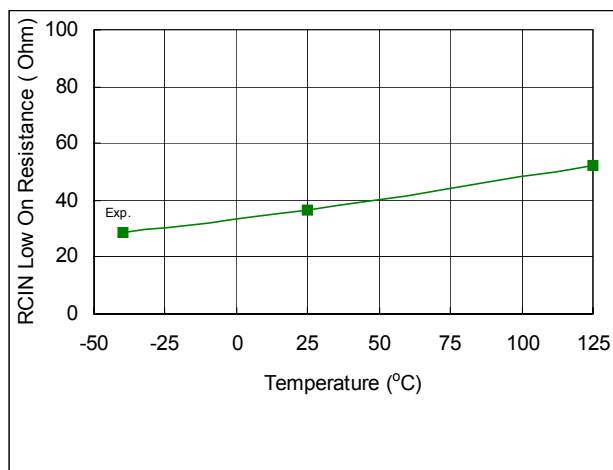


Fig. 18. RCIN Low On Resistance vs. Temperature

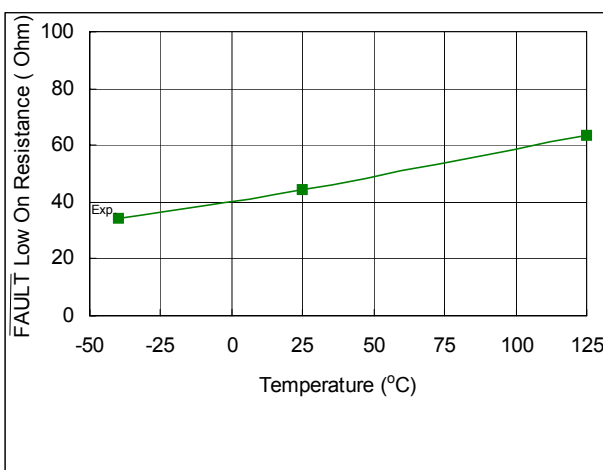


Fig. 19. FAULT Low On Resistance vs. Temperature

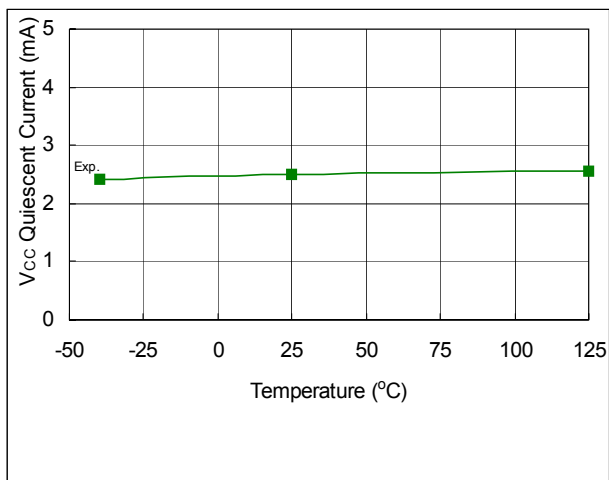


Fig. 20. V<sub>CC</sub> Quiescent Current vs. Temperature

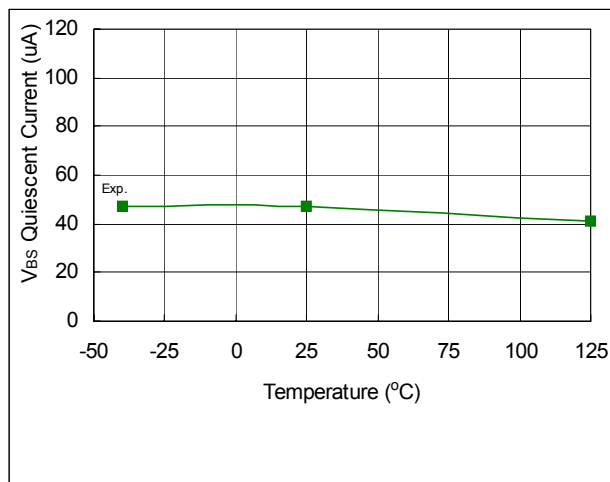


Fig. 21. V<sub>BS</sub> Quiescent Current vs. Temperature

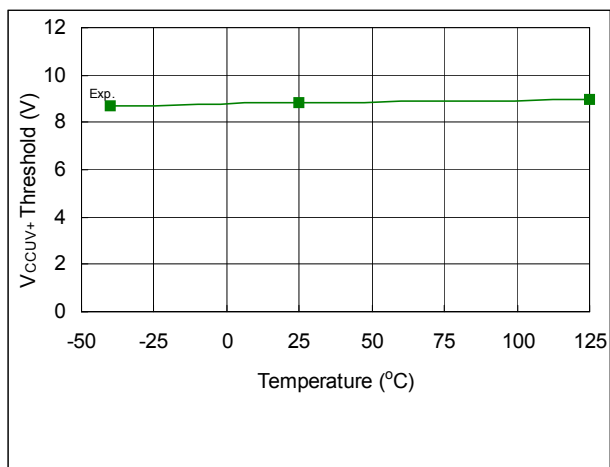


Fig. 22. V<sub>CCUV+</sub> Threshold vs. Temperature

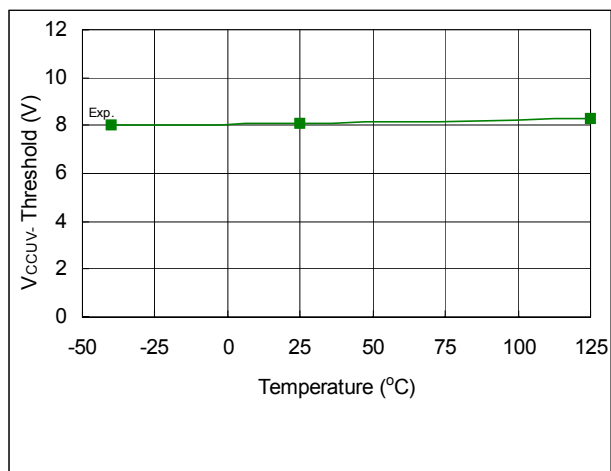


Fig. 23. V<sub>CCUV-</sub> Threshold vs. Temperature

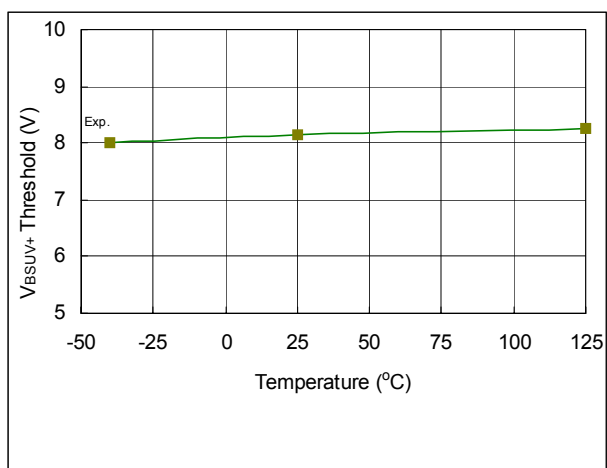


Fig. 24. V<sub>BSUV+</sub> Threshold vs. Temperature

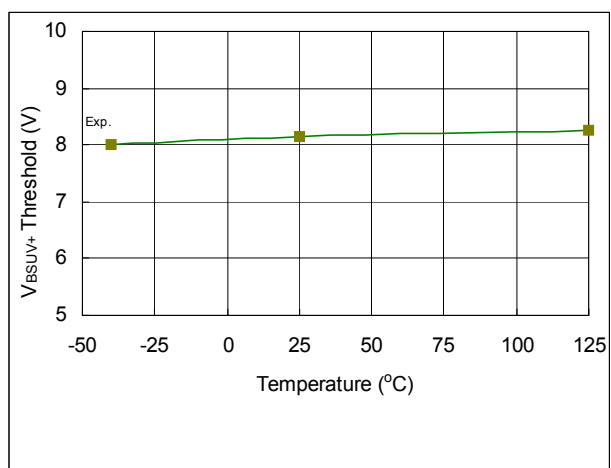


Fig. 25. V<sub>BSUV-</sub> Threshold vs. Temperature

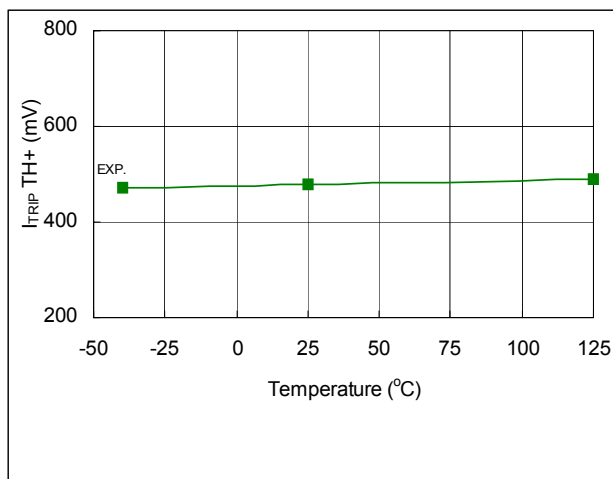


Fig. 26.  $I_{TRIP} TH+$  vs. Temperature

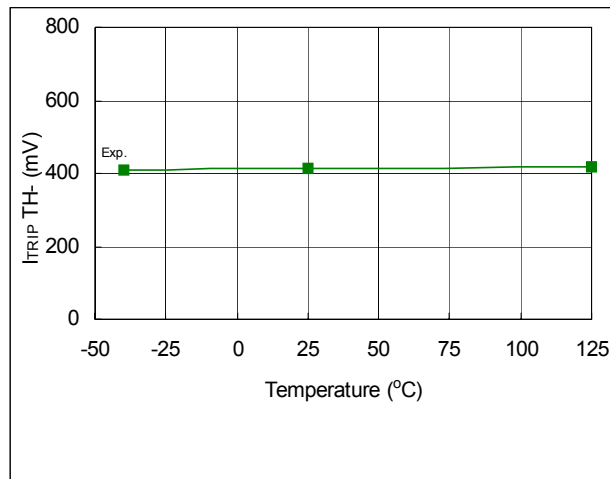


Fig. 27.  $I_{TRIP} TH-$  vs. Temperature

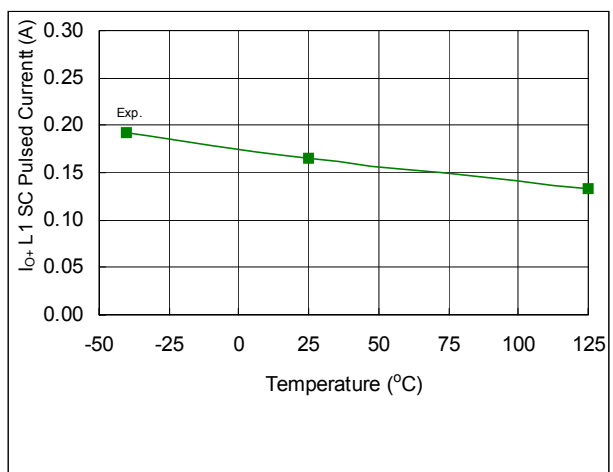


Fig. 28.  $I_{O+} L1 SC$  Pulsed Current vs. Temperature

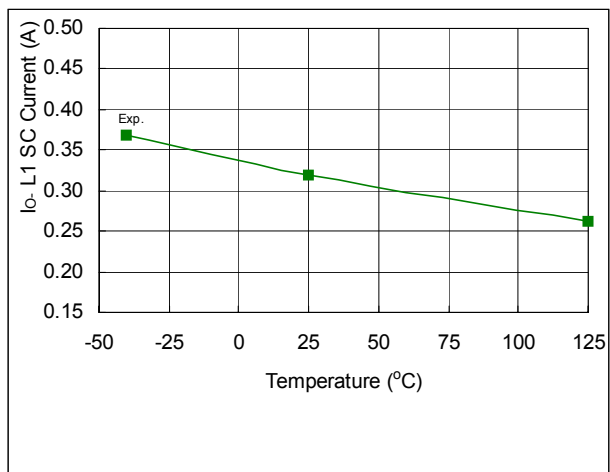


Fig. 29.  $I_{O-} L1 SC$  Pulsed Current vs. Temperature

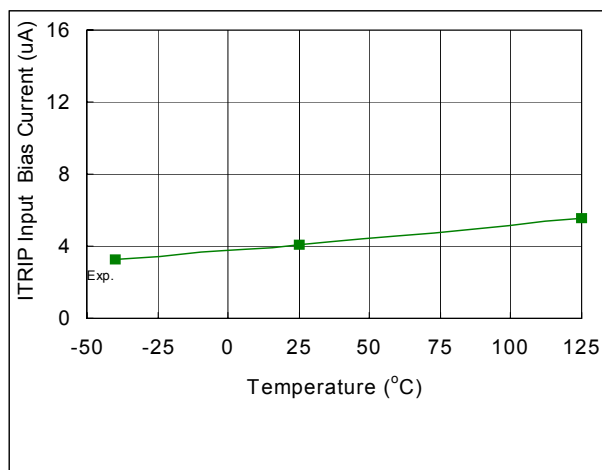
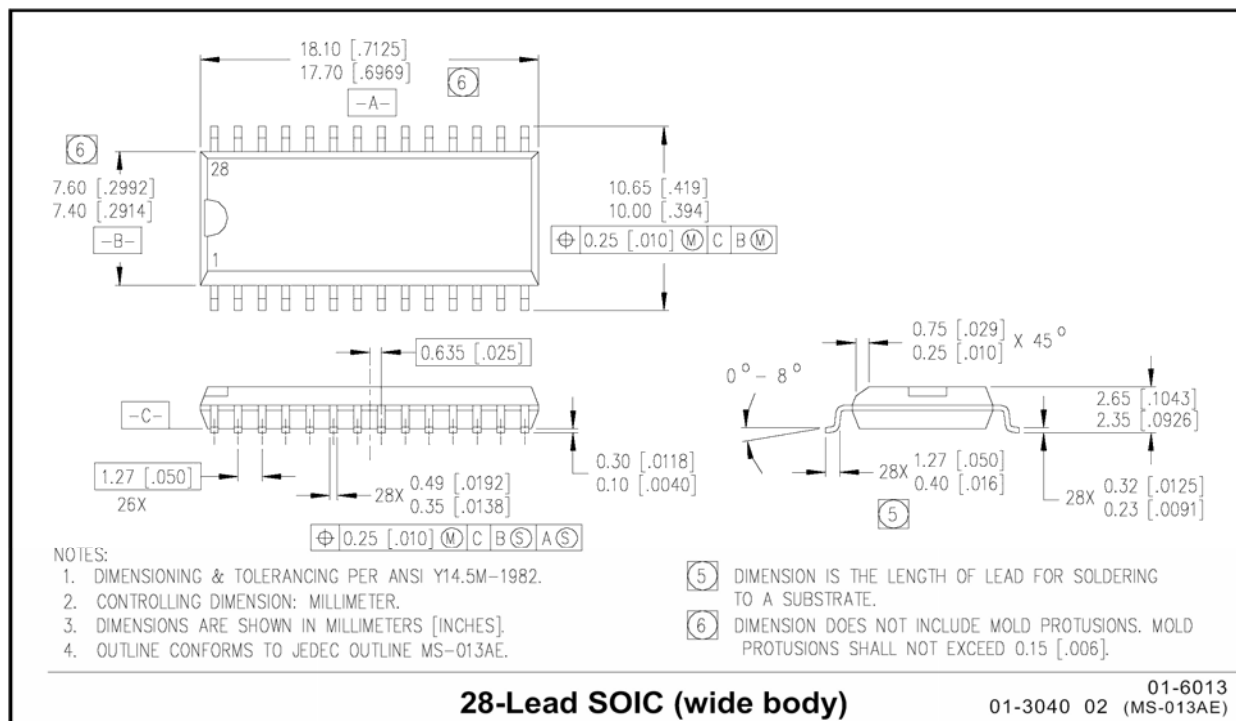
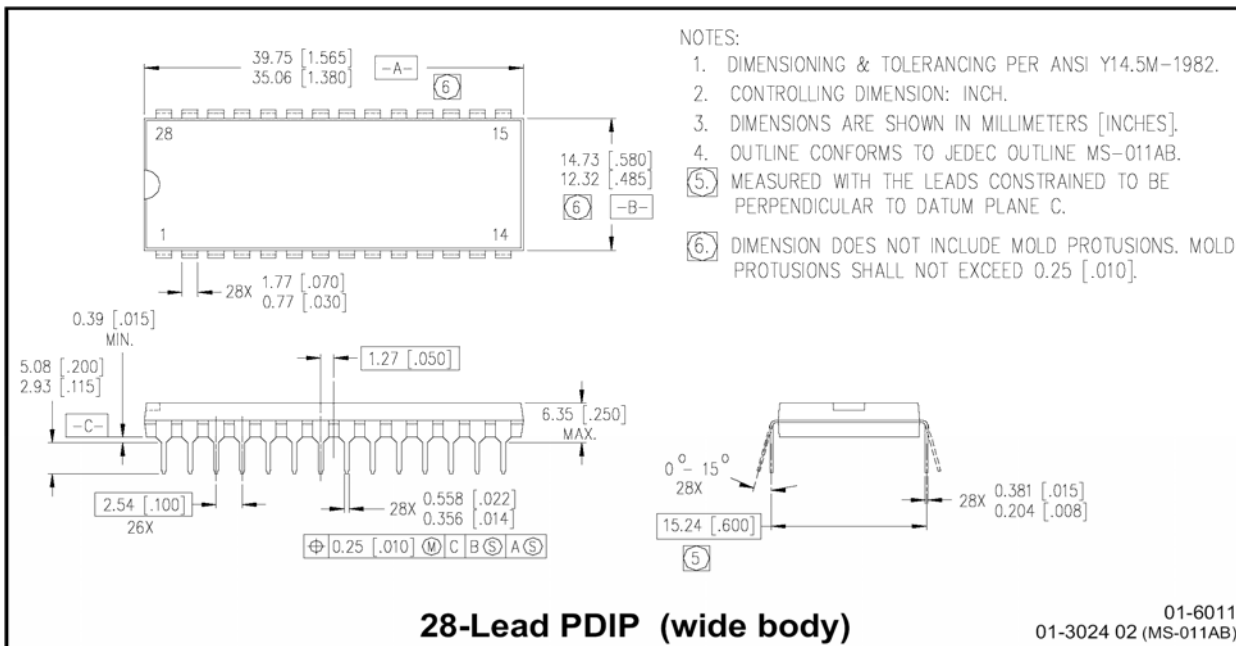
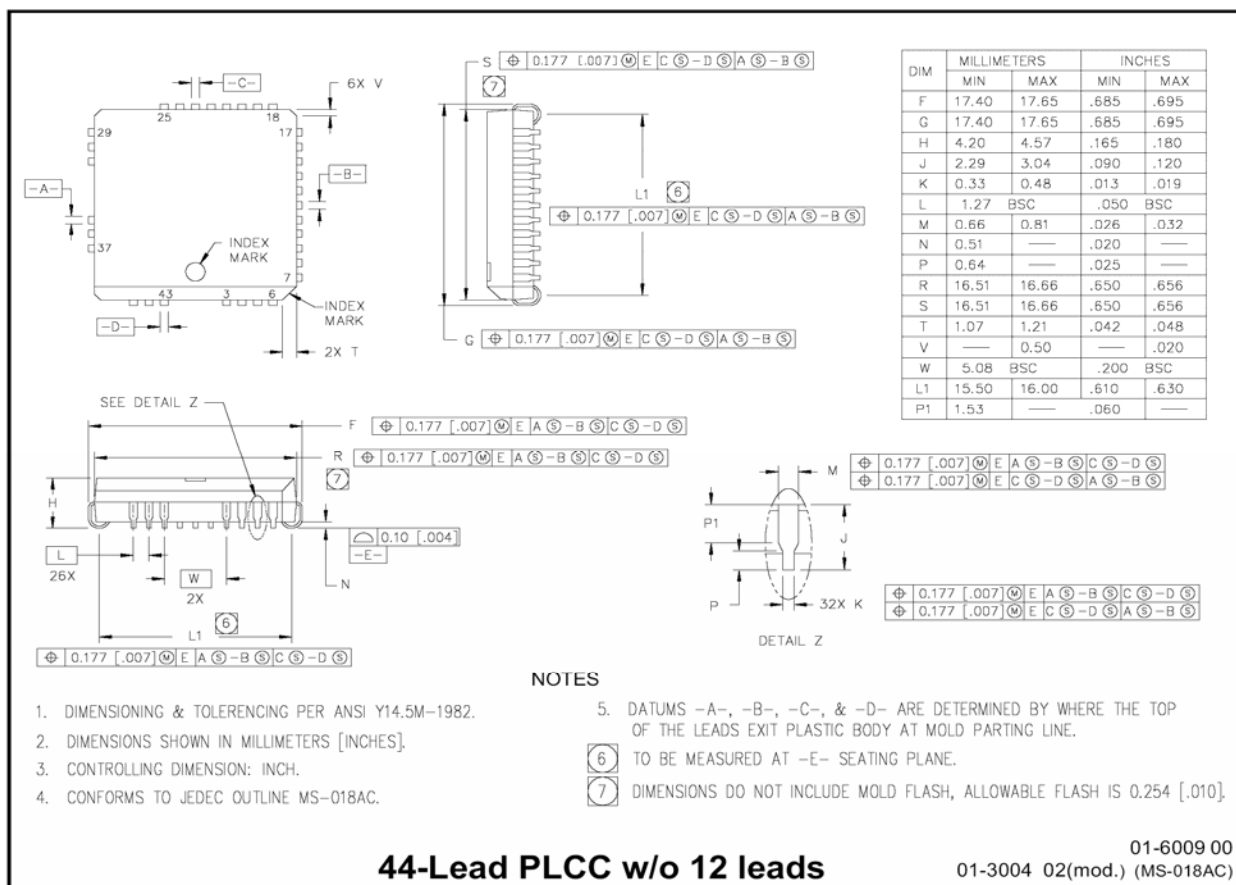


Fig. 30.  $I_{TRIP}$  Input Bias Current vs. Temperature

## Case Outlines



## Case Outlines

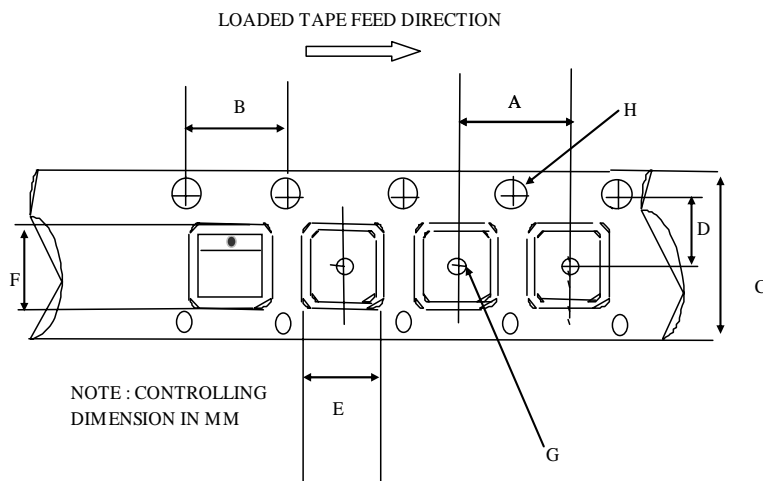


**44-Lead PLCC w/o 12 leads**

01-6009 00  
01-3004 02(mod.) (MS-018AC)

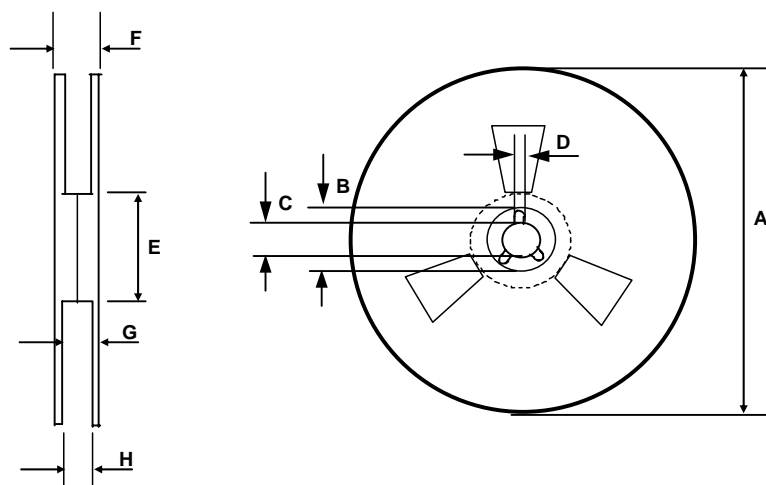
# IRS213(6,62,63,65,66,67,68)D(J&S)PbF

**PRELIMINARY**



CARRIER TAPE DIMENSION FOR 44PLCC

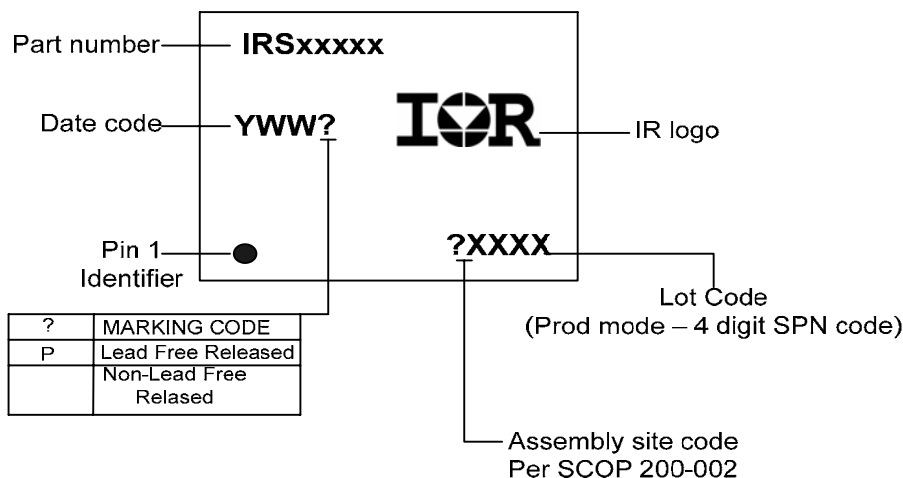
Code	Metric		Imperial	
	Min	Max	Min	Max
A	23.90	24.10	0.94	0.948
B	3.90	4.10	0.153	0.161
C	31.70	32.30	1.248	1.271
D	14.10	14.30	0.555	0.562
E	17.90	18.10	0.704	0.712
F	17.90	18.10	0.704	0.712
G	2.00	n/a	0.078	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 44PLCC

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	38.4	n/a	1.511
G	34.7	35.8	1.366	1.409
H	32.6	33.1	1.283	1.303

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 28-Lead SOIC IRS21363DSPbF  
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 28-Lead SOIC IRS21366DSPbF  
 28-Lead SOIC IRS21367DSPbF  
 28-Lead SOIC IRS21368DSPbF  
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 44-Lead PLCC IRS21363DJPbF  
 44-Lead PLCC IRS21365DJPbF  
 44-Lead PLCC IRS21366DJPbF  
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 44-Lead PLCC IRS21368DJPbF

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