

2.75-W FIXED GAIN MONO FILTER-FREE CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- Maximize Battery Life and Minimize Heat
 - 0.5- μ A Shutdown Current
 - 3.0-mA Quiescent Current
 - High Efficiency Class-D
 - 88% at 400mW at 8 Ω
 - 80% at 100mW at 8 Ω
- Three Fixed Gain Versions
 - TPA2032D1 has a gain of 2 V/V (6dB)
 - TPA2033D1 has a gain of 3 V/V (9.5dB)
 - TPA2034D1 has a gain of 4 V/V (12dB)
- Only One External Component Required
 - Internal Matched Input Gain and Feedback Resistors for Excellent PSRR and CMRR
 - Optimized PWM Output Stage Eliminates LC Output Filter
 - PSRR (–75 dB) and Wide Supply Voltage (2.5 V to 5.5 V) Eliminates Need for a Dedicated Voltage Regulator
 - Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
 - CMRR (–69 dB) Eliminates Two Input Coupling Capacitors
- Thermal and Short-Circuit Protection
- Pinout Very Similar to TPA2010D1

- Wafer Chip Scale Packaging (WCSP)
 - NanoFree™ Lead-Free (Pb-Free: YZF)

APPLICATIONS

- Ideal for Wireless Handsets, PDAs, and other mobile devices

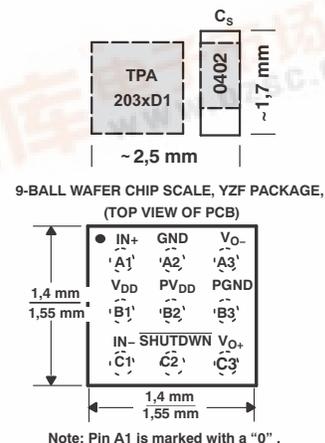
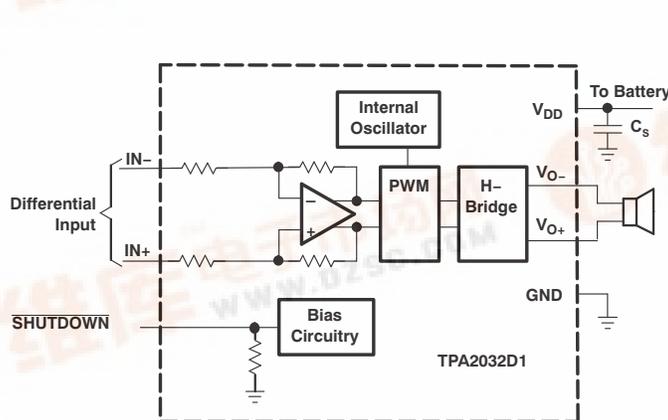
DESCRIPTION

The TPA2032D1 (2V/V gain), TPA2033D1 (3V/V gain), and TPA2034D1 (4V/V gain) are 2.75-W high efficiency filter-free class-D audio power amplifiers, each in an approximately 1.5-mm \times 1.5-mm wafer chip scale package (WCSP) that requires only one external component. The pinout is the same as the TPA2010D1 except that the external gain setting input resistors required by the TPA2010D1 are integrated into the fixed gain TPA203xD1 family.

Features like –75dB PSRR and improved RF-rectification immunity with a very small PCB footprint (WCSP amplifier plus single decoupling cap) make the TPA203xD1 family ideal for wireless handsets. A fast start-up time of 3.2 ms with minimal pop makes the TPA203xD1 family ideal for PDA applications.

In wireless handsets, the earpiece, speaker phone, and melody ringer can each be driven by a TPA203xD1. The TPA203xD1 family has a low 27- μ V noise floor, A-weighted.

APPLICATION CIRCUIT





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	PACKAGE	PART NUMBER	SYMBOL
–40°C to 85°C	Wafer chip scale packaging – Lead free (YZF)	TPA2032D1YZF ⁽¹⁾	BPX
–40°C to 85°C	Wafer chip scale packaging – Lead free (YZF)	TPA2033D1YZF ⁽¹⁾	BPY
–40°C to 85°C	Wafer chip scale packaging – Lead free (YZF)	TPA2034D1YZF ⁽¹⁾	BPZ

(1) The YZF package is only available taped and reeled. To order add the suffix *R* to the end of the part number for a reel of 3000, or add the suffix *T* to the end of the part number for a reel of 250 (e.g. TPA2032D1YZFR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

		TPA2032D1, TPA2033D1, TPA2034D1
V _{DD}	Supply voltage	In active mode
		In SHUTDOWN mode
V _I	Input voltage	–0.3 V to V _{DD} + 0.3 V
Continuous total power dissipation		See Dissipation Rating Table
T _A	Operating free-air temperature	–40°C to 85°C
T _J	Operating junction temperature	–40°C to 125°C
T _{stg}	Storage temperature	–65°C to 150°C
ESD	Electro-Static Discharge Tolerance - Human Body Model (HBM) for all pins ⁽²⁾	2KV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The output pins Vo– and Vo+ are tolerant to 1.5KV HBM ESD

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	2.5		5.5	V
V _{IH}	High-level input voltage	SHUTDOWN		V _{DD}	V
V _{IL}	Low-level input voltage	SHUTDOWN		0.35	V
V _{IC}	Common mode input voltage range	V _{DD} = 2.5 V, 5.5 V		V _{DD} –0.8	V
T _A	Operating free-air temperature	–40		85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR (1 / θ _{JA})	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
YZF	4.8 mW/°C ⁽¹⁾	480 mW	264 mW	192 mW
YZF	7.5 mW/°C ⁽²⁾	750 mW	412 mW	300 mW

(1) Derating factor measured with JEDEC Low-K board; 1S0P - One signal layer and zero plane layers.

(2) Derating factor measured with JEDEC High K board; 1S2P - One signal layer and two plane layers.

Please see JEDEC Standard 51-3 for Low-K board, JEDEC Standard 51-7 for High-K board, and JEDEC Standard 51-12 for using package thermal information.

Please see JEDEC document page for downloadable copies: <http://www.jedec.org/download/default.cfm>.

ELECTRICAL CHARACTERISTICS

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V _{OS}	Output offset voltage (measured differentially)	Inputs AC grounded, V _{DD} = 2.5 V to 5.5 V	TPA2032D1	5	25	mV	
			TPA2033D1	5	25		
			TPA2034D1	5	25		
PSRR	Power supply rejection ratio	V _{DD} = 2.5 V to 5.5 V	-75	-61		dB	
CMRR	Common mode rejection ratio	V _{IC} = 0.5 V to (V _{DD} - 0.8 V)	V _{DD} = 2.5 V	-69	-52	dB	
			V _{DD} = 3.6 V	-69	-52		
			V _{DD} = 5.5 V	-69	-52		
I _{IH}	High-level input current	V _{DD} = 5.5 V, V _I = 5.8 V			50	μA	
I _{IL}	Low-level input current	V _{DD} = 5.5 V, V _I = -0.3 V			5	μA	
I _(Q)	Quiescent current	V _{DD} = 5.5 V, no load		4	5.7	mA	
		V _{DD} = 3.6 V, no load		3			
		V _{DD} = 2.5 V, no load		2.2	3.7		
I _(SD)	Shutdown current	V _(SHUTDOWN) = 0.35 V, V _{DD} = 2.5 V to 5.5 V		0.5	0.8	μA	
r _{DS(on)}	Static drain-source on-state resistance	V _{DD} = 2.5 V		550		mΩ	
		V _{DD} = 3.6 V		420			
		V _{DD} = 5.0 V		350			
	Output impedance in SHUTDOWN	V _(SHUTDOWN) ≤ 0.35 V		2		kΩ	
f _(sw)	Switching frequency	V _{DD} = 2.5 V to 5.5 V	240	300	400	kHz	
Gain		V _{DD} = 2.5 V to 5.5 V	TPA2032D1	5.5	6	6.5	dB
			TPA2033D1	9.0	9.5	10.0	
			TPA2034D1	11.5	12	12.5	
R _{PD}	Resistance of internal pulldown resistor from shutdown pin to GND			300		kΩ	

OPERATING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _O	Output power	R _L = 4 Ω, THD + N = 10%, f = 1 kHz	V _{DD} = 5 V	2.75		W
			V _{DD} = 3.6 V	1.35		
			V _{DD} = 2.5 V	0.59		
		R _L = 4 Ω, THD + N = 1%, f = 1 kHz	V _{DD} = 5 V	2.25		W
			V _{DD} = 3.6 V	1.12		
			V _{DD} = 2.5 V	0.48		
		R _L = 8 Ω, THD + N = 10%, f = 1 kHz	V _{DD} = 5 V	1.68		W
			V _{DD} = 3.6 V	0.85		
			V _{DD} = 2.5 V	0.38		
		R _L = 8 Ω, THD + N = 1%, f = 1 kHz	V _{DD} = 5 V	1.37		W
			V _{DD} = 3.6 V	0.68		
			V _{DD} = 2.5 V	0.31		
THD+N	Total harmonic distortion plus noise	V _{DD} = 5 V, P _O = 1 W, R _L = 8 Ω, f = 1 kHz		0.18%		
		V _{DD} = 3.6 V, P _O = 0.5 W, R _L = 8 Ω, f = 1 kHz		0.11%		
		V _{DD} = 2.5 V, P _O = 200 mW, R _L = 8 Ω, f = 1 kHz		0.10%		
k _{SVR}	Supply ripple rejection ratio	V _{DD} = 3.6 V, Inputs AC grounded with C ₁ = 1 μF	f = 217 Hz, V _(RIPPLE) = 200 mV _{pp}	-73		dB
SNR	Signal-to-noise ratio	V _{DD} = 5 V, P _O = 1 W, R _L = 8 Ω, A weighted noise		100		dB

OPERATING CHARACTERISTICS (continued)

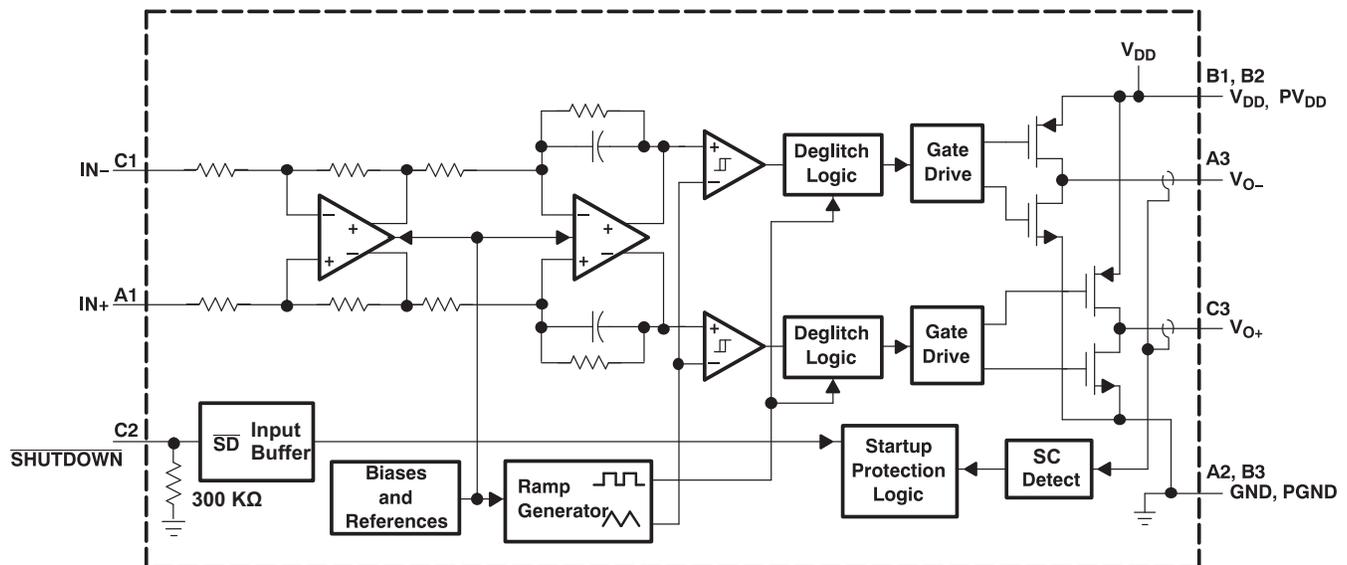
$T_A = 25^\circ\text{C}$, $R_L = 8\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_n	Output voltage noise	$V_{DD} = 3.6\ \text{V}$, $f = 20\ \text{Hz to } 20\ \text{kHz}$, Inputs AC grounded with $C_i = 1\ \mu\text{F}$	No weighting	35		μV_{RMS}
			A weighting	27		
CMRR	Common mode rejection ratio	$V_{DD} = 3.6\ \text{V}$, $V_{IC} = 1.0\ \text{V}_{\text{pp}}$, $V_{\text{Cm}} = 1.8\ \text{V}$ $f = 217\ \text{Hz}$		-69		dB
R_i	Input impedance	$A_V = 2\ \text{V/V}$		30.2		k Ω
		$A_V = 3\ \text{V/V}$		22.8		
		$A_V = 4\ \text{V/V}$		18.5		
Start-up time from shutdown		$V_{DD} = 3.6\ \text{V}$		3.2		ms

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	YZF		
IN-	C1	I	Negative differential audio input
IN+	A1	I	Positive differential audio input
V_{O-}	A3	O	Negative BTL audio output
V_{O+}	C3	O	Positive BTL audio output
GND	A2	I	Analog ground terminal. Must be connected to same potential as PGND using a direct connection to a single point ground.
PGND	B3		High-current Analog ground terminal. Must be connected to same potential as GND using a direct connection to a single point ground.
V_{DD}	B1	I	Power supply terminal. Must be connected to same power supply as PV_{DD} using a direct connection. Voltage must be within values listed in Recommended Operating Conditions table.
PV_{DD}	B2	I	High-current Power supply terminal. Must be connected to same power supply as V_{DD} using a direct connection. Voltage must be within values listed in Recommended Operating Conditions table.
SHUTDOWN	C2	I	Shutdown terminal. When terminal is low the device is put into Shutdown mode.

FUNCTIONAL BLOCK DIAGRAM

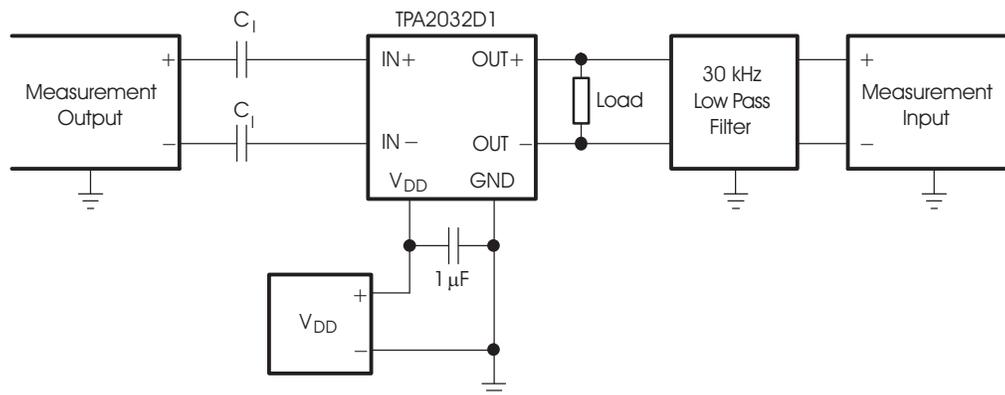


TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
Efficiency		vs Output power	1, 2
P_D	Power dissipation	vs Output power	3, 4
	Supply current	vs Output power	5, 6
I_{DD}	Supply current	vs Supply voltage	7
$I_{(SD)}$	Shutdown current	vs Shutdown voltage	8
P_O	Output power	vs Load resistance	9, 10
		vs Supply voltage	11
THD+N	Total harmonic distortion plus noise	vs Output power	12, 13
		vs Frequency	14, 15, 16, 17
		vs Common-mode input voltage	18
K_{SVR}	Supply voltage rejection ratio	vs Frequency	19, 20, 21, 22, 23, 24, 25, 26, 27
	GSM power supply rejection	vs Time	28
		vs Frequency	29
K_{SVR}	Supply voltage rejection ratio	vs Common-mode input voltage	30, 31, 32
CMRR	Common-mode rejection ratio	vs Frequency	33
		vs Common-mode input voltage	34

TEST SET-UP FOR GRAPHS



- (1) C_1 was shorted for any common-mode input voltage measurement. All other measurements were taken with a 1- μ F C_1 (unless otherwise noted).
- (2) A 33- μ H inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.
- (3) The 30-kHz low-pass filter is required, even if the analyzer has an internal low-pass filter. An RC low-pass filter (100 Ω , 47-nF) is used on each output for the data sheet graphs.

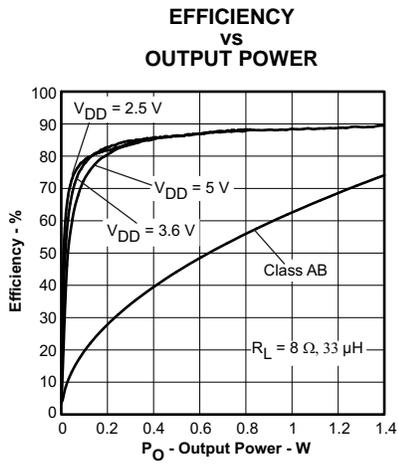


Figure 1.

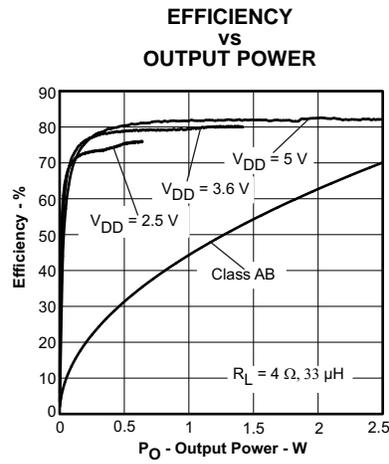


Figure 2.

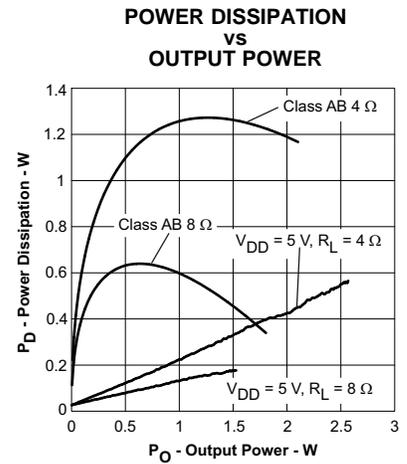


Figure 3.

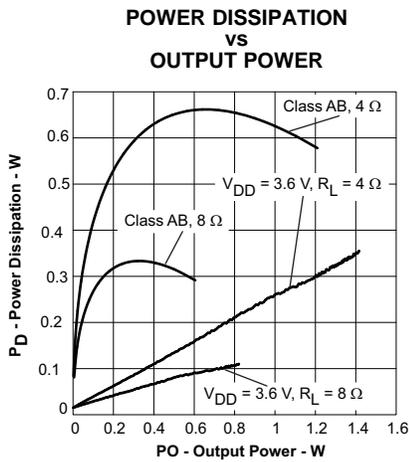


Figure 4.

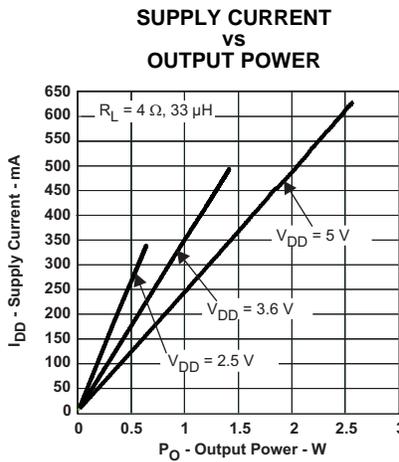


Figure 5.

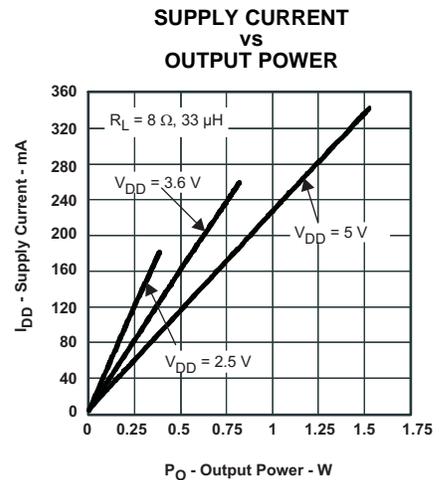


Figure 6.

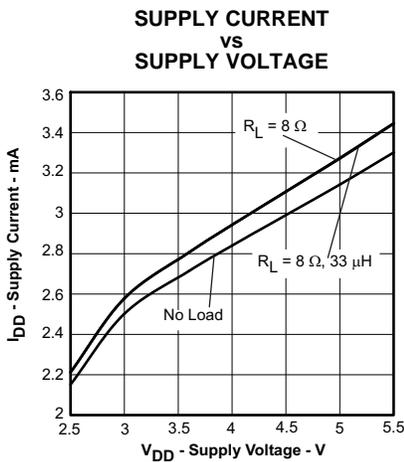


Figure 7.

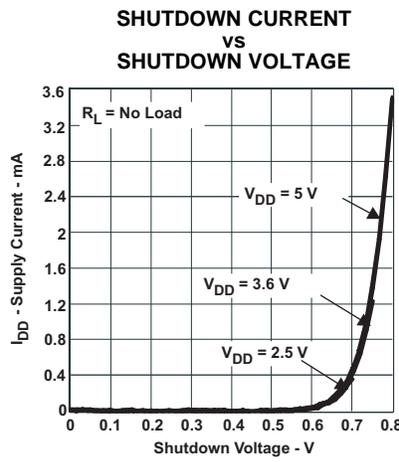


Figure 8.

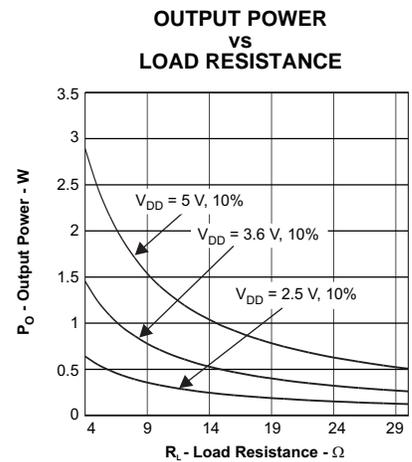


Figure 9.

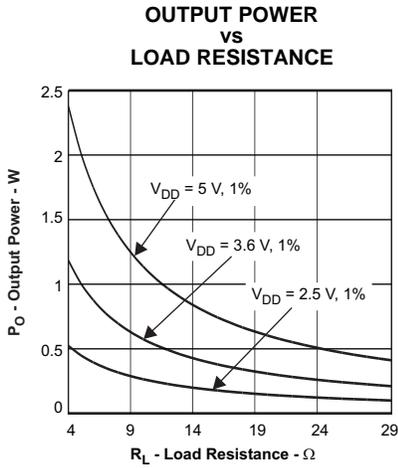


Figure 10.

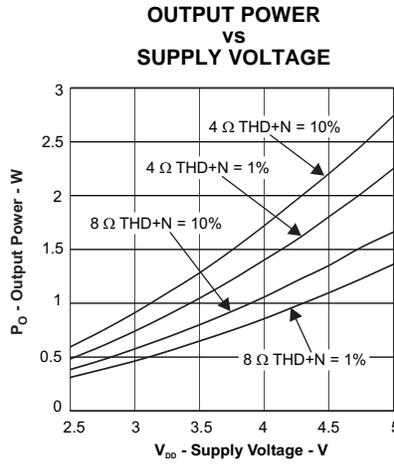


Figure 11.

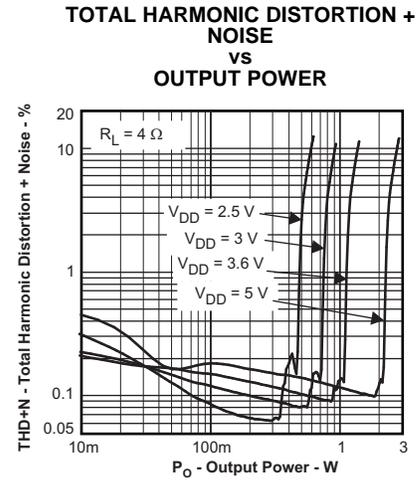


Figure 12.

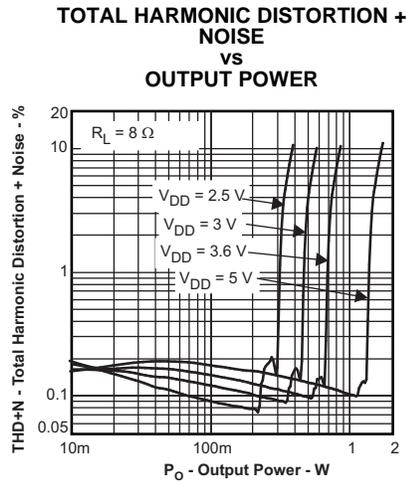


Figure 13.

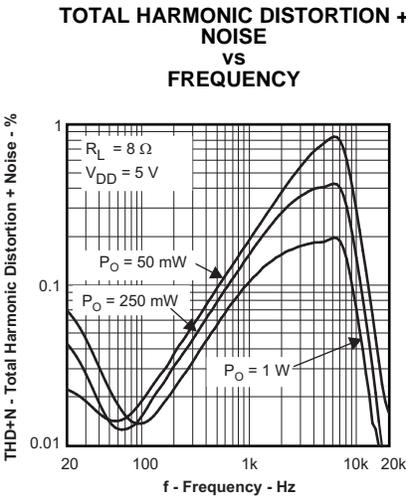


Figure 14.

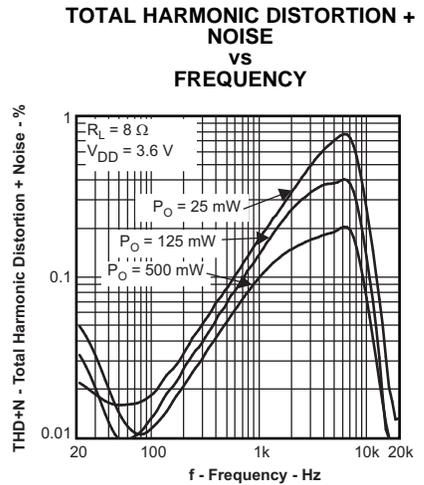


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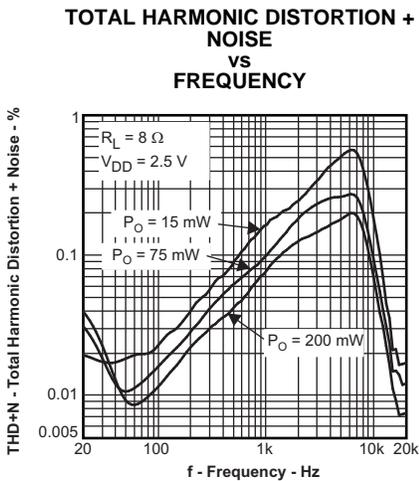


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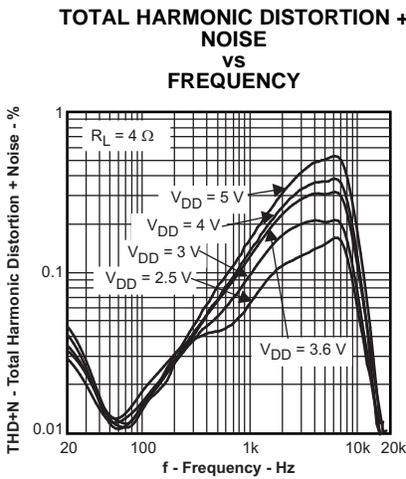


Figure 17.

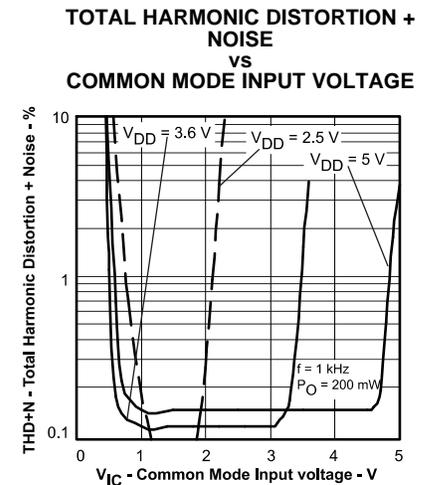


Figure 18.

**SUPPLY RIPPLE REJECTION RATIO
 vs
 FREQUENCY - TPA2032D1**

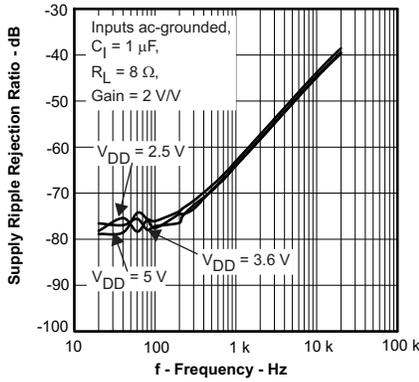


Figure 19.

**SUPPLY RIPPLE REJECTION RATIO
 vs
 FREQUENCY - TPA2033D1**

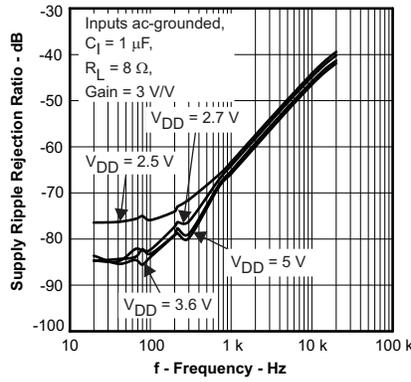


Figure 20.

**SUPPLY RIPPLE REJECTION RATIO
 vs
 FREQUENCY - TPA2034D1**

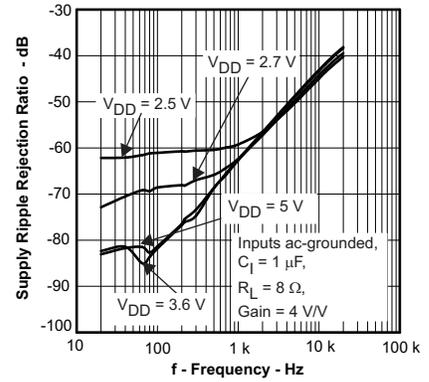


Figure 21.

**SUPPLY RIPPLE REJECTION RATIO
 vs
 FREQUENCY- TPA2032D1**

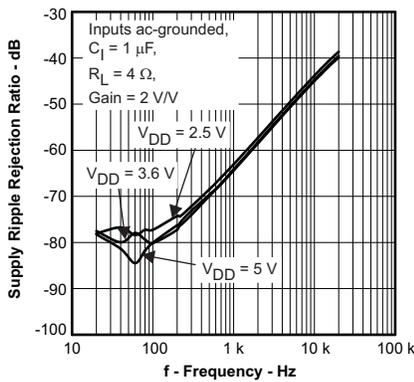


Figure 22.

**SUPPLY RIPPLE REJECTION RATIO
 vs
 FREQUENCY- TPA2033D1**

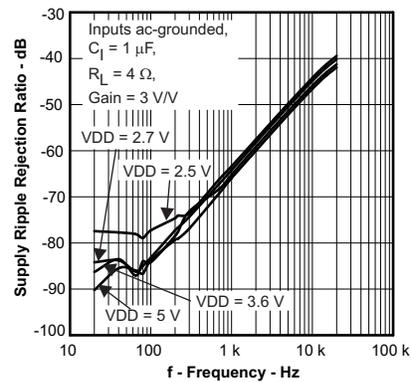


Figure 23.

**SUPPLY RIPPLE REJECTION RATIO
 vs
 FREQUENCY- TPA2034D1**

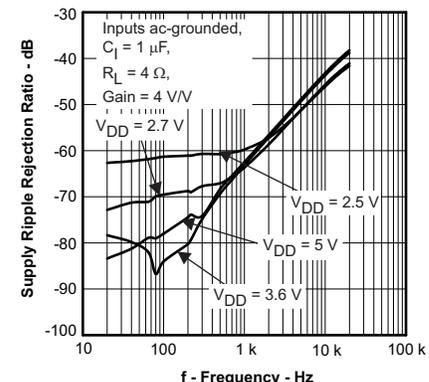


Figure 24.

**SUPPLY RIPPLE REJECTION RATIO
 vs
 FREQUENCY - TPA2032D1**

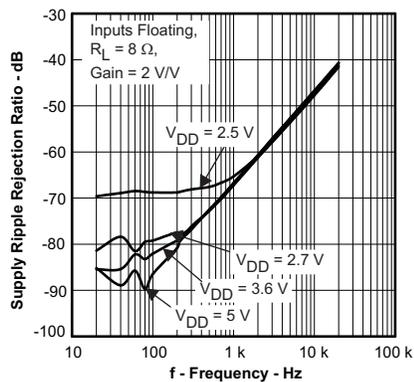


Figure 25.

**SUPPLY RIPPLE REJECTION RATIO
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 FREQUENCY - TPA2033D1**

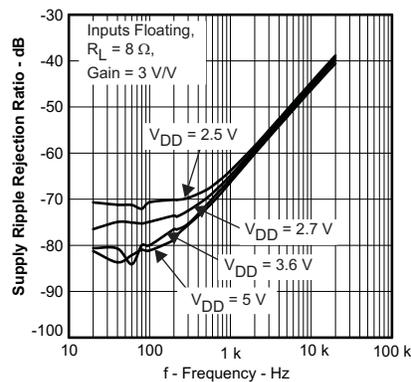


Figure 26.

**SUPPLY RIPPLE REJECTION RATIO
 vs
 FREQUENCY - TPA2034D1**

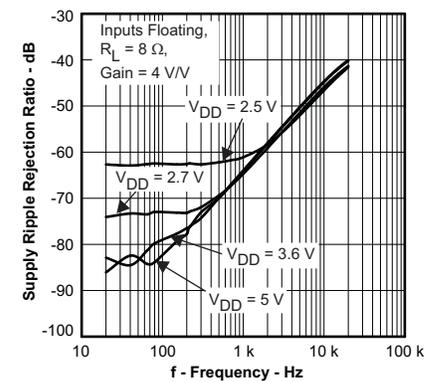


Figure 27.

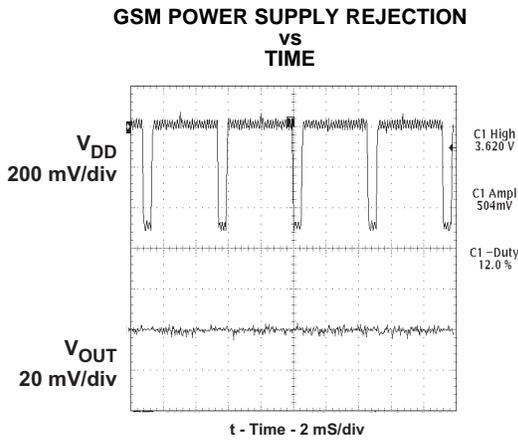


Figure 28.

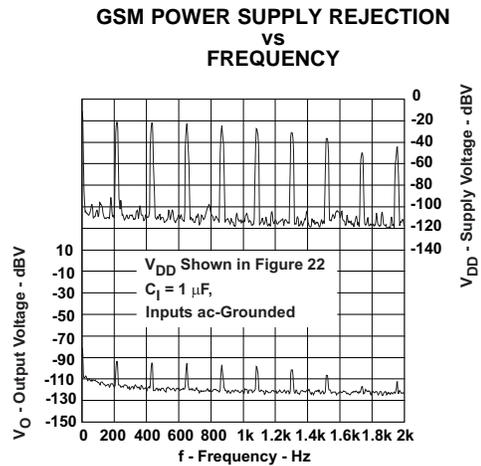


Figure 29.

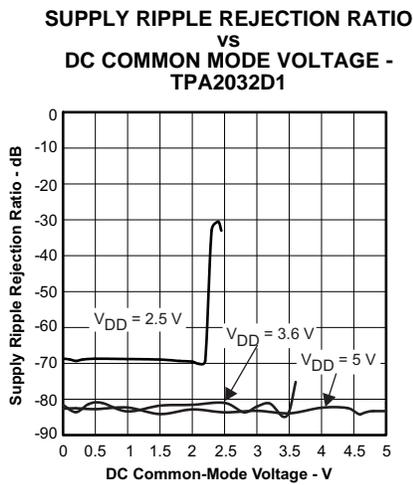


Figure 30.

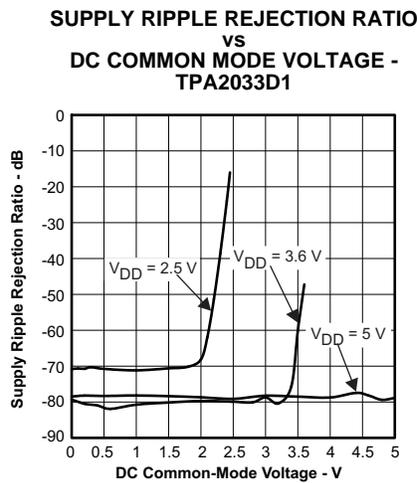


Figure 31.

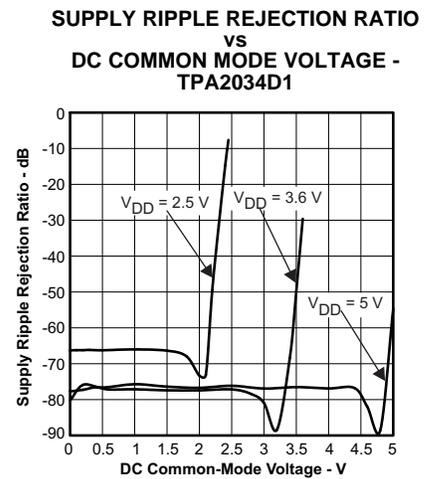


Figure 32.

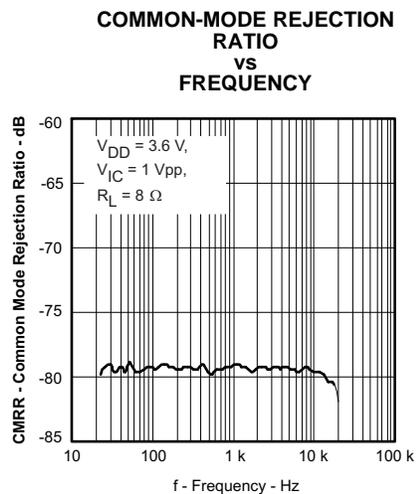


Figure 33.

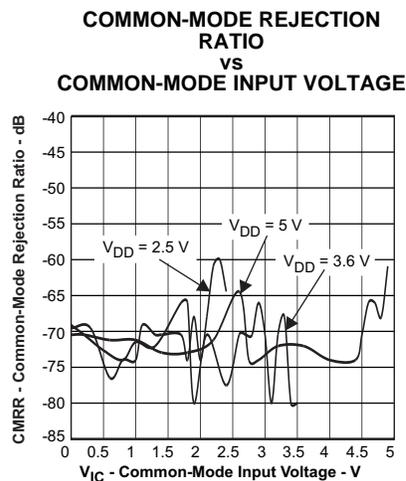


Figure 34.

APPLICATION INFORMATION

FULLY DIFFERENTIAL AMPLIFIER

The TPA2032D1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential TPA2032D1 can still be used with a single-ended input; however, the TPA2032D1 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

- Input-coupling capacitors not required:
 - The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. The inputs of the TPA2032D1 can be biased anywhere within the common mode input voltage range listed in the Recommended Operating Conditions table. If the inputs are biased outside of that range, input-coupling capacitors are required.
- Midsupply bypass capacitor, $C_{(BYPASS)}$, not required:
 - The fully differential amplifier does not require a bypass capacitor. Any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.
- Better RF-immunity:
 - GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal better than the typical audio amplifier.

COMPONENT SELECTION

[Figure 35](#) shows the TPA2032D1 typical schematic with differential inputs, while [Figure 36](#) shows the TPA2032D1 with differential inputs and input capacitors. [Figure 37](#) shows the TPA2032D1 with a single-ended input.

Decoupling Capacitor (C_S)

The TPA2032D1 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically $1\mu\text{F}$, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the TPA2032D1 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a $10\mu\text{F}$ or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device. Typically, the smaller the capacitor's case size, the lower the inductance and the closer it can be placed to the TPA2032D1.

Input Capacitors (C_I)

The TPA2032D1 does not require input coupling capacitors if the design uses a differential source that is biased within the common-mode input voltage range. That voltage range is listed in the Recommended Operating Conditions table. If the input signal is not biased within the recommended common-mode input range, such as in needing to use the input as a high pass filter, shown in [Figure 36](#), or if using a single-ended source, shown in [Figure 37](#), input coupling capacitors are required. The same value capacitors should be used on both $\text{IN}+$ and $\text{IN}-$ for best pop performance.

$$f_c = \frac{1}{(2\pi R_I C_I)} \quad (1)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speaker response may also be taken into consideration when setting the corner frequency using input capacitors.

APPLICATION INFORMATION (continued)

Equation 2 is reconfigured to solve for the input coupling capacitance.

$$C_1 = \frac{1}{(2\pi R_1 f_c)} \tag{2}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of $\pm 10\%$ or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low-frequency response, use large input coupling capacitors (1 μF or larger).

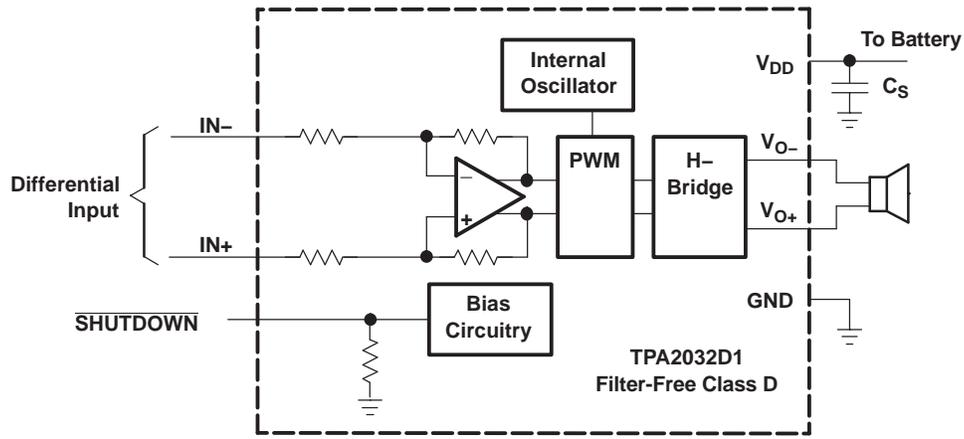


Figure 35. Typical TPA2032D1 Application Schematic With Differential Input for a Wireless Phone

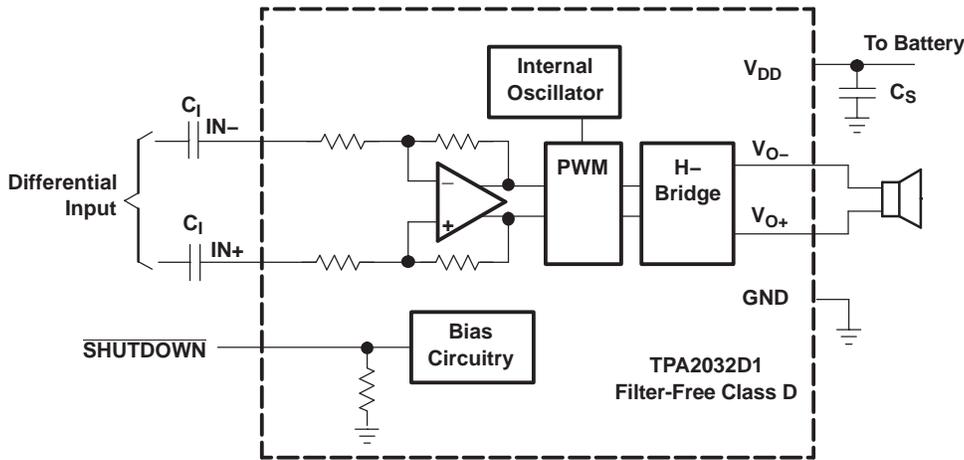


Figure 36. TPA2032D1 Application Schematic With Differential Input and Input Capacitors

APPLICATION INFORMATION (continued)

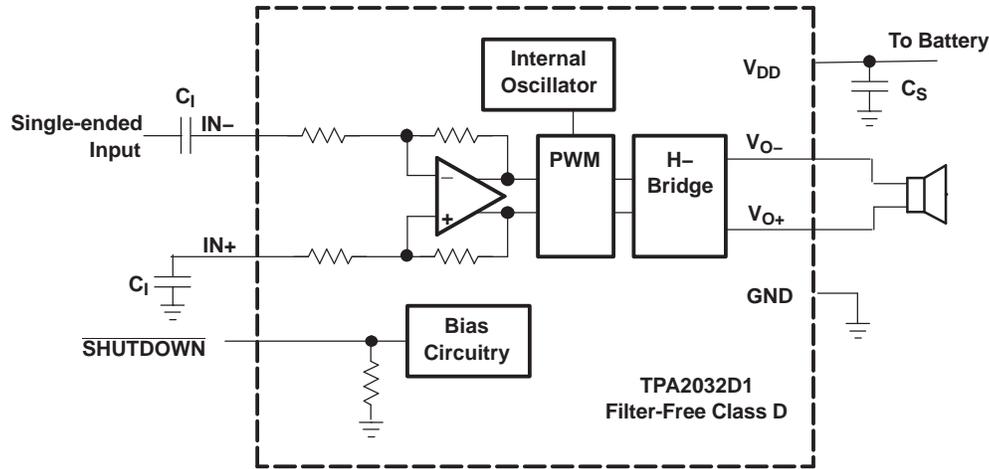


Figure 37. TPA2032D1 Application Schematic With Single-Ended Input

BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use nonsolder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 38 and Table 1 show the appropriate diameters for a WCSP layout. The TPA2032D1 evaluation module (EVM) layout is shown in the next section as a layout example.

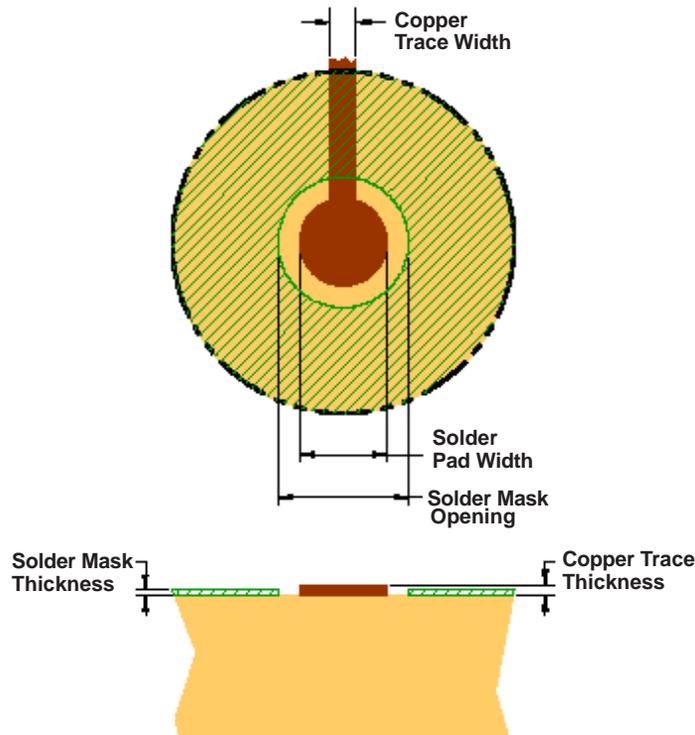


Figure 38. Land Pattern Dimensions

APPLICATION INFORMATION (continued)

Table 1. Land Pattern Dimensions

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK OPENING	COPPER THICKNESS	STENCIL OPENING	STENCIL THICKNESS
Nonsolder mask defined (NSMD)	275 μm (+0.0, -25 μm)	375 μm (+0.0, -25 μm)	1 oz max (32 μm)	275 μm x 275 μm Sq. (rounded corners)	125 μm thick

NOTES:

1. Circuit traces from NSMD defined PWB lands should be 75 μm to 100 μm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
2. Recommended solder paste is Type 3 or Type 4.
3. Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating range of the intended application.
4. For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 μm to avoid a reduction in thermal fatigue performance.
5. Solder mask thickness should be less than 20 μm on top of the copper circuit pattern.
6. Best solder stencil performance is achieved using laser-cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
7. Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

Component Location

Place all the external components very close to the TPA2032D1. Placing the decoupling capacitor, C_S , close to the TPA2032D1 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Trace Width

Recommended trace width at the solder balls is 75 μm to 100 μm to prevent solder wicking onto wider PCB traces. [Figure 39](#) shows the layout of the TPA2032D1 evaluation module (EVM).

For high current pins (V_{DD} , GND V_{O+} , and V_{O-}) of the TPA2032D1, use 100- μm trace widths at the solder balls and at least 500- μm PCB traces to ensure proper performance and output power for the device.

For input pins (IN-, IN+, and $\overline{\text{SHUTDOWN}}$) of the TPA2032D1, use 75- μm to 100- μm trace widths at the solder balls. IN- and IN+ traces need to run side-by-side to maximize common-mode noise cancellation.

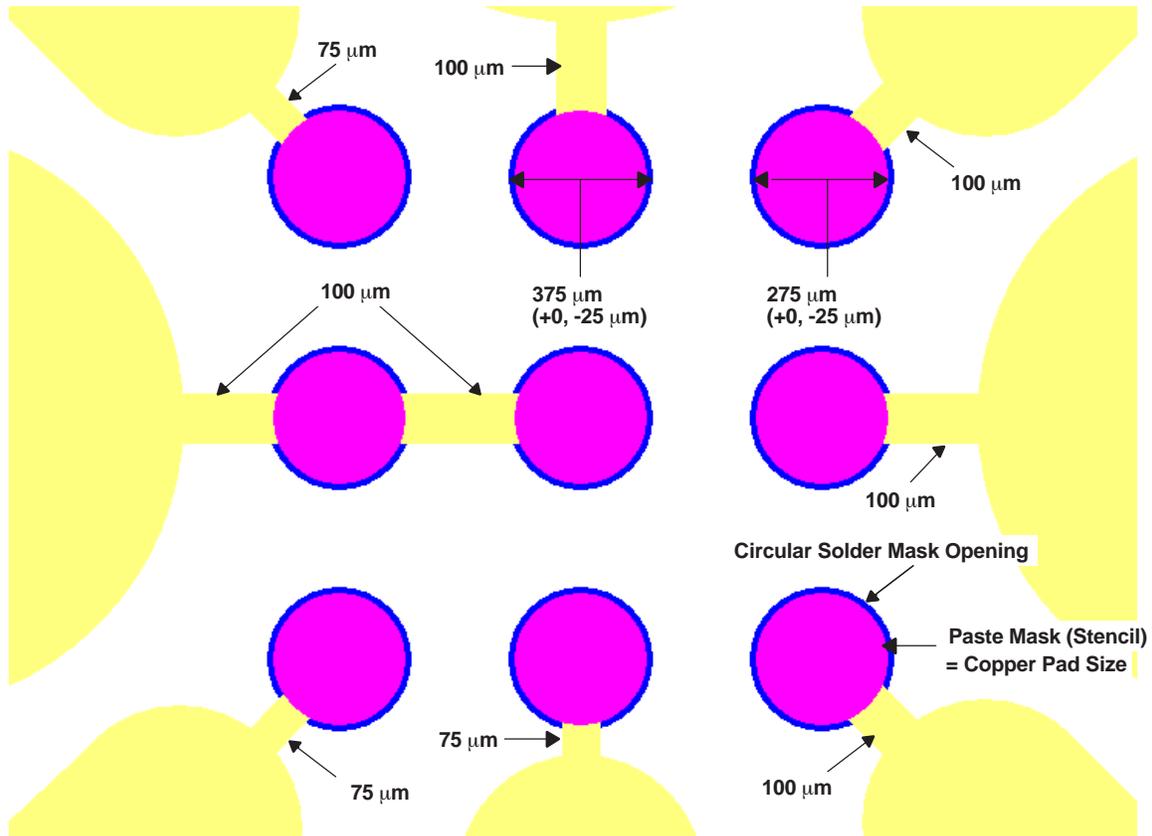


Figure 39. Close Up of TPA2032D1 Land Pattern From TPA2032D1 EVM

EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the YZF package is shown in the dissipation rating table. Converting this to θ_{JA} :

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} \quad (3)$$

Given θ_{JA} (from the Package Dissipation ratings table), the maximum allowable junction temperature (from the Absolute Maximum ratings table), and the maximum internal dissipation (from Power Dissipation vs Output Power figures) the maximum ambient temperature can be calculated with the following equation. Note that the units on these figures are Watts RMS. Because of crest factor (ratio of peak power to RMS power) from 9–15 dB, thermal limitations are not usually encountered.

$$T_{A\text{Max}} = T_{J\text{Max}} - \theta_{JA} P_{D\text{max}} \quad (4)$$

The TPA2032D1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Note that using speakers more resistive than 4-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier. θ_{JA} is a gross approximation of the complex thermal transfer mechanisms between the device and its ambient environment. If the θ_{JA} calculation reveals a potential problem, a more accurate estimate should be made. Please contact TI for further information.

WHEN TO USE AN OUTPUT FILTER

Design the TPA2032D1 without an output filter if the traces from the amplifier to the speaker are short. Wireless handsets and PDAs are great applications for this class-D amplifier to be used without an output filter.

The TPA2032D1 passed FCC- and CE-radiated emissions testing with no shielding with speaker trace wires 100 mm long or less. For longer speaker trace wires, a ferrite bead can often be used in the design if failing radiated emissions testing without an LC filter; and, the frequency-sensitive circuit is greater than 1 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies. The selection must also take into account the currents flowing through the ferrite bead. Ferrites can begin to lose effectiveness at much lower than rated current values. Please see the EVM User's Guide for components used successfully by TI.

Figure 40 shows a typical ferrite-bead output filter.

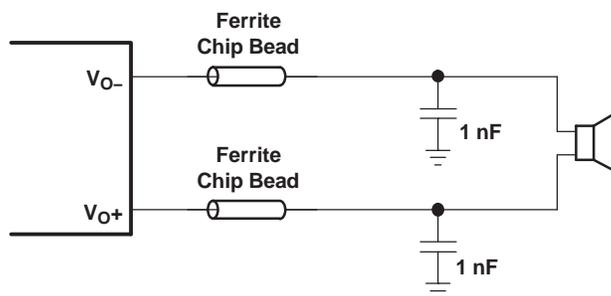
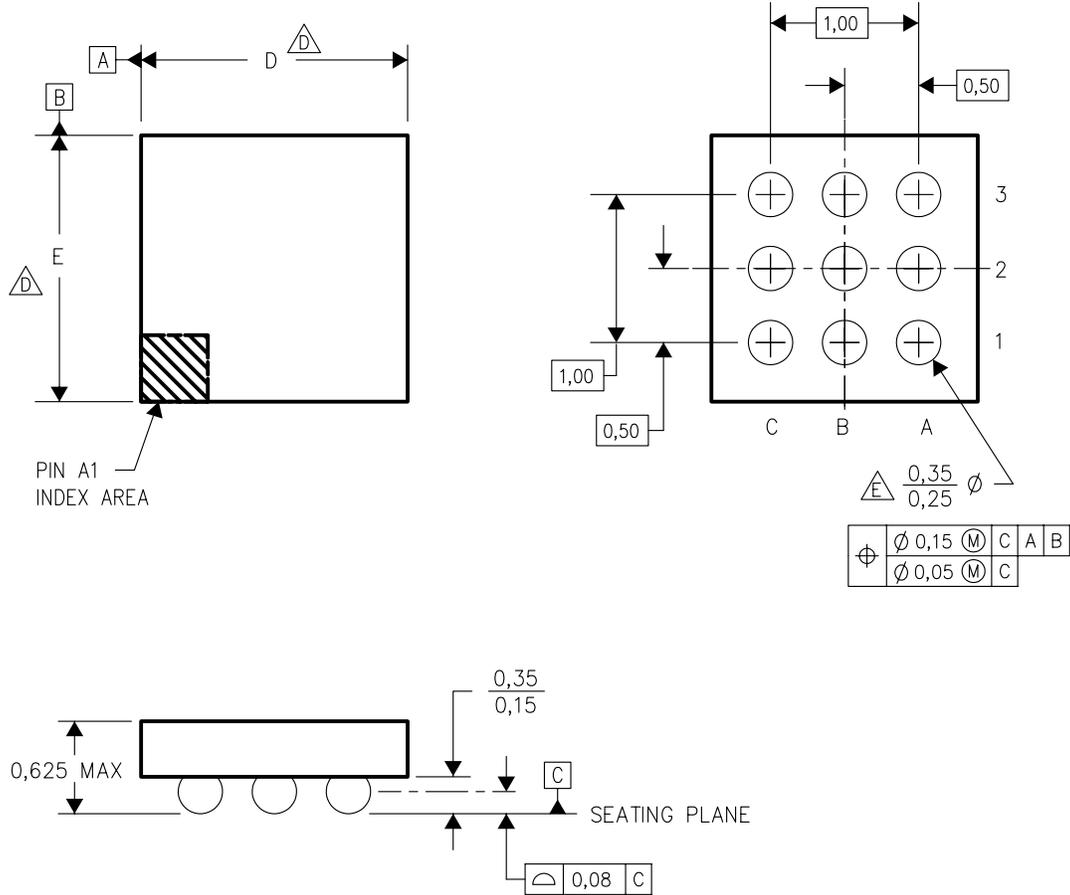


Figure 40. Typical Ferrite Chip Bead Filter

YZF (S-XBGA-N9)

DIE-SIZE BALL GRID ARRAY



4205058-3/D 10/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - Δ Devices in YZF package can have dimension D ranging from 1.35 to 2.15 mm and dimension E ranging from 1.35 to 2.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
 - E. Reference Product Data Sheet for array population. 3 x 3 matrix pattern is shown for illustration only.
 - F. This package contains lead-free balls. Refer to YEF (Drawing #4204181) for tin-lead (SnPb) balls.

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