MC9S12E-Family
Device User Guide
V01.04

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Motorola, Inc.

Revision History

Version Number	Revision Date	Author	Description of Changes
01.00	04.APR.03		Original Version.
01.01	24.JUN.03		Minor typo corrections.
01.02	9.OCT.03		MC9S12E32 added.
01.03	31.OCT.03		Added Colpitts and Pierce connections to 2.3.8. Updated input capacitance. Updated Table A-8. Changed pin name ROMONE to ROMCTL. Added S12 LRAE to Flash section. Added EXTAL VIH and VIL min/max values and hysteresis value to Oscillator Characteristics. New wording on NVM Reliability.
01.04	04.NOV.03		Updated PCB layouts. Changed PP6 to PK7 on Table 4-1. Updated DAC Supply min voltage and Operating frequency. Added Non-multiplexed Address and Chip Select external bus timing.

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Preface

The Device User Guide provides information about the MC9S12E-Family devices made up of standard HCS12 blocks and the HCS12 processor core. This document is part of the customer documentation. A complete set of device manuals also includes all the individual Block Guides of the implemented modules. In a effort to reduce redundancy, all module specific information is located only in the respective Block Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-1** for names and versions of the referenced documents throughout the Device User Guide.

Table 0-1 Document References

Block Guide	E256 Version	E128, E64 Version	E32 Version	Document Order Number
CPU12 Reference Manual	V02	V02	V02	S12CPUV2/D
HCS12 Background Debug (BDM)	V04	V04	V04	S12BDMV4/D
HCS12 Debug (DBG)	V01	V01	V01	S12DBGV1/D
HCS12 Interrupt (INT)	V01	V01	V01	S12INTV1/D
HCS12 Multiplexed Expanded Bus Interface (MEBI)	V03	V03	V03	S12MEBIV3/D
HCS12 Module Mapping Control (MMC)	V04	V04	V04	S12MMCV4/D
Analog to Digital Converter: 10-Bit, 16 Channels (ATD_10B16C)	V04	V02	V04	S12ATD10B16CVx/D[1]
Clock and Reset Generator (CRG)	V04	V04	V04	S12CRGV4/D
Digital to Analog Converter: 8-Bit, 1 Channel (DAC_8B1C)	V01	V01	V01	S12DAC8B1CV1/D
256Kbyte Flash EEPROM (FTS256K2)	V01	N/A	N/A	S12FTS256K2V1/D
128Kbyte Flash EEPROM (FTS128K1)	N/A	V01	N/A	S12FTS128K1V1/D
32Kbyte Flash EEPROM (FTS32K)	N/A	N/A	V02	S12FTS32KV2/D
Inter IC Bus (IIC)	V02	V02	V02	S12IICV2/D
Oscillator (OSC)	V02	V02	V02	S12OSCV2/D
Port Integration Module (PIM_9E128)	V01	V01	V01	S12PIM9E128V1/D
Pulse Modulator with Fault Protection: 15-Bit, 6 Channels (PMF_15B6C)	V02	V02	V02	S12PMF15B6CV2/D
Pulse Width Modulator: 8-Bit, 6 Channels (PWM_8B6C)	V01	V01	V01	S12PWM8B6CV1/D
Serial Communications Interface (SCI)	V04	V03	V04	S12SCIVy/D[2]
Serial Peripheral Interface (SPI)	V03	V03	V03	S12SPIV3/D
Timer: 16-Bit, 4 Channels (TIM_16B4C)	V01	V01	V01	S12TIM16B4CV1/D
Voltage Regulator (VREG_3V3)	V02	V02	V02	S12VREG3V3V2/D

NOTES:
1. x in S12ATD10B16CVx/D is 2 for E64 and E128, and 4 for E32 and E256.
2. y in S12SCIVy/D is 3 for E64 and E128, and 4 for E32 and E256.

Part Number

Figure 0-1 provides an ordering number example.

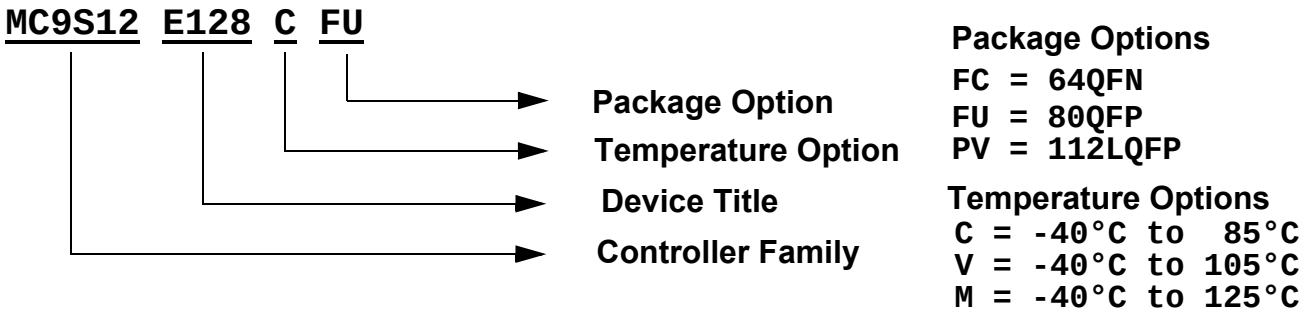


Figure 0-1 Order Part Number Coding

Table 0-2 lists the part number coding based on the package and temperature.

Table 0-2 Part Number Coding

Part Number	Temp.	Package	Description
MC9S12E256CFU	-40°C, 85°C	80QFP	MC9S12E256
MC9S12E256CPV	-40°C, 85°C	112LQFP	MC9S12E256
MC9S12E256MFU	-40°C, 125°C	80QFP	MC9S12E256
MC9S12E256MPV	-40°C, 125°C	112LQFP	MC9S12E256
MC9S12E128CFU	-40°C, 85°C	80QFP	MC9S12E128
MC9S12E128CPV	-40°C, 85°C	112LQFP	MC9S12E128
MC9S12E128MFU	-40°C, 125°C	80QFP	MC9S12E128
MC9S12E128MPV	-40°C, 125°C	112LQFP	MC9S12E128
MC9S12E64CFU	-40°C, 85°C	80QFP	MC9S12E64
MC9S12E64CPV	-40°C, 85°C	112LQFP	MC9S12E64
MC9S12E64MFU	-40°C, 125°C	80QFP	MC9S12E64
MC9S12E64MPV	-40°C, 125°C	112LQFP	MC9S12E64
MC9S12E32CFU	-40°C, 85°C	80QFP	MC9S12E32
MC9S12E32MFU	-40°C, 125°C	80QFP	MC9S12E32

Table 0-3 summarizes the package option and size configuration.

Table 0-3 Package Option Summary

Package	Device	Part Number	Temp.[1] Options	Flash	RAM	I/O[2]
80QFP	MC9S12E256	MC9S12E256	M, C	256K	16K	60
112LQFP	MC9S12E256	MC9S12E256	M, C			92
80QFP	MC9S12E128	MC9S12E128	M, C	128K	8K	60
112LQFP	MC9S12E128	MC9S12E128	M, C			92
80QFP	MC9S12E64	MC9S12E64	M, C	64K	4K	60
112LQFP	MC9S12E64	MC9S12E64	M, C			92
64QFN	MC9S12E32	MC9S12E32	M, C	32K	2K	44
80QFP	MC9S12E32	MC9S12E32	M, C			60

NOTES:
1. C: T_A = 85¯C, f = 25MHz. M: T_A= 125¯C, f = 25MHz
2. I/O is the sum of ports capable to act as digital input or output.

Table 0-4 List of MC9S12E-Family members

Device	Flash	RAM	Package	MEBI	TIM	SCI	SPI	IIC	A/D	D/A	PWM	PMF	KWU	I/O
E256	256K	16K	112 LQFP	1	12	3	1	1	16	2	6	6	16	92
			80 QFP	0										60
E128	128K	8K	112 LQFP	1	12	3	1	1	16	2	6	6	16	92
			80 QFP	0										60
E64	64K	4K	112 LQFP	1	12	3	1	1	16	2	6	6	16	92
			80 QFP	0										60
E32	32K	2K	80 QFP	0	8	2	1	1	16	2	0	6	16	60

• Pin out explanations:
— TIM is the number of channels.
— A/D is the number of A/D channels.
— D/A is the number of D/A channels.
— PWM is the number of channels.
— PMF is the number of channels.
— KWU is the number of key wake up interrupt pins.
— I/O is the sum of ports capable to act as digital input or output.
112 Pin Packages:
Port A = 8, B = 8, E = 6 + 2 input only, K = 8, M = 7, P = 6, Q = 7,
S = 8, T = 8, U = 8, AD = 16.
18 inputs provide Interrupt capability (AD = 16, IRQ, XIRQ)
80 Pin Packages:
E = 2 + 2 input only, M = 7, P = 6, Q = 7,
S = 8, T = 8, U = 4, AD = 16.
18 inputs provide Interrupt capability (AD = 16, IRQ, XIRQ)
— Versions with 3 SCI modules will have SCI0, SCI1 and SCI2.
— Versions with 2 SCI modules will have SCI0 and SCI1.
— Versions with 3 TIM modules will have TIM0, TIM1 and TIM2.
— Versions with 2 TIM modules will have TIM0 and TIM1.

Section 1 Introduction

1.1 Overview

The MC9S12E-Family is a 112/80 pin low cost general purpose MCU family. All members of the MC9S12E-Family are comprised of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), up to 256K bytes of Flash EEPROM, up to 16K bytes of RAM, three asynchronous serial communications interface modules (SCI), a serial peripheral interface (SPI), an Inter-IC Bus (IIC), three 4-channel 16-bit timer modules (TIM), a 6-channel 15-bit Pulse Modulator with Fault protection module (PMF), a 6-channel 8-bit Pulse Width Modulator (PWM), a 16-channel 10-bit analog-to-digital converter (ADC), and two 1-channel 8-bit digital-to-analog converters (DAC). The MC9S12E-Family has full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available on each module, 16 dedicated I/O port bits are available with Wake-Up capability from STOP or WAIT mode. Furthermore, an on chip bandgap based voltage regulator (VREG) generates the internal digital supply voltage of 2.5V (VDD) from a 3.135V to 5.5V external supply range.

1.2 Features

- 16-bit HCS12 CORE
  - HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer's model identical to M68HC11
    iii. Instruction queue
    iv. Enhanced indexed addressing
  - Module Mapping Control (MMC)
  - Interrupt Control (INT)
  - Background Debug Module (BDM)
  - Debugger (DBG12) including breakpoints and change-of-flow trace buffer
  - Multiplexed External Bus Interface (MEBI)
- Wake-Up interrupt inputs
  - Up to 16 port bits available for wake up interrupt function with digital filtering
- Memory options
  - 32K, 64K, 128K or 256K Byte Flash EEPROM
  - 2K, 4K, 8K or 16K Byte RAM
- Two 1-channel Digital-to-Analog Converters (DAC)
  - 8-bit resolution

- Analog-to-Digital Converter (ADC)
  - 16-channel module with 10-bit resolution
  - External conversion trigger capability
- Three 4-channel Timers (TIM)
  - Programmable input capture or output compare channels
  - Simple PWM mode
  - Counter Modulo Reset
  - External Event Counting
  - Gated Time Accumulation
- 6 PWM channels (PWM)
  - Programmable period and duty cycle
  - 8-bit 6-channel or 16-bit 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- 6-channel Pulse width Modulator with Fault protection (PMF)
  - Three independent 15-bit counters with synchronous mode
  - Complementary channel operation
  - Edge and center aligned PWM signals
  - Programmable dead time insertion
  - Integral reload rates from 1 to 16
  - Four fault protection shut down input pins
  - Three current sense input pins
- Serial interfaces
  - Three asynchronous serial communication interfaces (SCI)
  - Synchronous serial peripheral interface (SPI)
  - Inter-IC Bus (IIC)
- Clock and Reset Generator (CRG)
  - Windowed COP watchdog
  - Real Time interrupt
  - Clock Monitor

  - Pierce or low current Colpitts oscillator
  - Phase-locked loop clock frequency multiplier
  - Self Clock mode in absence of external clock
  - Low power 0.5 to 16Mhz crystal oscillator reference clock
- Operating frequency
  - 50MHz equivalent to 25MHz Bus Speed
- Internal 2.5V Regulator
  - Input voltage range from 3.135V to 5.5V
  - Low power mode capability
  - Includes low voltage reset (LVR) circuitry
  - Includes low voltage interrupt (LVI) circuitry
- 112-Pin LQFP or 80-Pin QFP package
  - Up to 90 I/O lines with 5V input and drive capability (112 pin package)
  - Up to two dedicated 5V input only lines (IRQ and XIRQ)
  - Sixteen 3.3V/5V A/D converter inputs
- Development Support.
  - Single-wire background debug^{TM} mode
  - On-chip hardware breakpoints
  - Enhanced debug features

1.3 Modes of Operation

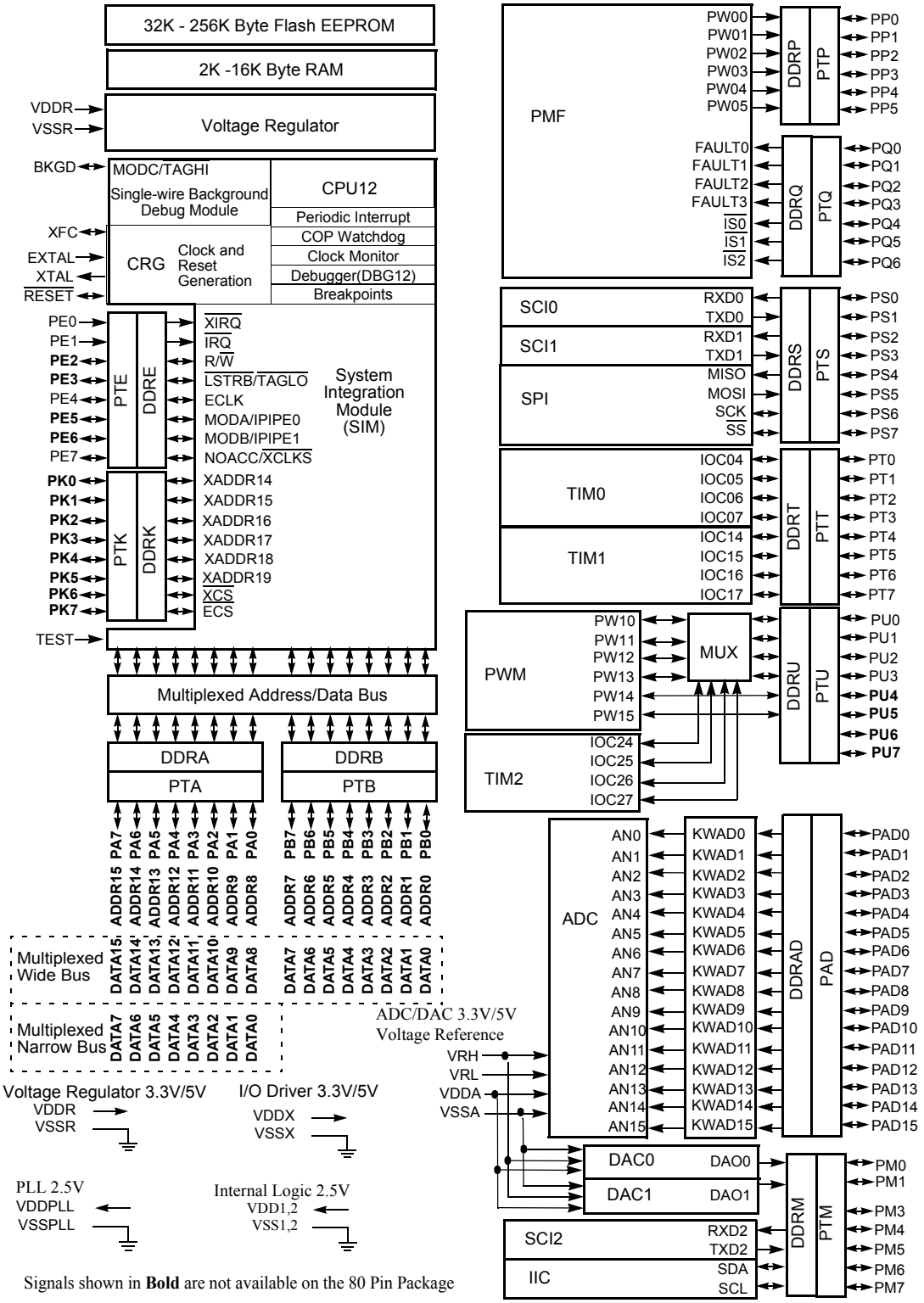
User modes **(Expanded modes are only available in the 112 pin package version)**

- Normal modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode **(Motorola use only)**
  - Special Peripheral Mode **(Motorola use only)**

- Low power modes
  - Stop Mode
  - Pseudo Stop Mode
  - Wait Mode

1.4 Block Diagram

Figure 1-1 MC9S12E-Family Block Diagram



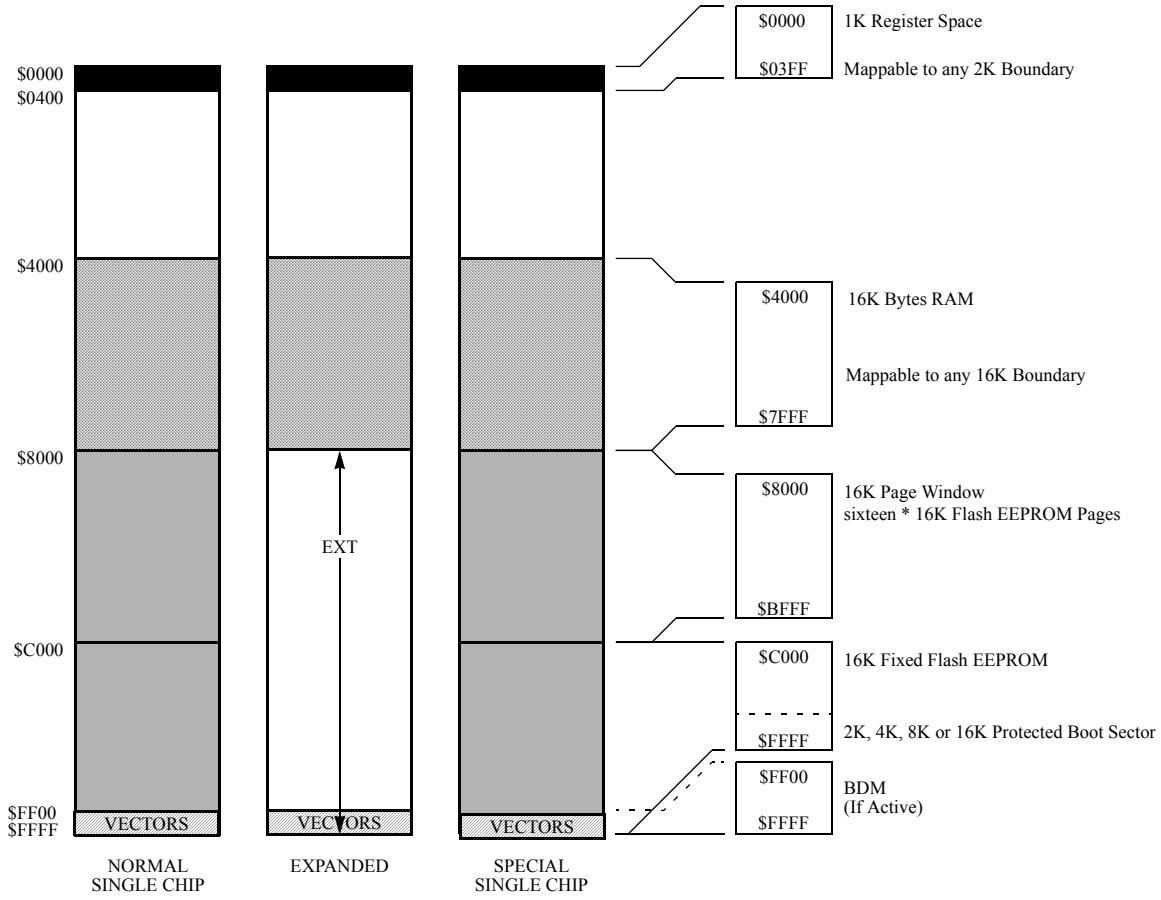
Signals shown in **Bold** are not available on the 80 Pin Package

1.5 Device Memory Map

Table 1-1 shows the device register map of the MC9S12E-Family after reset. The following figures (, **Figure 1-3**, and **Figure 1-4**) illustrate the full device memory map with Flash and RAM.

Table 1-1 Device Register Map Overview

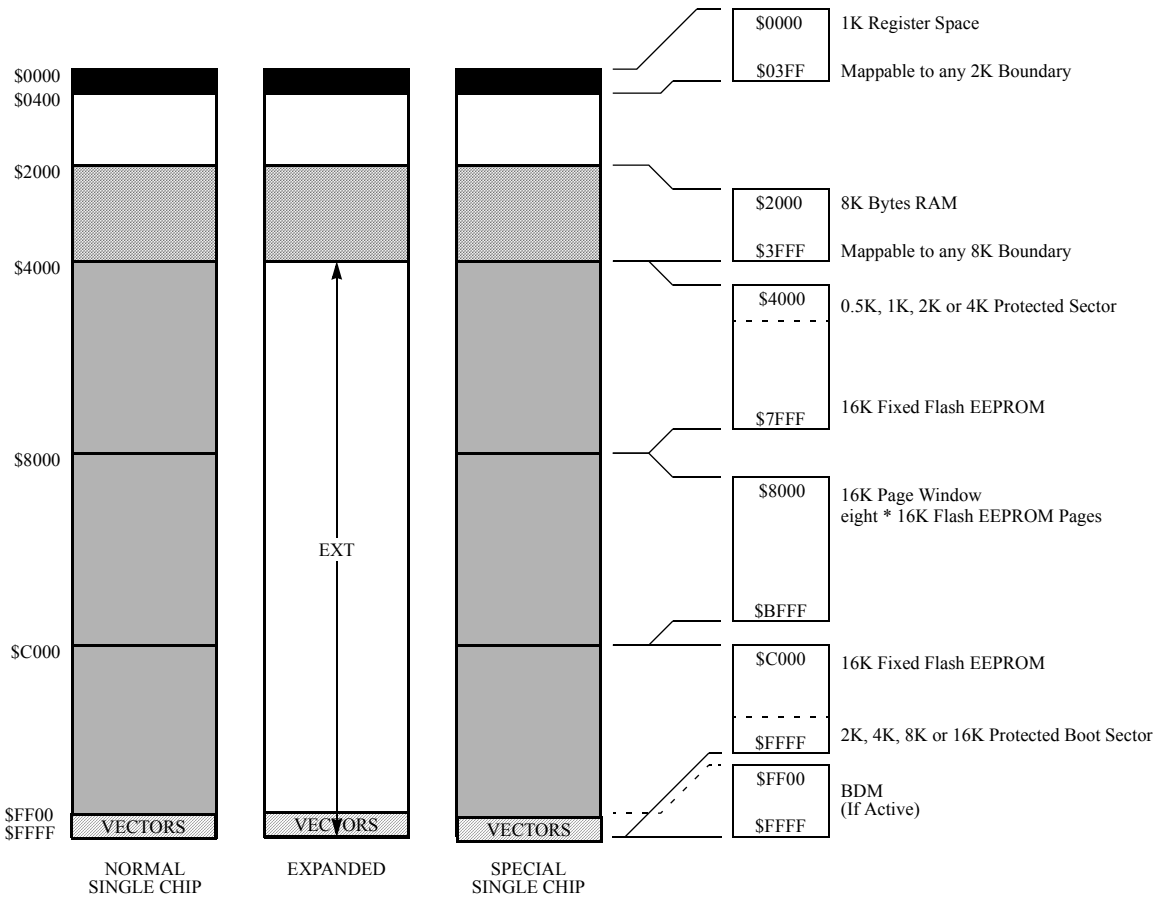
Address	Module	Size
$000 - $017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$018	Reserved	1
$019	Voltage Regulator (VREG)	1
$01A - $01B	Device ID register (PARTID)	2
$01C - $01F	CORE (MEMSIZ, IRQ, HPRIO)	4
$020 - $02F	CORE (DBG)	16
$030 - $033	CORE (PPAGE, Port K)	4
$034 - $03F	Clock and Reset Generator (PLL, RTI, COP)	12
$040 - $06F	Standard Timer 16-bit 4 channels (TIM0)	48
$070 - $07F	Reserved	16
$080 - $0AF	Analog to Digital Converter 10-bit 16 channels (ATD)	48
$0B0 - $0C7	Reserved	24
$0C8 - $0CF	Serial Communications Interface 0 (SCI0)	8
$0D0 - $0D7	Serial Communications Interface 1 (SCI1)	8
$0D8 - $0DF	Serial Peripheral Interface (SPI)	8
$0E0 - $0E7	Inter IC Bus	8
$0E8 - $0EF	Serial Communications Interface 2 (SCI2)	8
$0F0 - $0F3	Digital to Analog Converter 8-bit 1-channel (DAC0)	4
$0F4 - $0F7	Digital to Analog Converter 8-bit 1-channel (DAC1)	4
$0F8 - $0FF	Reserved	8
$100- $10F	Flash Control Register	16
$110 - $13F	Reserved	48
$140 - $16F	Standard Timer 16-bit 4 channels (TIM1)	48
$170 - $17F	Reserved	16
$180 - $1AF	Standard Timer 16-bit 4 channels (TIM2)	48
$1B0 - $1DF	Reserved	48
$1E0 - $1FF	Pulse Width Modulator 8-bit 6 channels (PWM)	32
$200 - $23F	Pulse Width Modulator with Fault 15-bit 6 channels (PMF)	64
$240 - $27F	Port Integration Module (PIM)	64
$280 - $3FF	Reserved	384



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $3FFF: 16K RAM (only 15K RAM visible $0400 - $3FFF)

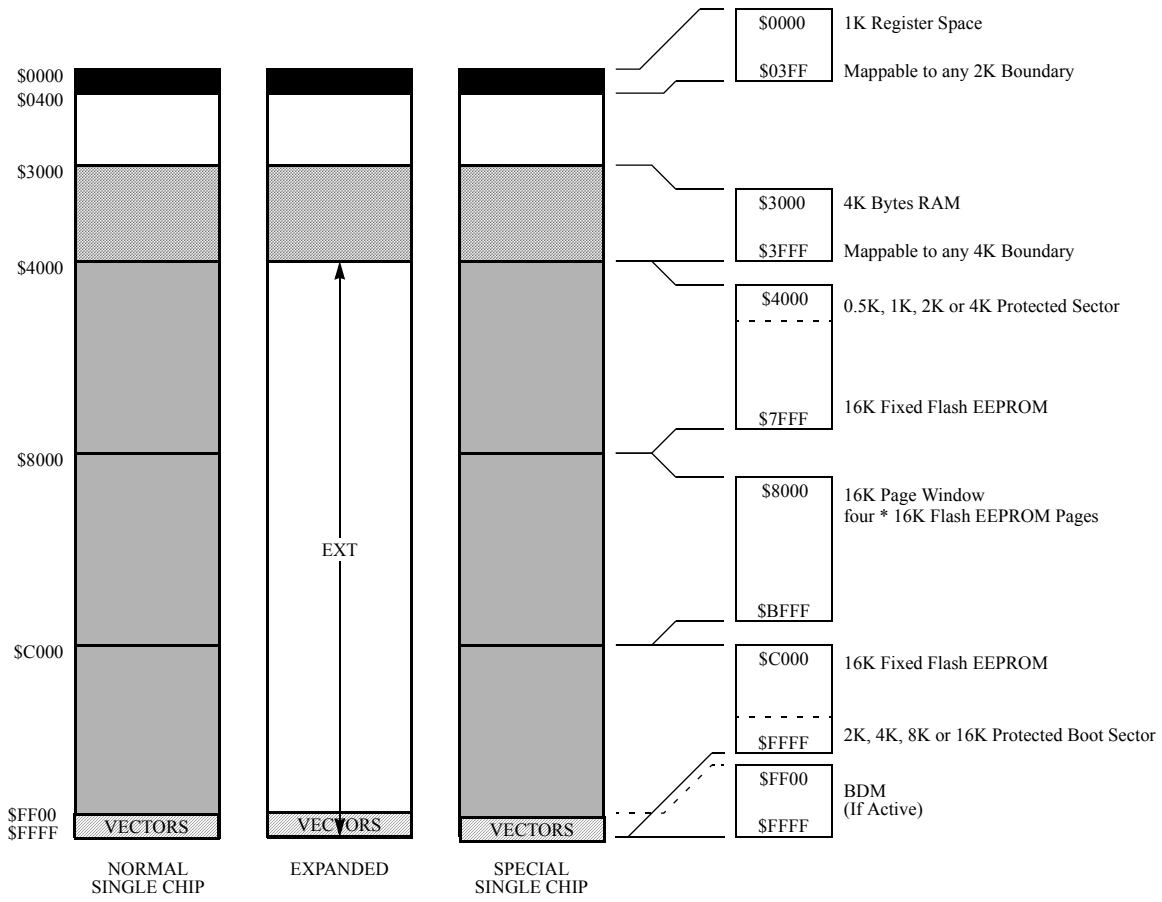
Figure 1-2 MC9S12E256 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $1FFF: 8K RAM (only 7K RAM visible $0400 - $1FFF)

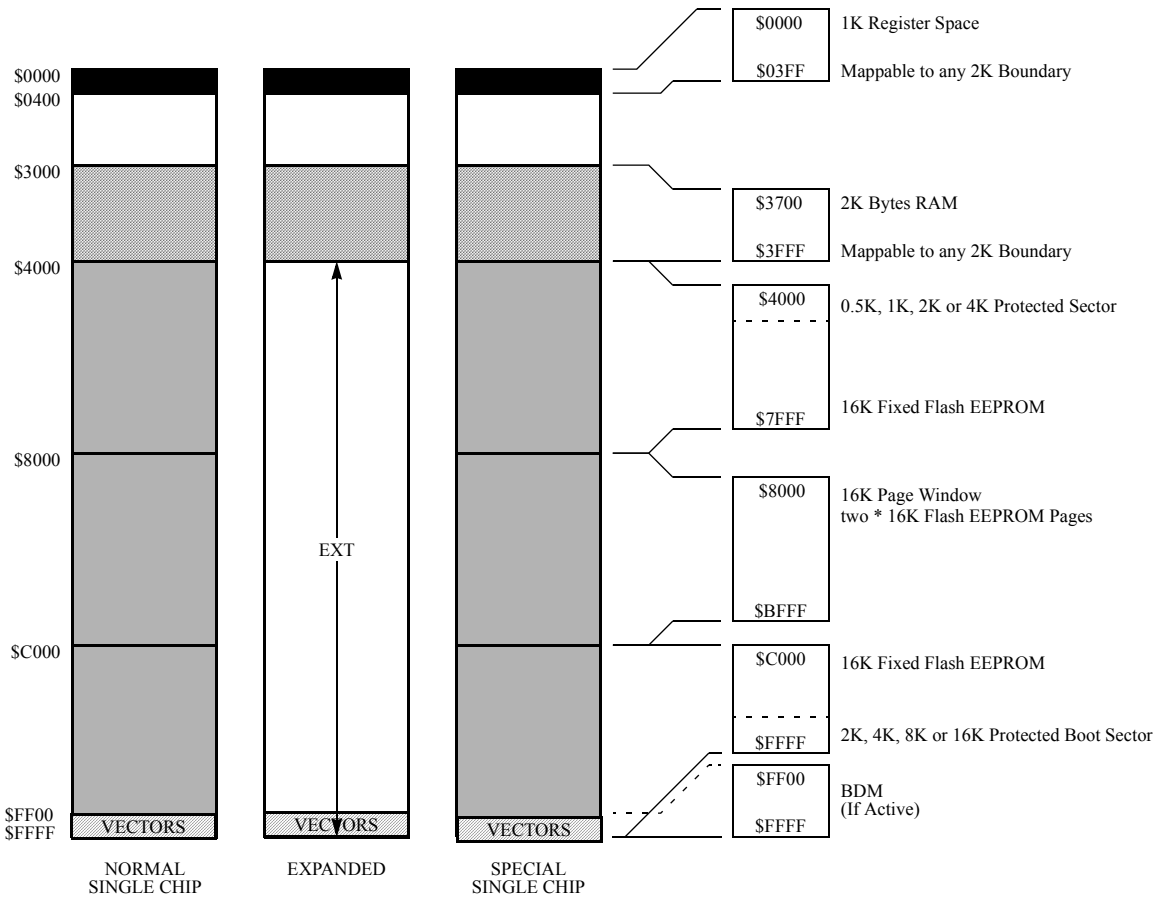
Figure 1-3 MC9S12E128 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $0FFF: 4K RAM (only 3K RAM visible $0400 - $0FFF)

Figure 1-4 MC9S12E64 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $07FF: 2K RAM (only 1K RAM visible $0400 - $07FF)

Figure 1-5 MC9S12E32 User configurable Memory Map

1.6 Detailed Register Map

The detailed register map of the MC9S12E-Family is listed in address order below. For detailed information about register function please refer to the appropriate block guide.

$0000 - $000F **MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0000	PORTA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0001	PORTB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0002	DDRA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0003	DDRB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0004	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0005	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0006	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0007	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0008	PORTE	Read:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
		Write:								
$0009	DDRE	Read:	Bit 7	6	5	4	3	Bit 2	0	0
		Write:								
$000A	PEAR	Read:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								

$0000 - $000F MEBI map 1 of 3 (HCS12 Multiplexed External Bus Interface)

$000B	MODE	Read:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
		Write:								
$000C	PUCR	Read:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
		Write:								
$000D	RDRIV	Read:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		Write:								
$000E	EBICTL	Read:	0	0	0	0	0	0	0	ESTR
		Write:								
$000F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0010 - $0014 MMC map 1 of 4 (HCS12 Module Mapping Control)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0010	INITRM	Read:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
		Write:								
$0011	INITRG	Read:	0	REG14	REG13	REG12	REG11	0	0	0
		Write:								
$0012	INITEE	Read:	EE15	EE14	EE13	EE12	EE11	0	0	EEON
		Write:								
$0013	MISC	Read:	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
		Write:								
$0014	MTST0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0015 - $0016 INT map 1 of 2 (HCS12 Interrupt)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0015	ITCR	Read:	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:								
$0016	ITEST	Read:	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write:								

$0017 - $0017 MMC map 2 of 4 (HCS12 Module Mapping Control)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0017	MTST1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0018 - $0018 Miscellaneous Peripherals (Device User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0018	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0019 - $0019 VREG3V3 (Voltage Regulator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0019	VREGCTRL	Read:	0	0	0	0	0	LVDS	LVIE	LVIF
		Write:								

$001A - $001B Miscellaneous Peripherals (Device User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001A	PARTIDH	Read:	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:								
$001B	PARTIDL	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								

$001C - $001D MMC map 3 of 4 (HCS12 Module Mapping Control, Device User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001C	MEMSIZ0	Read:	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:								
$001D	MEMSIZ1	Read:	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:								

$001E - $001E MEBI map 2 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001E	INTCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:								

$001F - $001F INT map 2 of 2 (HCS12 Interrupt)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001F	HPRIO	Read:	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:								

$0020 - $002F DBG (including BKP) map 1of 1 (HCS12 Debug)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0020	DBGC1	read	DBGEN	ARM	TRGSEL	BEGIN	DBGBRK	0	CAPMOD	
		write								
$0021	DBGSC	read	AF	BF	CF	0	TRG			
		write								
$0022	DBGTBH	read	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		write								
$0023	DBGTBL	read	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		write								
$0024	DBGCNT	read	TBF	0	CNT					
		write								
$0025	DBGCCX	read	PAGSEL		EXTCMP					
		write								
$0026	DBGCCH	read	Bit 15	14	13	12	11	10	9	Bit 8
		write								
$0027	DBGCCL	read	Bit 7	6	5	4	3	2	1	Bit 0
		write								
$0028	DBGC2 BKPCT0	read	BKABEN	FULL	BDM	TAGAB	BKCEN	TAGC	RWCEN	RWC
		write								
$0029	DBGC3 BKPCT1	read	BKAMBH	BKAMBL	BKBMBH	BKBMBL	RWAEN	RWA	RWBEN	RWB
		write								
$002A	DBGCAX BKP0X	read	PAGSEL		EXTCMP					
		write								
$002B	DBGCAH BKP0H	read	Bit 15	14	13	12	11	10	9	Bit 8
		write								
$002C	DBGCAL BKP0L	read	Bit 7	6	5	4	3	2	1	Bit 0
		write								
$002D	DBGCBX BKP1X	read	PAGSEL		EXTCMP					
		write								
$002E	DBGCBH BKP1H	read	Bit 15	14	13	12	11	10	9	Bit 8
		write								
$002F	DBGCBL BKP1L	read	Bit 7	6	5	4	3	2	1	Bit 0
		write								

$0030 - $0031 MMC map 4 of 4 (HCS12 Module Mapping Control)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0030	PPAGE	Read:	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
		Write:								
$0031	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0032 - $0033 MEBI map 3 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0032	PORTK	Read: Write:	ECS	XCS	XAB19	XAB18	XAB17	XAB16	XAB15	XAB14
$0033	DDRK	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0034 - $003F CRG (Clock and Reset Generator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0034	SYNR	Read:	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
		Write:								
$0035	REFDV	Read:	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
		Write:								
$0036	CTFLG TEST ONLY	Read:	TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0
		Write:								
$0037	CRGFLG	Read:	RTIF	PROF	0	LOCKIF	LOCK	TRACK	SCMIF	SCM
		Write:								
$0038	CRGINT	Read:	RTIE	0	0	LOCKIE	0	0	SCMIE	0
		Write:								
$0039	CLKSEL	Read:	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
		Write:								
$003A	PLLCTL	Read:	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
		Write:								
$003B	RTICTL	Read:	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		Write:								

$0034 - $003F CRG (Clock and Reset Generator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$003C	COPCTL	Read:	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		Write:								
$003D	FORBYP TEST ONLY	Read:	RTIBYP	COPBYP	0	PLLBYP	0	0	FCM	0
		Write:								
$003E	CTCTL TEST ONLY	Read:	TCTL7	TCTL6	TCTL5	TCTL4	TCLT3	TCTL2	TCTL1	TCTL0
		Write:								
$003F	ARMCOP	Read:	0	0	0	0	0	0	0	0
		Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0040 - $006F TIM0 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0040	TIOS	Read:	IOS7	IOS6	IOS5	IOS4	0	0	0	0
		Write:								
$0041	CFORC	Read:	0	0	0	0	0	0	0	0
		Write:	FOC7	FOC6	FOC5	FOC4				
$0042	OC7M	Read:	OC7M7	OC7M6	OC7M5	OC7M4	0	0	0	0
		Write:								
$0043	OC7D	Read:	OC7D7	OC7D6	OC7D5	OC7D4	0	0	0	0
		Write:								
$0044	TCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0045	TCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0040 - $006F TIM0 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0046	TSCR1	Read:	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
		Write:								
$0047	TTOV	Read:	TOV7	TOV6	TOV5	TOV4	0	0	0	0
		Write:								
$0048	TCTL1	Read:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		Write:								
$0049	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$004A	TCTL3	Read:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		Write:								
$004B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$004C	TIE	Read:	C7I	C6I	C5I	C4I	0	0	0	0
		Write:								
$004D	TSCR2	Read:	TOI	0	0	0	TCRE	PR2	PR1	PR0
		Write:								
$004E	TFLG1	Read:	C7F	C6F	C5F	C4F	0	0	0	0
		Write:								
$004F	TFLG2	Read:	TOF	0	0	0	0	0	0	0
		Write:								
$0050	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0040 - $006F TIM0 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0051	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0052	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0053	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0054	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0055	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0056	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0057	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0058	TC4 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0059	TC4 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005A	TC5 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005B	TC5 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0040 - $006F TIM0 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$005C	TC6 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005D	TC6 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005E	TC7 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005F	TC7 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0060	PACTL	Read:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		Write:								
$0061	PAFLG	Read:	0	0	0	0	0	0	PAOVF	PAIF
		Write:								
$0062	PACNT (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0063	PACNT (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0064	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0065	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0066	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0040 - $006F TIM0 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0067	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0068	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0069	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0070 - $007F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0070 - $007F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATDCTL0	Read:	0	0	0	0	WRAP3[1]	WRAP2[1]	WRAP1[1]	WRAP0[1]
		Write:								
$0081	ATDCTL1	Read:	ETRIGSEL[2]	0	0	0	ETRIGCH3[2]	ETRIGCH2[2]	ETRIGCH1[2]	ETRIGCH0[2]
		Write:								
$0082	ATDCTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0083	ATDCTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0084	ATDCTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0085	ATDCTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
$0086	ATDSTAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$0087	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0088	ATDTEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0089	ATDTEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$008A	ATDSTAT0	Read:	CCF15	CCF14	CCF13	CCF12	CCF11	CCF10	CCF9	CCF8
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$008B	ATDSTAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$008C	ATDDIEN0	Read:	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8
		Write:								
$008D	ATDDIEN1	Read:	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
		Write:								
$008E	PORTAD0	Read:	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
		Write:								
$008F	PORTAD1	Read:	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
		Write:								
$0090	ATDDR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0091	ATDDR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0092	ATDDR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0093	ATDDR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0094	ATDDR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0095	ATDDR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0096	ATDDR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0097	ATDDR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0098	ATDDR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0099	ATDDR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009A	ATDDR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009B	ATDDR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009C	ATDDR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009D	ATDDR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009E	ATDDR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009F	ATDDR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A0	ATDDR8H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00A1	ATDDR8L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A2	ATDDR9H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A3	ATDDR9L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A4	ATDDR10H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A5	ATDDR10L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A6	ATDDR11H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A7	ATDDR11L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00A8	ATDDR12H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A9	ATDDR12L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00AA	ATDDR13H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AB	ATDDR13L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00AC	ATDDR14H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AD	ATDDR14L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$00AE	ATDDR15H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AF	ATDDR15L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

NOTES:
1. WRAP0-3 bits are available in version V04 of ATD10B16C
2. ETRIGSEL and ETRIGCH0-3 bits are available in version V04 of ATD10B16C

$00B0 - $00C7 Reserved

$00B0 - $00C7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00C8 - $00CF SCI0 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C8	SCIBDH	Read: Write:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
$00C9	SCIBDL	Read: Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
$00CA	SCICR1	Read: Write:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT

$00C8 - $00CF SCI0 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00CB	SCICR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$00CC	SCISR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$00CD	SCISR2	Read:	0	0	0	TXPOL[1]	RXPOL[1]	BRK13	TXDIR	RAF
		Write:								
$00CE	SCIDRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00CF	SCIDRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

NOTES:
1. TXPOL and RXPOL bits are available in version V04 of SCI

$00D0 - $00D7 SCI1 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D0	SCIBDH	Read:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00D1	SCIBDL	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$00D2	SCICR1	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$00D3	SCICR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								

$00D0 - $00D7 SCI1 (Asynchronous Serial Interface)

$00D4	SCISR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$00D5	SCISR2	Read:	0	0	0	TXPOL[1]	RXPOL[1]	BRK13	TXDIR	RAF
		Write:								
$00D6	SCIDRH	Read:	R8	T8		0	0	0	0	0
		Write:								
$00D7	SCIDRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

NOTES:
1. TXPOL and RXPOL are available in version V04 of SCI

$00D8 - $00DF SPI (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D8	SPICR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
$00D9	SPICR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
$00DA	SPIBR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
$00DB	SPISR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
$00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00D8 - $00DF SPI (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00DD	SPIDR	Read: Write:	Bit7	6	5	4	3	2	1	Bit0
$00DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E0 - $00E7 IIC (Inter-IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E0	IBAD	Read:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		Write:								
$00E1	IBFD	Read: Write:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
$00E2	IBCR	Read:	IBEN	IBIE	MS/$\overline{SL}$	Tx/$\overline{Rx}$	TXAK	0	0	IBSWAI
		Write:						RSTA		
$00E3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
$00E4	IBDR	Read: Write:	D7	D6	D5	D4	D3	D2	D1	D0

$00E0 - $00E7 IIC (Inter-IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E8 - $00EF SCI2 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E8	SCIBDH	Read:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00E9	SCIBDL	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$00EA	SCICR1	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$00EB	SCICR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$00EC	SCISR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								

$00E8 - $00EF SCI2 (Asynchronous Serial Interface)

$00ED	SCISR2	Read:	0	0	0	TXPOL[1]	RXPOL[1]	BRK13	TXDIR	RAF
		Write:								
$00EE	SCIDRH	Read:	R8	T8		0	0	0	0	0
		Write:								
$00EF	SCIDRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

NOTES:
1. TXPOL and RXPOL are available in version V04 of SCI

$00F0 - $00F3 DAC0 (Digital-to-Analog Converter)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00F0	DACC0	Read:	DACE	DACTE	0	0	DJM	DSGN	DACWAI	DACOE
		Write:								
$00F1	DACC1	Read:	0	0	0	0	0	0	0	0
		Write:								
$00F2	DACD	Read:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		Write:								
$00F3	DACD	Read:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		Write:								

$00F4 - $00F7 DAC1 (Digital-to-Analog Converter)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00F4	DACC0	Read:	DACE	DACTE	0	0	DJM	DSGN	DACWAI	DACOE
		Write:								
$00F5	DACC1	Read:	0	0	0	0	0	0	0	0
		Write:								
$00F6	DACD	Read:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		Write:								
$00F7	DACD	Read:	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		Write:								

$00F8 - $00FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00F8 - $00FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0100 - $010F Flash Control Register

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0100	FCLKDIV	Read:	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		Write:								
$0101	FSEC	Read:	KEYEN 1	NV6	NV5	NV4	NV3	NV2	SEC1	SEC0
		Write:								
$0102	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								

$0100 - $010F Flash Control Register

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0103	FCNFG	Read:	CBEIE	CCIE	KEYACC	0	0	0	0	0
		Write:								
$0104	FPROT	Read:	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		Write:								
$0105	FSTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0106	FCMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0107	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0108	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0109	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$010A	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$010B	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$010C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0100 - $010F Flash Control Register

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$010D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$010E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$010F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0110 - $013F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0110 - $013F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0140 - $016F TIM1 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0140	TIOS	Read:	IOS7	IOS6	IOS5	IOS4	0	0	0	0
		Write:								
$0141	CFORC	Read:	0	0	0	0	0	0	0	0
		Write:	FOC7	FOC6	FOC5	FOC4				
$0142	OC7M	Read:	OC7M7	OC7M6	OC7M5	OC7M4	0	0	0	0
		Write:								
$0143	OC7D	Read:	OC7D7	OC7D6	OC7D5	OC7D4	0	0	0	0
		Write:								
$0144	TCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								

$0140 - $016F TIM1 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0145	TCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0146	TSCR1	Read:	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
		Write:								
$0147	TTOV	Read:	TOV7	TOV6	TOV5	TOV4	0	0	0	0
		Write:								
$0148	TCTL1	Read:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		Write:								
$0149	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$014A	TCTL3	Read:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		Write:								
$014B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$014C	TIE	Read:	C7I	C6I	C5I	C4I	0	0	0	0
		Write:								
$014D	TSCR2	Read:	TOI	0	0	0	TCRE	PR2	PR1	PR0
		Write:								
$014E	TFLG1	Read:	C7F	C6F	C5F	C4F	0	0	0	0
		Write:								
$014F	TFLG2	Read:	TOF	0	0	0	0	0	0	0
		Write:								

$0140 - $016F TIM1 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0150	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0151	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0152	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0153	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0154	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0155	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0156	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0157	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0158	TC4 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0159	TC4 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$015A	TC5 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								

$0140 - $016F TIM1 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$015B	TC5 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$015C	TC6 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$015D	TC6 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$015E	TC7 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$015F	TC7 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0160	PACTL	Read:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		Write:								
$0161	PAFLG	Read:	0	0	0	0	0	0	PAOVF	PAIF
		Write:								
$0162	PACNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0163	PACNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0164	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0165	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0140 - $016F TIM1 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0166	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0167	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0168	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0169	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$016A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$016B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$016C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$016D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$016E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$016F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0170 - $017F Reserved

$0110 - $013F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0180 - $01AF TIM2 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0180	TIOS	Read:	IOS7	IOS6	IOS5	IOS4	0	0	0	0
		Write:								
$0181	CFORC	Read:	0	0	0	0	0	0	0	0
		Write:	FOC7	FOC6	FOC5	FOC4				
$0182	OC7M	Read:	OC7M7	OC7M6	OC7M5	OC7M4	0	0	0	0
		Write:								
$0183	OC7D	Read:	OC7D7	OC7D6	OC7D5	OC7D4	0	0	0	0
		Write:								
$0184	TCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0185	TCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0186	TSCR1	Read:	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
		Write:								
$0187	TTOV	Read:	TOV7	TOV6	TOV5	TOV4	0	0	0	0
		Write:								
$0188	TCTL1	Read:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		Write:								

$0180 - $01AF TIM2 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0189	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$018A	TCTL3	Read:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		Write:								
$018B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$018C	TIE	Read:	C7I	C6I	C5I	C4I	0	0	0	0
		Write:								
$018D	TSCR2	Read:	TOI	0	0	0	TCRE	PR2	PR1	PR0
		Write:								
$018E	TFLG1	Read:	C7F	C6F	C5F	C4F	0	0	0	0
		Write:								
$018F	TFLG2	Read:	TOF	0	0	0	0	0	0	0
		Write:								
$0190	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0191	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0192	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0193	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0180 - $01AF TIM2 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0194	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0195	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0196	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0197	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0198	TC4 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0199	TC4 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$015A	TC5 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$019B	TC5 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$019C	TC6 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$019D	TC6 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$019E	TC7 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								

$0180 - $01AF TIM2 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$019F	TC7 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$01A0	PACTL	Read:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		Write:								
$01A1	PAFLG	Read:	0	0	0	0	0	0	PAOVF	PAIF
		Write:								
$01A2	PACNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$01A3	PACNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$01A4	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01A5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01A6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01A7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01A8	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01A9	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0180 - $01AF TIM2 (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01AA	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01AB	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01AC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01AD	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01AE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01AF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$01B0 - $01DF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01B0 - $01DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$01E0 - $01FF PWM (Pulse Width Modulator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01E0	PWME	Read:	0	0	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		Write:								
$01E1	PWMPOL	Read:	0	0	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		Write:								
$01E2	PWMCLK	Read:	0	0	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		Write:								
$01E3	PWMPRCLK	Read:	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		Write:								
$01E4	PWMCAE	Read:	0	0	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		Write:								
$01E5	PWMCTL	Read:	0	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		Write:								
$01E6	PWMTST Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$01E7	PWMPRSC	Read:	0	0	0	0	0	0	0	0
		Write:								
$01E8	PWMSCLA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$01E9	PWMSCLB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$01EA	PWMSCNTA	Read:	0	0	0	0	0	0	0	0
		Write:								

$01E0 - $01FF PWM (Pulse Width Modulator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01EB	PWMSCNTB	Read:	0	0	0	0	0	0	0	0
		Write:								
$01EC	PWMCNT0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$01ED	PWMCNT1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$01EE	PWMCNT2	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$01EF	PWMCNT3	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$01F0	PWMCNT4	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$01F1	PWMCNT5	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$01F2	PWMPER0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01F3	PWMPER1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01F4	PWMPER2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01F5	PWMPER3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$01E0 - $01FF PWM (Pulse Width Modulator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01F6	PWMPER4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01F7	PWMPER5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01F8	PWMDTY0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01F9	PWMDTY1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01FA	PWMDTY2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01FB	PWMDTY3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01FC	PWMDTY4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01FD	PWMDTY5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$01FE	PWMSDN	Read:	PWMIF	PWMIE	0	PWMLVL	0	PWM5IN	PWM5INL	PWM5ENA
		Write:			PWMRSTRT					
$01FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0200 - $023F PMF (Pulse width Modulator with Fault protection)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0200	PMFCFG0	Read: Write:	WP	MTG	EDGEC	EDGEB	EDGEA	INDEPC	INDEPB	INDEPA
$0201	PMFCFG1	Read: Write:	ENHA	0	BOTNEGC	TOPNEGC	BOTNEGB	TOPNEGB	BOTNEGA	TOPNEGA
$0202	PMFCFG2	Read: Write:	0	0	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0
$0203	PMFCFG3	Read: Write:	PMFWAI	PMFFRZ	0	VLMODE		SWAPC	SWAPB	SWAPA
$0204	PMFFCTL	Read: Write:	FMODE3	FIE3	FMODE2	FIE2	FMODE1	FIE1	FMODE0	FIE0
$0205	PMFFPIN	Read: Write:	0	FPINE3	0	FPINE2	0	FPINE1	0	FPINE0
$0206	PMFFSTA	Read: Write:	0	FFLAG3	0	FFLAG2	0	FFLAG1	0	FFLAG0
$0207	PMFQSMP	Read: Write:	QSMP3		QSMP2		QSMP1		QSMP0	
$0208	PMFDMPA	Read: Write:	DMP13	DMP12	DMP11	DMP10	DMP03	DMP02	DMP01	DMP00
$0209	PMFDMPB	Read: Write:	DMP33	DMP32	DMP31	DMP30	DMP23	DMP22	DMP21	DMP20
$020A	PMFDMPC	Read: Write:	DMP53	DMP52	DMP51	DMP50	DMP43	DMP42	DMP41	DMP40

$0200 - $023F **PMF (**Pulse width Modulator with Fault protection**)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$020B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$020C	PMFOUTC	Read:	0	0	OUTCTL5	OUTCTL4	OUTCTL3	OUTCTL2	OUTCTL1	OUTCTL0
		Write:								
$020D	PMFOUTB	Read:	0	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
		Write:								
$020E	PMFDTMS	Read:	0	0	DT5	DT4	DT3	DT2	DT1	DT0
		Write:								
$020F	PMFCCTL	Read:	0	0	ISENS		0	IPOLC	IPOLB	IPOLA
		Write:								
$0210	PMFVAL0	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0211	PMFVAL0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0212	PMFVAL1	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0213	PMFVAL1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0214	PMFVAL2	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0215	PMFVAL2	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0200 - $023F **PMF (**Pulse width Modulator with Fault protection**)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0216	PMFVAL3	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0217	PMFVAL3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0218	PMFVAL4	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0219	PMFVAL4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$021A	PMFVAL5	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$021B	PMFVAL5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$021C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$021D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$021E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$021F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0220	PMFENCA	Read:	PWMENA	0	0	0	0	0	LDOKA	PWMRIEA
		Write:								

$0200 - $023F **PMF (**Pulse width Modulator with Fault protection**)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0221	PMFFQCA	Read: Write:	LDFQA				HALFA	PRSCA		PWMRFA
$0222	PMFCNTA	Read:	0	Bit 14	13	12	11	10	9	Bit 8
		Write:								
$0223	PMFCNTA	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0224	PMFMODA	Read:	0	Bit 14	13	12	11	10	9	Bit 8
		Write:								
$0225	PMFMODA	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0226	PMFDTMA	Read:	0	0	0	0	Bit 11	10	9	Bit 8
		Write:								
$0227	PMFDTMA	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0228	PMFENCB	Read:	PW-MENB	0	0	0	0	0	LDOKB	PWM-RIEB
		Write:								
$0229	PMFFQCB	Read: Write:	LDFQB				HALFB	PRSCB		PWMRFB
$022A	PMFCNTB	Read:	0	Bit 14	13	12	11	10	9	Bit 8
		Write:								
$022B	PMFCNTB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0200 - $023F **PMF (**Pulse width Modulator with Fault protection**)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$022C	PMFMODB	Read:	0	Bit 14	13	12	11	10	9	Bit 8
		Write:								
$022D	PMFMODB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$022E	PMFDTMB	Read:	0	0	0	0	Bit 11	10	9	Bit 8
		Write:								
$022F	PMFDTMB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0230	PMFENCC	Read:	PW-MENC	0	0	0	0	0	LDOKC	PWM-RIEC
		Write:								
$0231	PMFFQCC	Read:	LDFQC				HALFC	PRSCC		PWMRFC
		Write:								
$0232	PMFCNTC	Read:	0	Bit 14	13	12	11	10	9	Bit 8
		Write:								
$0233	PMFCNTC	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0234	PMFMODC	Read:	0	Bit 14	13	12	11	10	9	Bit 8
		Write:								
$0235	PMFMODC	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0236	PMFDTMC	Read:	0	0	0	0	Bit 11	10	9	Bit 8
		Write:								

$0200 - $023F **PMF (**Pulse width Modulator with Fault protection**)**

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0237	PMFDTMC	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0238	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0239	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$023A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$023B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$023C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$023D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$023E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$023F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0240 - $027F PIM (Port Interface Module)

$0240	PTT	Read:	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		Write:								
$0241	PTIT	Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		Write:								
$0242	DDRT	Read:	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		Write:								
$0243	RDRT	Read:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		Write:								
$0244	PERT	Read:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		Write:								
$0245	PPST	Read:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		Write:								
$0246	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0247	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0248	PTS	Read:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
		Write:								
$0249	PTIS	Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		Write:								
$024A	DDRS	Read:	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
		Write:								
$024B	RDRS	Read:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
		Write:								

$0240 - $027F PIM (Port Interface Module)

$024C	PERS	Read:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
		Write:								
$024D	PPSS	Read:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
		Write:								
$024E	WOMS	Read:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		Write:								
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250	PTM	Read:	PTM7	PTM6	PTM5	PTM4	PTM3	0	PTM1	PTM0
		Write:								
$0251	PTIM	Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	0	PTIM1	PTIM0
		Write:								
$0252	DDRM	Read:	DDRM7	DDRM6	DDRM5	DDRM4	DDRM3	0	DDRM1	DDRM0
		Write:								
$0253	RDRM	Read:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	0	RDRM1	RDRM0
		Write:								
$0254	PERM	Read:	PERM7	PERM6	PERM5	PERM4	PERM3	0	PERM1	PERM0
		Write:								
$0255	PPSM	Read:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	0	PPSM1	PPSM0
		Write:								
$0256	WOMM	Read:	WOMM7	WOMM6	WOMM5	WOMM4	0	0	0	0
		Write:								
$0257	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0240 - $027F PIM (Port Interface Module)

$0258	PTP	Read:	0	0	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		Write:								
$0259	PTIP	Read:	0	0	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		Write:								
$025A	DDRP	Read:	0	0	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		Write:								
$025B	RDRP	Read:	0	0	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
		Write:								
$025C	PERP	Read:	0	0	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		Write:								
$025D	PPSP	Read:	0	0	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
		Write:								
$025E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$025F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0260	PTQ	Read:	0	PTQ6	PTQ5	PTQ4	PTQ3	PTQ2	PTQ1	PTQ0
		Write:								
$0261	PTIQ	Read:	0	PTIQ6	PTIQ5	PTIQ4	PTIQ3	PTIQ2	PTIQ1	PTIQ0
		Write:								
$0262	DDRQ	Read:	0	DDRQ6	DDRQ5	DDRQ4	DDRQ3	DDRQ2	DDRQ1	DDRQ0
		Write:								
$0263	RDRQ	Read:	0	RDRQ6	RDRQ5	RDRQ4	RDRQ3	RDRQ2	RDRQ1	RDRQ0
		Write:								

$0240 - $027F PIM (Port Interface Module)

$0264	PERQ	Read:	0	PERQ6	PERQ5	PERQ4	PERQ3	PERQ2	PERQ1	PERQ0
		Write:								
$0265	PPSQ	Read:	0	PPSQ6	PPSQ5	PPSQ4	PPSQ3	PPSQ2	PPSQ1	PPSQ0
		Write:								
$0266	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0267	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0268	PTU	Read:	PTU7	PTU6	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
		Write:								
$0269	PTIU	Read:	PTIU7	PTIU6	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
		Write:								
$026A	DDRU	Read:	DDRU7	DDRU6	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
		Write:								
$026B	RDRU	Read:	RDRU7	RDRU6	RDRU5	RDRU4	RDRU3	RDRU2	RDRU1	RDRU0
		Write:								
$026C	PERU	Read:	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
		Write:								
$026D	PPSU	Read:	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
		Write:								
$026E	MODRR	Read:	0	0	0	0	MODRR3	MODRR2	MODRR1	MODRR0
		Write:								
$026F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0240 - $027F PIM (Port Interface Module)

$0270	PTAD(H)	Read: Write:	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
$0271	PTAD(L)	Read: Write:	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
$0272	PTIAD(H)	Read:	PTIAD15	PTIAD14	PTIAD13	PTIAD12	PTIAD11	PTIAD10	PTIAD9	PTIAD8
		Write:								
$0273	PTIAD(L)	Read:	PTIAD7	PTIAD6	PTIAD5	PTIAD4	PTIAD3	PTIAD2	PTIAD1	PTIAD0
		Write:								
$0274	DDRAD(H)	Read: Write:	DDRAD15	DDRAD14	DDRAD13	DDRAD12	DDRAD11	DDRAD10	DDRAD9	DDRAD8
$0275	DDRAD(L)	Read: Write:	DDRAD7	DDRAD6	DDRAD5	DDRAD4	DDRAD3	DDRAD2	DDRAD1	DDRAD0
$0276	RDRAD(H)	Read: Write:	RDRAD15	RDRAD14	RDRAD13	RDRAD12	RDRAD11	RDRAD10	RDRAD9	RDRAD8
$0277	RDRAD(L)	Read: Write:	RDRAD7	RDRAD6	RDRAD5	RDRAD4	RDRAD3	RDRAD2	RDRAD1	RDRAD0
$0278	PERAD(H)	Read: Write:	PERAD15	PERAD14	PERAD13	PERAD12	PERAD11	PERAD10	PERAD9	PERAD8
$0279	PERAD(L)	Read: Write:	PERAD7	PERAD6	PERAD5	PERAD4	PERAD3	PERAD2	PERAD1	PERAD0
$027A	PPSAD(H)	Read: Write:	PPSAD15	PPSAD14	PPSAD13	PPSAD12	PPSAD11	PPSAD10	PPSAD9	PPSAD8
$027B	PPSAD(L)	Read: Write:	PPSAD7	PPSAD6	PPSAD5	PPSAD4	PPSAD3	PPSAD2	PPSAD1	PPSAD0
$027C	PIEAD(H)	Read: Write:	PIEAD15	PIEAD14	PIEAD13	PIEAD12	PIEAD11	PIEAD10	PIEAD9	PIEAD8

$0240 - $027F PIM (Port Interface Module)

$027D	PIEAD(L)	Read: Write:	PIEAD7	PIEAD6	PIEAD5	PIEAD4	PIEAD3	PIEAD2	PIEAD1	PIEAD0
$027E	PIFAD(H)	Read: Write:	PIFAD15	PIFAD14	PIFAD13	PIFAD12	PIFAD11	PIFAD10	PIFAD9	PIFAD8
$027F	PIFAD(L)	Read: Write:	PIFAD7	PIFAD6	PIFAD5	PIFAD4	PIFAD3	PIFAD2	PIFAD1	PIFAD0

$0280 - $03FF Reserved space

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0280 - $2FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0300 - $03FF	Unimplemented	Read:	0	0	0	0	0	0	0	0
		Write:								

1.7 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses $001A and $001B after reset. The read-only value is a unique part ID for each revision of the chip. **Table 1-2** shows the assigned part ID numbers.

Table 1-2 Assigned Part ID Numbers

Device	Mask Set Number	Part ID[1]
MC9S12E256	**TBD**	$5000
MC9S12E128	2L15P	$5102
MC9S12E64	2L15P	$5200
MC9S12E32	**TBD**	$5300

NOTES:
1. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor - non full - mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses $001C and $001D after reset). **Table 1-3** shows the read-only values of these registers. Refer to HCS12 Module Mapping Control (MMC) Block Guide for further details.

Table 1-3 Memory size registers

Device	Register name	Value
MC9S12E32	MEMSIZ0	$00
MC9S12E32	MEMSIZ1	$80
MC9S12E64	MEMSIZ0	$03
MC9S12E64	MEMSIZ1	$80
MC9S12E128	MEMSIZ0	$03
MC9S12E128	MEMSIZ1	$80
MC9S12E256	MEMSIZ0	$07
MC9S12E256	MEMSIZ1	$81

Section 2 Signal Description

2.1 Device Pinout

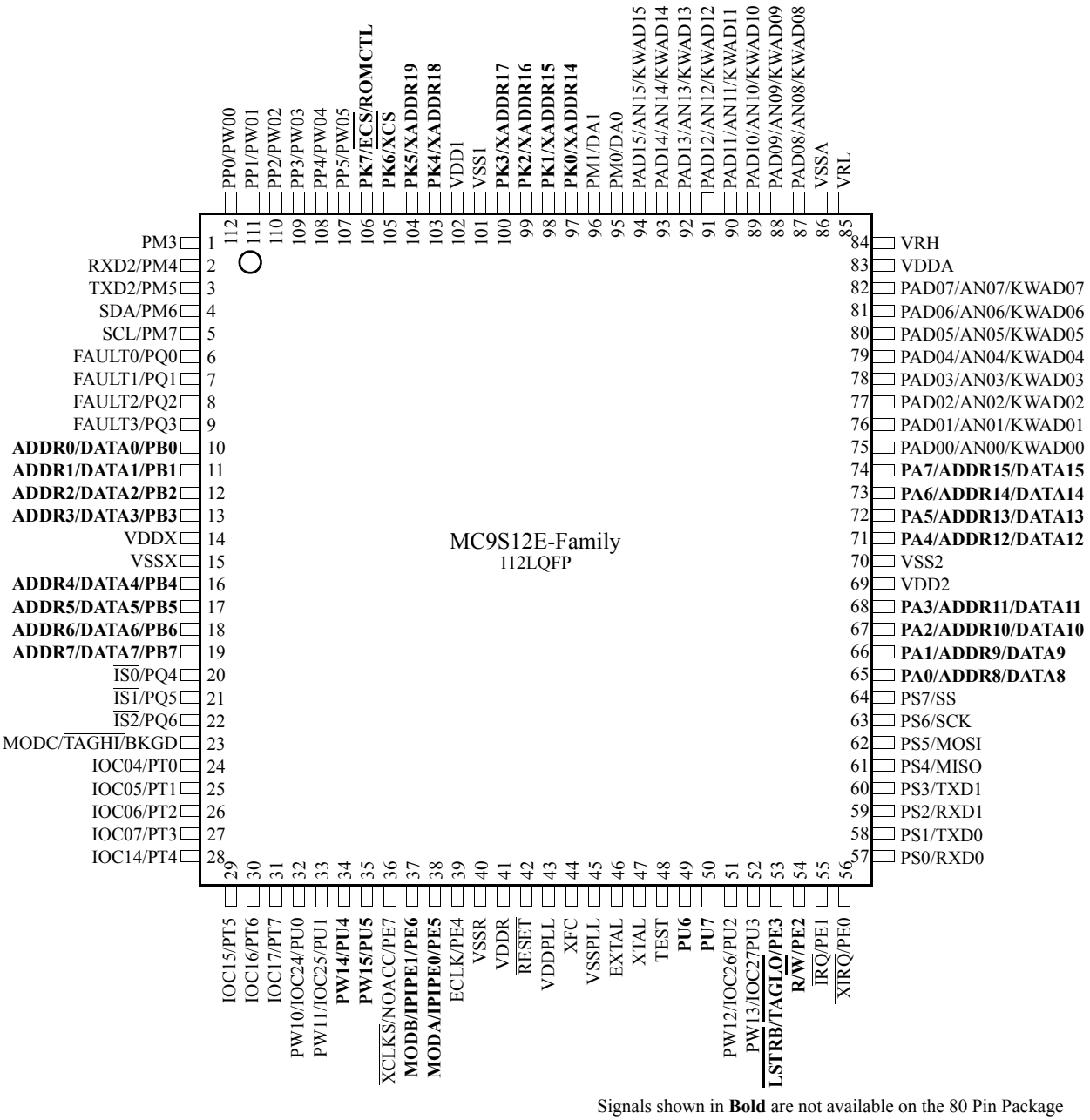


Figure 2-1 Pin assignments 112 LQFP for MC9S12E-Family

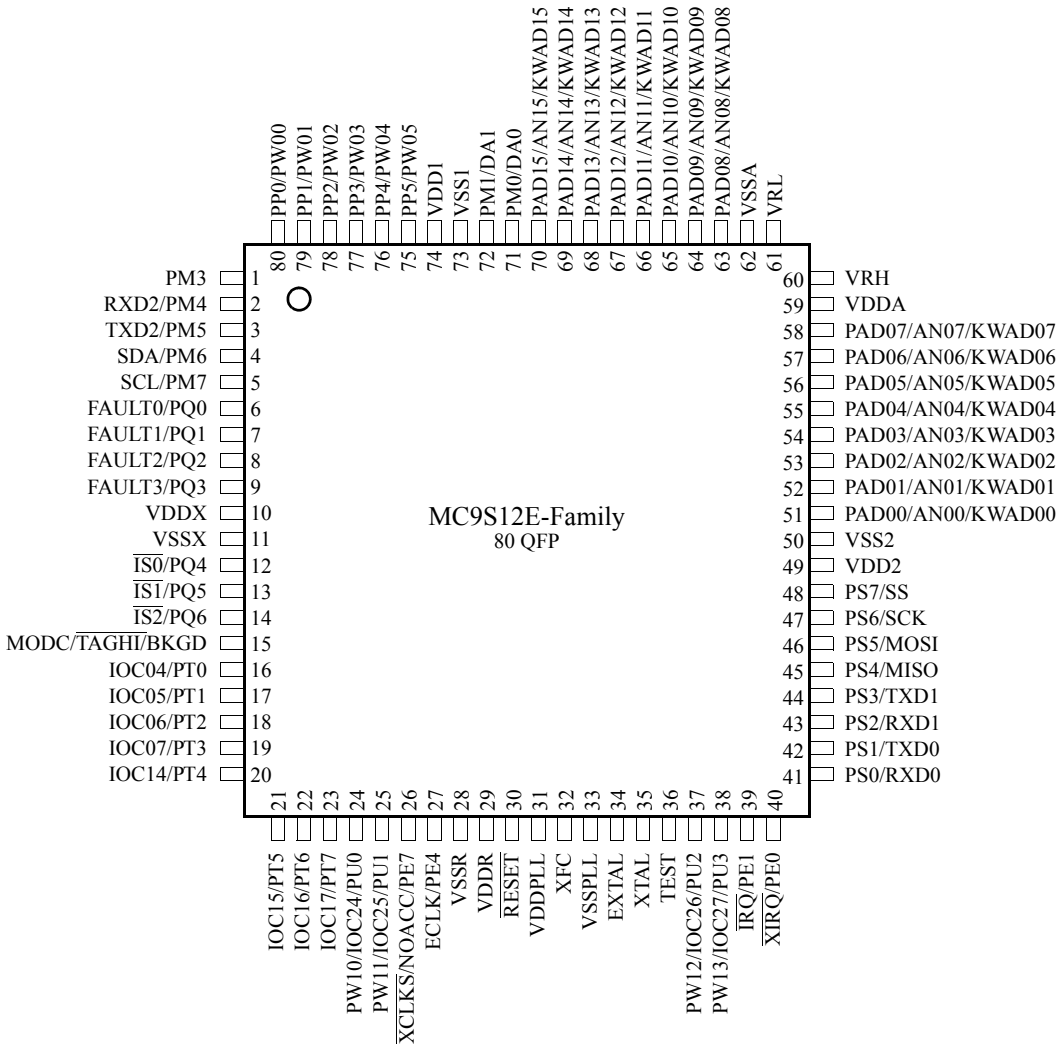


Figure 2-2 Pin assignments in 80 QFP for MC9S12E-Family

2.2 Signal Properties Summary

Table 2-1 Signal Properties

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Power Domain	Internal Pull Resistor		Description
				CTRL	Reset State	
EXTAL	—	—	VDDPLL	NA	NA	Oscillator pins
XTAL	—	—	VDDPLL	NA	NA	
XFC	—	—	VDDPLL	NA	NA	PLL loop filter pin
RESET	—	—	VDDX	None	None	External reset pin
BKGD	MODC	TAGHI	VDDX	Up	Up	Background debug, mode pin, tag signal high
TEST	VPP	—	NA	NA	NA	Test pin only
PAD[15:0]	AN[15:0]	KWAD[15:0}	VDDX	PERAD/ PPSAD	Disabled	Port AD I/O Pins, ATD inputs, keypad Wake-up
PA[7:0]	**ADDR[15:8]/ DATA[15:8]**	**—**	**VDDX**	**PUCR**	**Disabled**	**Port A I/O pin, multiplexed address/data**
PB[7:0]	**ADDR[7:0]/ DATA[7:0]**	**—**	**VDDX**	**PUCR**	**Disabled**	**Port B I/O pin, multiplexed address/data**
PE7	NOACC	XCLKS	VDDX	Input	Input	Port E I/O pin, access, clock select
PE6	**IPIPE1**	**MODB**	**VDDX**	**While RESET is low: Down**		**Port E I/O pin, pipe status, mode selection**
PE5	**IPIPE0**	**MODA**	**VDDX**	**While RESET is low: Down**		**Port E I/O pin, pipe status, mode selection**
PE4	ECLK	—	VDDX	PUCR	Mode Dep[1]	Port E I/O pin, bus clock output
PE3	**LSTRB**	**TAGLO**	**VDDX**	**PUCR**	**Mode Dep(1)**	**Port E I/O pin, low strobe, tag signal low**
PE2	**R/W**	**—**	**VDDX**	**PUCR**	**Mode Dep(1)**	**Port E I/O pin, R/W in expanded modes**
PE1	IRQ	—	VDDX	PUCR	Up	Port E input, external interrupt pin
PE0	XIRQ	—	VDDX	PUCR	Up	Port E input, non-maskable interrupt pin
PK[7]	**ECS**	**ROMCTL**	**VDDX**	**PUCR**	**Up**	**Port K I/O Pin, Emulation Chip Select**
PK[6]	**XCS**	**—**	**VDDX**	**PUCR**	**Up**	**Port K I/O Pin, External Chip Select**
PK[5:0]	**XADDR[19:14]**	**—**	**VDDX**	**PUCR**	**Up**	**Port K I/O Pins, Extended Addresses**
PM7	SCL	—	VDDX	PERM/ PPSM	Up	Port M I/O Pin, IIC SCL signal
PM6	SDA	—	VDDX	PERM/ PPSM	Up	Port M I/O Pin, IIC SDA signal
PM5	TXD2	—	VDDX	PERM/ PPSM	Up	Port M I/O Pin, SCI2 transmit signal
PM4	RXD2	—	VDDX	PERM/ PPSM	Up	Port M I/O Pin, SCI2 receive signal
PM3	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O Pin, IIC SDA signal
PM1	DAO1	—	VDDX	PERM/ PPSM	Disabled	Port M I/O Pin, DAC1 output
PM0	DAO0	—	VDDX	PERM/ PPSM	Disabled	Port M I/O Pin, DAC0 output
PP[5:0]	PW0[5:0]	—	VDDX	PERP/ PPSP	Disabled	Port P I/O Pins, PWM output

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Power Domain	Internal Pull Resistor		Description
				CTRL	Reset State	
PQ[6:4]	$\overline{IS}$[6:4]	—	VDDX	PERQ/ PPSQ	Disabled	Port Q I/O Pins, $\overline{IS}$[6:4] input
PQ[3:0]	FAULT[3:0]	—	VDDX	PERQ/ PPSQ	Disabled	Port Q I/O Pins, Fault[3:0] input
PS7	$\overline{SS}$	—	VDDX	PERS/ PPSS	Up	Port S I/O Pin, SPI SS signal
PS6	SCK	—	VDDX	PERS/ PPSS	Up	Port S I/O Pin, SPI SCK signal
PS5	MOSI	—	VDDX	PERS/ PPSS	Up	Port S I/O Pin, SPI MOSI signal
PS4	MISO	—	VDDX	PERS/ PPSS	Up	Port S I/O Pin, SPI MISO signal
PS3	TXD1	—	VDDX	PERS/ PPSS	Up	Port S I/O Pin, SCI1 transmit signal
PS2	RXD1	—	VDDX	PERS/ PPSS	Up	Port S I/O Pin, SCI1 receive signal
PS1	TXD0	—	VDDX	PERS/ PPSS	Up	Port S I/O Pin, SCI0 transmit signal
PS0	RXD0	—	VDDX	PERS/ PPSS	Up	Port S I/O Pin, SCI0 receive signal
PT[7:4]	IOC1[7:4]	—	VDDX	PERT/ PPST	Disabled	Port T I/O Pins, timer (TIM1)
PT[3:0]	IOC0[7:4]	—	VDDX	PERT/ PPST	Disabled	Port T I/O Pins, timer (TIM0)
PU[7:6]	**—**	**—**	**VDDX**	**PERU/ PPSU**	**Disabled**	**Port U I/O Pins**
PU[5:4]	**PW1[5:4]**	**—**	**VDDX**	**PERU/ PPSU**	**Disabled**	**Port U I/O Pins, PWM outputs**
PU[3:0]	IOC2[7:4]	PW1[3:0]	VDDX	PERU/ PPSU	Disabled	Port U I/O Pins, timer (TIM2), PWM outputs

NOTES:

1. The Port E output buffer enable signal control at reset is determined by the PEAR register and is mode dependent. For example, in special test mode RDWE = LSTRE = 1 which enables the PE[3:2] output buffers and disables the pull-ups. Refer to the S12 MEBI Block Guide for PEAR register details.

NOTE: *Signals shown in bold are not available in the 80 pin package.*

NOTE: *If the port pins are not bonded out in the chosen package the user should initialize the registers to be inputs with enabled pull resistance to avoid excess current consumption. This applies to the following pins:*

(80QFP): Port A[7:0], Port B[7:0], Port E[6,5,3,2], Port K[7:0], Port U[7:4]

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the external clock and crystal driver pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

RESET is an active low bidirectional control signal that acts as an input to initialize the MCU to a known start-up state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or COP watchdog circuit. External circuitry connected to the RESET pin should not include a large capacitance that would interfere with the ability of this signal to rise to a valid logic one within 32 ECLK cycles after the low drive is released. Upon detection of any reset, an internal circuit drives the RESET pin low and a clocked reset sequence controls when the MCU can begin normal processing The $\overline{\text{RESET}}$ pin includes an internal pull up device.

2.3.3 TEST — Test Pin

The TEST pin is reserved for test and must be tied to VSS in all applications.

2.3.4 XFC — PLL Loop Filter Pin

Dedicated pin used to create the PLL loop filter. See appendix **B.4.3.1**and the CRG Block Guide for more detailed information.

2.3.5 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High & Mode Pin

The BKGD / $\overline{\text{TAGHI}}$ / MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of RESET. In MCU expanded modes of operation, when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. This pin always has an internal pull up.

2.3.6 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA[7:0] are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus. PA[7:0] pins are not available in the 80 pin package version.

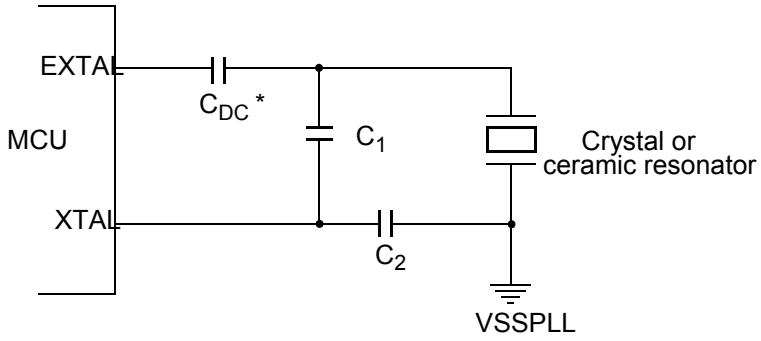
2.3.7 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB[7:0] are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus. PB[7:0] pins are not available in the 80 pin package version.

2.3.8 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free cycle”. This signal will assert when the CPU is not using the bus. The $\overline{\text{XCLKS}}$ is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of $\overline{\text{RESET}}$. If the input is a logic low the EXTAL pin is configured for an external clock drive or a Pierce Oscillator. If the input is a logic high a Colpitts oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device during reset, if the pin is left floating, the default configuration is a Colpitts oscillator circuit on EXTAL and XTAL.

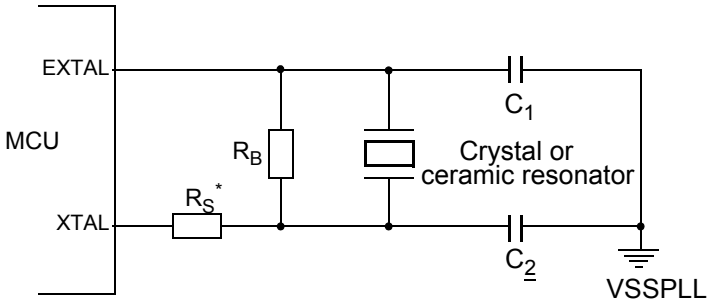
Figure 2-3 Colpitts Oscillator Connections (PE7=1)



* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal

.Please contact the crystal manufacturer for crystal DC

Figure 2-4 Pierce Oscillator Connections (PE7=0)



* Rs can be zero (shorted) when use with higher frequency crystals. Refer to manufacturer's data.

2.3.9 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of RESET. This pin is shared with the

instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when RESET is low. PE6 is not available in the 80 pin package version.

2.3.10 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of RESET. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when RESET is low. PE5 is not available in the 80 pin package version.

2.3.11 PE4 / ECLK— Port E I/O Pin 4 / E-Clock Output

PE4 is a general purpose input or output pin. In Normal Single Chip mode PE4 is configured with an active pull-up while in reset and immediately out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register. In all modes except Normal Single Chip Mode, the PE4 pin is initially configured as the output connection for the internal bus clock(ECLK). ECLK is used as a timing reference and to demultiplex the address and data in expanded modes. The ECLK frequency is equal to 1/2 the crystal frequency out of reset. The ECLK output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. All clocks, including the ECLK, are halted when the MCU is in STOP mode. It is possible to configure the MCU to interface to slow external memory. ECLK can be stretched for such accesses. The PE4 pin is initially configured as ECLK output with stretch in all expanded modes. Reference the MISC register (EXSTR[1:0] bits) for more information. In normal expanded narrow mode, the ECLK is available for use in external select decode logic or as a constant speed clock for use in the external application system.

2.3.12 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3 / Low-Byte Strobe ($\overline{\text{LSTRB}}$)

PE3 can be used as a general-purpose I/O in all modes and is an input with an active pull-up out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register. PE3 can also be configured as a Low-Byte Strobe ($\overline{\text{LSTRB}}$). The $\overline{\text{LSTRB}}$ signal is used in write operations, so external low byte writes will not be possible until this function is enabled. $\overline{\text{LSTRB}}$ can be enabled by setting the LSTRE bit in the PEAR register. In Expanded Wide and Emulation Narrow modes, and when BDM tagging is enabled, the $\overline{\text{LSTRB}}$ function is multiplexed with the $\overline{\text{TAGLO}}$ function. When enabled a logic zero on the $\overline{\text{TAGLO}}$ pin at the falling edge of ECLK will tag the low byte of an instruction word being read into the instruction queue. PE3 is not available in the 80 pin package version.

2.3.13 PE2 / R/$\overline{\text{W}}$ — Port E I/O Pin 2 / Read/$\overline{\text{Write}}$

PE2 can be used as a general-purpose I/O in all modes and is configured an input with an active pull-up out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register. If the read/$\overline{\text{write}}$ function is required it should be enabled by setting the RDWE bit in the PEAR register. External writes will not be possible until the read/$\overline{\text{write}}$ function is enabled. The PE2 pin is not available in the 80 pin package version.

2.3.14 PE1 / $\overline{\text{IRQ}}$ — Port E input Pin 1 / Maskable Interrupt Pin

PE1 is always an input and can always be read. The PE1 pin is also the $\overline{\text{IRQ}}$ input used for requesting an asynchronous interrupt to the MCU. During reset, the I bit in the condition code register (CCR) is set and any $\overline{\text{IRQ}}$ interrupt is masked until software enables it by clearing the I bit. The $\overline{\text{IRQ}}$ is software programmable to either falling edge-sensitive triggering or level-sensitive triggering based on the setting of the IRQE bit in the IRQCR register. The $\overline{\text{IRQ}}$ is always enabled and configured to level-sensitive triggering out of reset. It can be disabled by clearing IRQEN bit in the IRQCR register. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register.

2.3.15 PE0 / $\overline{\text{XIRQ}}$ — Port E input Pin 0 / Non Maskable Interrupt Pin

PE0 is always an input and can always be read. The PE0 pin is also the $\overline{\text{XIRQ}}$ input for requesting a nonmaskable asynchronous interrupt to the MCU. During reset, the X bit in the condition code register (CCR) is set and any $\overline{\text{XIRQ}}$ interrupt is masked until MCU software enables it by clearing the X bit. Because the $\overline{\text{XIRQ}}$ input is level sensitive triggered, it can be connected to a multiple-source wired-OR network. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register.

2.3.16 PK7 / $\overline{\text{ECS}}$ / ROMCTL — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, when the EMK bit in the MODE register is set to 1, this pin is used as the emulation chip select output ($\overline{\text{ECS}}$). In expanded modes the PK7 pin can be used to determine the reset state of the ROMON bit in the MISC register. At the rising edge of $\overline{\text{RESET}}$, the state of the PK7 pin is latched to the ROMON bit. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPKE in the PUCR register. Refer to the HCS12 MEBI Block Guide for further details. PK7 is not available in the 80 pin package version.

2.3.17 PK6 / $\overline{\text{XCS}}$ — Port K I/O Pin 6

PK6 is a general purpose input or output pin. During MCU expanded modes of operation, when the EMK bit in the MODE register is set to 1, this pin is used as an external chip select signal for most external accesses that are not selected by ECS. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPKE in the PUCR register. Refer to the HCS12 MEBI Block Guide for further details. PK6 is not available in the 80 pin package version.

2.3.18 PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]

PK[5:0] are general purpose input or output pins. In MCU expanded modes of operation, when the EMK bit in the MODE register is set to 1, PK[5:0] provide the expanded address XADDR[19:14] for the external bus. There are active pull-ups on PK[5:0] pins while in reset and immediately out of reset. The pullup can be turned off by clearing PUPKE in the PUCR register. Refer to the HCS12 MEBI Block Guide for further details. PK[5:0] are not available in the 80 pin package version.

2.3.19 PAD[15:0] / AN[15:0] / KWAD[15:0] — Port AD I/O Pins [15:0]

PAD[15:0] are the analog inputs for the analog to digital converter (ADC). They can also be configured as general purpose digital input or output pin. When enabled as digital inputs or outputs, the PAD[15:0] can also be configured as Keypad Wake-up pins (KWU) and generate interrupts causing the MCU to exit STOP or WAIT mode. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the ATD_10B16C Block Guide for information about pin configurations.

2.3.20 PM7 / SCL — Port M I/O Pin 7

PM7 is a general purpose input or output pin. When the IIC module is enabled it becomes the serial clock line (SCL) for the IIC module (IIC). While in reset and immediately out of reset the PM7 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the IIC Block Guide for information about pin configurations.

2.3.21 PM6 / SDA — Port M I/O Pin 6

PM6 is a general purpose input or output pin. When the IIC module is enabled it becomes the Serial Data Line (SDL) for the IIC module (IIC). While in reset and immediately out of reset the PM6 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the IIC Block Guide for information about pin configurations.

2.3.22 PM5 / TXD2 — Port M I/O Pin 5

PM5 is a general purpose input or output. When the Serial Communications Interface 2 (SCI2) transmitter is enabled the PM5 pin is configured as the transmit pin TXD2 of SCI2. While in reset and immediately out of reset the PM5 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the SCI Block Guide for information about pin configurations.

2.3.23 PM4 / RXD2 — Port M I/O Pin 4

PM4 is a general purpose input or output. When the Serial Communications Interface 2 (SCI2) receiver is enabled the PM4 pin is configured as the receive pin RXD2 of SCI2. While in reset and immediately out of reset the PM4 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the SCI Block Guide for information about pin configurations.

2.3.24 PM3 — Port M I/O Pin 3

PM3 is a general purpose input or output pin. While in reset and immediately out of reset the PM3 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide for information about pin configurations.

2.3.25 PM1 / DAO1 — Port M I/O Pin 1

PM1 is a general purpose input or output pin. When the Digital to Analog module 1 (DAC1) is enabled the PM1 pin is configured as the analog output DA01 of DAC1. While in reset and immediately out of reset the PM1 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the DAC_8B1C Block Guide for information about pin configurations.

2.3.26 PM0 / DAO2 — Port M I/O Pin 0

PM0 is a general purpose input or output pin. When the Digital to Analog module 2 (DAC2) is enabled the PM0 pin is configured as the analog output DA02 of DAC2. While in reset and immediately out of reset the PM0 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the DAC_8B1C Block Guide for information about pin configurations.

2.3.27 PP[5:0] / PW0[5:0] — Port P I/O Pins [5:0]

PP[5:0] are general purpose input or output pins. When the Pulse width Modulator with Fault protection (PMF) is enabled the PP[5:0] output pins, as a whole or as pairs, can be configured as PW0[5:0] outputs. While in reset and immediately out of reset the PP[5:0] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the PMF_15B6C Block Guide for information about pin configurations.

2.3.28 PQ[6:4] / IS[2:0] — Port Q I/O Pins [6:4]

PQ[6:4] are general purpose input or output pins. When enabled in the Pulse width Modulator with Fault protection module (PMF), the PQ[6:4] pins become the current status input pins, $\overline{IS}$[2:0], for top/bottom pulse width correction. While in reset and immediately out of reset PP[5:0] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the PMF_15B6C Block Guide for information about pin configurations.

2.3.29 PQ[3:0] / FAULT[3:0] — Port Q I/O Pins [3:0]

PQ[3:0] are general purpose input or output pins. When enabled in the Pulse width Modulator with Fault protection module (PMF), the PQ[3:0] pins become the Fault protection inputs pins, FAULT[3:0], of the PMF. While in reset and immediately out of reset the PQ[3:0] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the PMF_15B6C Block Guide for information about pin configurations.

2.3.30 PS7 / $\overline{SS}$ — Port S I/O Pin 7

PS7 is a general purpose input or output. When the Serial Peripheral Interface (SPI) is enabled PS7 becomes the slave select pin $\overline{SS}$. While in reset and immediately out of reset the PS7 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the SPI Block Guide for information about pin configurations.

2.3.31 PS6 / SCK — Port S I/O Pin 6

PS6 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS6 becomes the serial clock pin, SCK. While in reset and immediately out of reset the PS6 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the SPI Block Guide for information about pin configurations.

2.3.32 PS5 / MOSI — Port S I/O Pin 5

PS5 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS5 is the master output (during master mode) or slave input (during slave mode) pin. While in reset and immediately out of reset the PS5 pin is configured as a high impedance input pin Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the SPI Block Guide for information about pin configurations.

2.3.33 PS4 / MISO — Port S I/O Pin 4

PS4 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS4 is the master input (during master mode) or slave output (during slave mode) pin. While in reset and immediately out of reset the PS4 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the SPI Block Guide for information about pin configurations.

2.3.34 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output. When the Serial Communications Interface 1 (SCI1) transmitter is enabled the PS3 pin is configured as the transmit pin, TXD1, of SCI1. While in reset and immediately out of reset the PS3 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the SCI Block Guide for information about pin configurations.

2.3.35 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output. When the Serial Communications Interface 1 (SCI1) receiver is enabled the PS2 pin is configured as the receive pin RXD1 of SCI1. While in reset and immediately out of reset the PS2 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the SCI Block Guide for information about pin configurations.

2.3.36 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) transmitter is enabled the PS1 pin is configured as the transmit pin, TXD0, of SCI0. While in reset and immediately out of reset the PS1 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the SCI Block Guide for information about pin configurations.

2.3.37 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) receiver is enabled the PS0 pin is configured as the receive pin RXD0 of SCI0. While in reset and immediately out of reset the PS0 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the SCI Block Guide for information about pin configurations.

2.3.38 PT[7:4] / IOC1[7:4]— Port T I/O Pins [7:4]

PT[7:4] are general purpose input or output pins. When the Timer system 1 (TIM1) is enabled they can also be configured as the TIM1 input capture or output compare pins IOC1[7-4]. While in reset and immediately out of reset the PT[7:4] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the TIM_16B4C Block Guide for information about pin configurations.

2.3.39 PT[3:0] / IOC0[7:4]— Port T I/O Pins [3:0]

PT[3:0] are general purpose input or output pins. When the Timer system 0 (TIM0) is enabled they can also be configured as the TIM0 input capture or output compare pins IOC0[7-4]. While in reset and immediately out of reset the PT[3:0] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the TIM_16B4C Block Guide for information about pin configurations.

2.3.40 PU[7:6] — Port U I/O Pins [7:6]

PU[7:6] are general purpose input or output pins. While in reset and immediately out of reset the PU[7:6] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 for information about pin configurations. PU[7:6] are not available in the 80 pin package version.

2.3.41 PU[5:4] / PW1[5:4] — Port U I/O Pins [5:4]

PU[5:4] are general purpose input or output pins. When the Pulse Width Modulator (PWM) is enabled the PU[5:4] output pins, individually or as a pair, can be configured as PW1[5:4] outputs. While in reset and immediately out of reset the PU[5:4] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide and the PWM_8B6C Block Guide for information about pin configurations. PU[5:4] are not available in the 80 pin package version.

2.3.42 PU[3:0] / IOC2[7:4]/PW1[3:0] — Port U I/O Pins [3:0]

PU[3:0] are general purpose input or output pins. When the Timer system 2 (TIM2) is enabled they can also be configured as the TIM2 input capture or output compare pins IOC2[7-4]. When the Pulse Width Modulator (PWM) is enabled the PU[3:0] output pins, individually or as a pair, can be configured as PW1[3:0] outputs. The MODRR register in the Port Integration Module determines if the TIM2 or PWM function is selected. While in reset and immediately out of reset the PU[3:0] pins are configured as a high

impedance input pins. Consult the Port Integration Module (PIM) PIM_9E128 Block Guide, TIM_16B4C Block Guide, and the PWM_8B6C Block Guide for information about pin configurations.

2.4 Power Supply Pins

2.4.1 VDDX,VSSX — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR, VSSR — Power Supply Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Power Supply Pins for Internal Logic

Power is supplied to the MCU through VDD and VSS. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VDDR is tied to ground.

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the analog to digital converter.

2.4.5 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.6 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently.This 2.5V voltage is generated by the internal voltage regulator.

Table 2-2 MC9S12E-Family Power and Ground Connection Summary

Mnemonic	Nominal Voltage	Description
VDD1 VDD2	2.5 V	Internal power and ground generated by internal regulator. These also allow an external source to supply the core VDD/VSS voltages and bypass the internal voltage regulator.
VSS1 VSS2	0V	
VDDR	3.3/5.0 V	External power and ground, supply to internal voltage regulator. To disable voltage regulator attach V_{DDR} to V_{SSR}.
VSSR	0 V	
VDDX	3.3/5.0 V	External power and ground, supply to pin drivers.
VSSX	0 V	
VDDA	3.3/5.0 V	Operating voltage and ground for the analog-to-digital converter, the reference for the internal voltage regulator and the digital-to-analog converters, allows the supply voltage to the A/D to be bypassed independently.
VSSA	0 V	
VRH	3.3/5.0 V	Reference voltage high for the ATD converter, and DAC.
VRL	0 V	Reference voltage low for the ATD converter.
VDDPLL	2.5 V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	0 V	

NOTE: *All VSS pins must be connected together in the application. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on MCU pin load.*

Section 3 System Clock Description

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules. Consult the CRG Block Guide for details on clock generation.

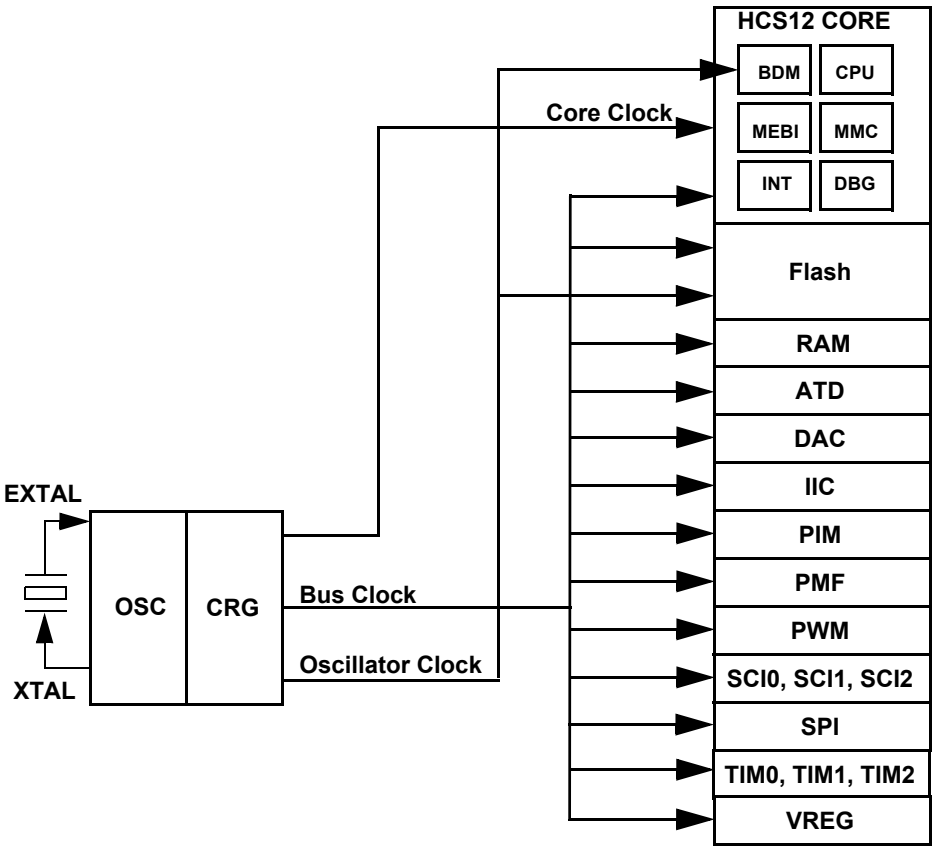


Figure 3-1 Clock Connections

Table 3-1Clock Selection Based on PE7

PE7 = XCLKS	Description
1	Colpitts Oscillator selected
0	Pierce Oscillator/external clock selected

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12E-Family. Each mode has an associated default memory map and external bus configuration controlled by a further pin.

Three low power modes exist for the device.

4.2 Chip Configuration Summary

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset. The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal. The ROMCTL signal allows the setting of the ROMON bit in the MISC register thus controlling whether the internal Flash is visible in the memory map. ROMON = 1 mean the Flash is visible in the memory map. The state of the ROMCTL pin is latched into the ROMON bit in the MISC register on the rising edge of the reset signal.

Table 4-1 Mode Selection

BKGD = MODC	PE6 = MODB	PE5 = MODA	PK7 = ROMCTL	ROMON Bit	Mode Description
0	0	0	X	1	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	0	1	Emulation Expanded Narrow, BDM allowed
			1	0	
0	1	0	X	0	Special Test (Expanded Wide), BDM allowed
0	1	1	0	1	Emulation Expanded Wide, BDM allowed
			1	0	
1	0	0	X	1	Normal Single Chip, BDM allowed
1	0	1	0	0	Normal Expanded Narrow, BDM allowed
			1	1	
1	1	0	X	1	Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	0	0	Normal Expanded Wide, BDM allowed
			1	1	

For further explanation on the modes refer to the HCS12 MEBI Block Guide.

Table 4-2 Clock Selection Based on PE7

PE7 = XCLKS	Description
1	Colpitts Oscillator selected
0	Pierce Oscillator/external clock selected

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH, the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH will be disabled. BDM operations will be blocked.

4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH must be erased. This can be done through an external program in expanded mode.

Once the user has erased the FLASH, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to

an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

4.4 Low Power Modes

The microcontroller features three main low power modes. Consult the respective Block Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is the Clock and Reset Generator (CRG) Block Guide.

4.4.1 Stop

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

4.4.2 Pseudo Stop

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

4.4.3 Wait

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and databus) will be fully static. All peripherals stay active. For further power consumption the peripherals can individually turn off their local clocks.

4.4.4 Run

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

Section 5 Resets and Interrupts

5.1 Overview

Consult the Exception Processing section of the CPU12 Reference Manual for information on resets and interrupts. System resets can be generated through external control of the $\overline{\text{RESET}}$ pin, through the clock and reset generator module CRG or through the low voltage reset (LVR) generator of the voltage regulator module. Refer to the CRG and VREG Block Guides for detailed information on reset generation.

5.2 Vectors

Table 5-1 lists interrupt sources and vectors in default order of priority.

Table 5-1 Interrupt Vector Locations

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFFE, $FFFF	External Reset, Power On Reset or Low Voltage Reset (see CRG Flags Register to determine reset source)	None	None	–
$FFFC, $FFFD	Clock Monitor fail reset	None	COPCTL (CME, FCME)	–
$FFFA, $FFFB	COP failure reset	None	COP rate select	–
$FFF8, $FFF9	Unimplemented instruction trap	None	None	–
$FFF6, $FFF7	SWI	None	None	–
$FFF4, $FFF5	XIRQ	X-Bit	None	–
$FFF2, $FFF3	IRQ	I-Bit	INTCR (IRQEN)	$F2
$FFF0, $FFF1	Real Time Interrupt	I-Bit	CRGINT (RTIE)	$F0
$FFE8 to $FFEF	Reserved			
$FFE6, $FFE7	Standard Timer 0 channel 4	I-Bit	TIE (C4I)	$E6
$FFE4, $FFE5	Standard Timer 0 channel 5	I-Bit	TIE (C5I)	$E4
$FFE2, $FFE3	Standard Timer 0 channel 6	I-Bit	TIE (C6I)	$E2
$FFE0, $FFE1	Standard Timer 0 channel 7	I-Bit	TIE (C7I)	$E0
$FFDE, $FFDF	Standard Timer overflow	I-Bit	TSCR2 (TOI)	$DE
$FFDC, $FFDD	Pulse accumulator overflow	I-Bit	PACTL(PAOVI)	$DC
$FFDA, $FFDB	Pulse accumulator input edge	I-Bit	PACTL (PAI)	$DA
$FFD8, $FFD9	SPI	I-Bit	SPICR1 (SPIE, SPTIE)	$D8
$FFD6, $FFD7	SCI0	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	$D6
$FFD4, $FFD5	SCI1	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	$D4
$FFD2, $FFD3	SCI2	I-Bit	SCICR2 (TIE, TCIE, RIE, ILIE)	$D2
$FFD0, $FFD1	ATD	I-Bit	ATDCTL2 (ASCIE)	$D0
$FFCE, $FFCF	Port AD (KWU)	I-Bit	PTADIF (PTADIE)	$CE
$FFC8 to $FFCD	Reserved			
$FFC6, $FFC7	CRG PLL lock	I-Bit	PLLCR (LOCKIE)	$C6
$FFC4, $FFC5	CRG Self Clock Mode	I-Bit	PLLCR (SCMIE)	$C4

$FFC2, $FFC3	Reserved			
$FFC0, $FFC1	IIC Bus	I-Bit	IBCR (IBIE)	$C0
$FFBA to $FFBF	Reserved			
$FFB8, $FFB9	FLASH	I-Bit	FCNFG (CCIE, CBEIE)	$B8
$FFB6, $FFB7	Standard Timer 1 channel 4	I-Bit	TIE (C4I)	$B6
$FFB4, $FFB5	Standard Timer 1 channel 5	I-Bit	TIE (C5I)	$B4
$FFB2, $FFB3	Standard Timer 1 channel 6	I-Bit	TIE (C6I)	$B2
$FFB0, $FFB1	Standard Timer 1 channel 7	I-Bit	TIE (C7I)	$B0
$FFAE, $FFAF	Standard Timer 1 overflow	I-Bit	TSCR2 (TOI)	$AE
$FFAC, $FFAD	Standard Timer 1 Pulse accumulator overflow	I-Bit	PACTL (PAOVI)	$AC
$FFAA, $FFAB	Standard Timer 1 Pulse accumulator input edge	I-Bit	PACTL (PAI)	$AA
$FFA8, $FFA9	Reserved			
$FFA6, $FFA7	Standard Timer 2 channel 4	I-Bit	TIE (C4I)	$A6
$FFA4, $FFA5	Standard Timer 2 channel 5	I-Bit	TIE (C5I)	$A4
$FFA2, $FFA3	Standard Timer 2 channel 6	I-Bit	TIE (C6I)	$A2
$FFA0, $FFA1	Standard Timer 2 channel 7	I-Bit	TIE (C7I)	$A0
$FF9E, $FF9F	Standard Timer overflow	I-Bit	TSCR2 (TOI)	$9E
$FF9C, $FF9D	Standard Timer 2 Pulse accumulator overflow	I-Bit	PACTL (PAOVI)	$9C
$FF9A, $FF9B	Standard Timer 2 Pulse accumulator input edge	I-Bit	PACTL (PAI)	$9A
$FF98, $FF99	PMF Generator A Reload	I-Bit	PMFENCA (PWMRIEA)	$98
$FF96, $FF97	PMF Generator B Reload	I-Bit	PMFENCB (PWMRIEB)	$96
$FF94, $FF95	PMF Generator C Reload	I-Bit	PMFENCC (PWMRIEC)	$94
$FF92, $FF93	PMF Fault 0	I-Bit	PMFFCTL (FIE0)	$92
$FF90, $FF91	PMF Fault 1	I-Bit	PMFFCTL (FIE1)	$90
$FF8E, $FF8F	PMF Fault 2	I-Bit	PMFFCTL (FIE2)	$8E
$FF8C, $FF8D	PMF Fault 3	I-Bit	PMFFCTL (FIE3)	$8C
$FF8A, $FF8B	VREG LVI	I-Bit	CTRL0 (LVIE)	$8A
$FF88, $FF89	PWM Emergency Shutdown	I-Bit	PWMSDN(PWMIE)	$88
$FF80 to $FF87	Reserved			

5.3 Resets

Resets are a subset of the interrupts featured in**Table 5-1**. The different sources capable of generating a system reset are summarized in **Table 5-2**.

Table 5-2 Reset Summary

Reset	Priority	Source	Vector
Power-on Reset	1	CRG Module	$FFFE, $FFFF
External Reset	1	RESET pin	$FFFE, $FFFF
Low Voltage Reset	1	VREG Module	$FFFE, $FFFF
Clock Monitor Reset	2	CRG Module	$FFFC, $FFFD

Table 5-2 Reset Summary

COP Watchdog Reset	3	CRG Module	$FFFA, $FFFB

5.3.1 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block Guides for register reset states. Refer to the HCS12 MEBI Block Guide for mode dependent pin configuration of port A, B and E out of reset.

Refer to the PIM Block Guide for reset configurations of all peripheral module ports.

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

Section 6 HCS12 Core Block Description

6.1 CPU12 Block Description

Consult the CPU12 Reference Manual for information about the Central Processing Unit.

When the CPU12 Reference Manual refers to *cycles* this is equivalent to *Bus Clock periods*.
So *1 cycle* is equivalent to *1 Bus Clock period*.

6.2 HCS12 Background Debug Module (BDM) Block Description

Consult the HCS12 BDM Block Guide for information about the Background Debug Module.

When the BDM Block Guide refers to *alternate clock* this is equivalent to *Oscillator Clock*.

6.3 HCS12 Debug (DBG) Block Description

Consult the HCS12 DBG Block Guide for information about the Debug module.

6.4 HCS12 Interrupt (INT) Block Description

Consult the HCS12 INT Block Guide for information about the Interrupt module.

6.5 HCS12 Multiplexed External Bus Interface (MEBI) Block Description

Consult the HCS12 MEBI Block Guide for information about the Multiplexed External Bus Interface module.

6.6 HCS12 Module Mapping Control (MMC) Block Description

Consult the HCS12 MMC Block Guide for information about the Module Mapping Control module.

Section 7 Analog to Digital Converter (ATD) Block Description

Consult the ATD_10B16C Block Guide for further information about the A/D Converter module.

Note that V04 of the ATD has an external trigger (ETRIG) function which is tied off and not available for use.

Section 8 Clock Reset Generator (CRG) Block Description

Consult the CRG Block Guide for information about the Clock and Reset Generator module.

8.1 Device-specific information

The Low Voltage Reset feature uses the low voltage reset signal from the VREG module as an input to the CRG module. When the regulator output voltage supply to the internal chip logic falls below a specified threshold the LVR signal from the VREG module causes the CRG module to generate a reset. Consult the VREG Block Guide for voltage level specifications. 3F.

8.1.1 $\overline{\text{XCLKS}}$

The $\overline{\text{XCLKS}}$ input signal is active low (see **2.3.8 PE7 / NOACC / XCLKS — Port E I/O Pin 7**).

Section 9 Digital to Analog Converter (DAC) Block Description

There are two digital to analog converter modules (DAC0, DAC1). Consult the DAC Block Guide for information about the DAC Module.

Section 10 Flash EEPROM Block Description

Consult the FTS32K Block Guide for information about the flash module for the MC9S12E32.

Consult the FTS128K1 Block Guide for information about the flash module for the MC9S12E64.

Consult the FTS128K1 Block Guide for information about the flash module for the MC9S12E128.

Consult the FTS256K2 Block Guide for information about the flash module for the MC9S12E256.

The "S12 LRAE" is a generic Load RAM and Execute (LRAE) program which will be programmed into the flash memory of this device during manufacture. This LRAE program will provide greater programming flexibility to the end users by allowing the device to be programmed directly using SCI after it is assembled on the PCB. Use of the LRAE program is at the discretion of the end user and, if not required, it must simply be erased prior to flash programming. For more details of the S12 LRAE and its implementation, please see the S12 LREA Application Note (AN2546/D) .

It is planned that most HC9S12 devices manufactured after Q1 of 2004 will be shipped with the S12 LRAE programmed in the Flash . Exact details of the changeover (ie blank to programmed) for each product will be communicated in advance via GPCN and will be traceable by the customer via datecode marking on the device.

Please contact Motorola SPS Sales if you have any additional questions.

Section 11 IIC Block Description

Consult the IIC Block Guide for information about the IIC Module.

Section 12 Oscillator (OSC) Block Description

Consult the OSC Block Guide for information about the Oscillator module.

Section 13 Port Integration Module (PIM) Block Description

Consult the PIM_9E128 Block Guide for information about the Port Integration Module.

Section 14 Pulse width Modulator with Fault protection (PMF) Block Description

Consult the PMF_15B6C Block Guide for information about the Pulse width Modulator with Fault protection Module.

Section 15 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B6C Block Guide for information about the Pulse Width Modulator Module.

Section 16 Serial Communications Interface (SCI) Block

Description

There are three Serial Communications Interface modules (SCI0, SCI1, SCI2). Consult the SCI Block Guide for information about the Serial Communications Interface module.

Section 17 Serial Peripheral Interface (SPI) Block Description

Consult the SPI Block Guide for information about the Serial Peripheral Interface module.

Section 18 Timer (TIM) Block Description

There are three timer modules (TIM0, TIM1, TIM2). Consult the TIM_16B4C Block Guide for information about the Timer module.

Section 19 Voltage Regulator (VREG) Block Description

Consult the VREG Block Guide for information about the dual output linear voltage regulator.

19.1 VREGEN

On the MC9S12E-Family the regulator enable signal (VREGEN) is not available externally and is connected internally to VDDR.

19.2 VDD1, VDD2, VSS1, VSS2

In both the 112 pin LQFP and the 80 pin QFP package versions, both internal VDD and VSS of the 2.5V domain are bonded out on 2 sides of the device as two pin pairs (VDD1, VSS1 & VDD2, VSS2). VDD1 and VDD2 are connected together internally. VSS1 and VSS2 are connected together internally. This allows systems to employ better supply routing and further decoupling.

Section 20 Printed Circuit Board Layout Proposals

The Printed Circuit Board (PCB) must be carefully laid out to ensure proper operation of the voltage regulator as well as the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins (C1 - C6).

- Central point of the ground star should be the VSSR pin.
- Use low ohmic low inductance connections between VSS1, VSS2 and VSSR.
- VSSPLL must be directly connected to VSSR.
- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C7, C8, C11 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8, C10 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

Table 20-1 Recommended decoupling capacitor choice

Component	Purpose	Type	Value
C1	VDD1 filter cap	ceramic X7R	100 - 220nF
C2	VDD2 filter cap (80 QFP only)	ceramic X7R	100 - 220nF
C3	VDDA filter cap	ceramic X7R	100nF
C4	VDDR filter cap	X7R/tantalum	>=100nF
C5	VDDPLL filter cap	ceramic X7R	100nF
C6	VDDX filter cap	X7R/tantalum	>=100nF
C7	OSC load cap	See PLL specification chapter	
C8	OSC load cap		
C9	PLL loop filter cap		
C10	PLL loop filter cap		
C11	DC cutoff cap		
R1	PLL loop filter res		
Q1	Quartz		

Figure 20-1 Recommended PCB Layout (112 LQFP)

NOTE: Oscillator in Colpitts mode.

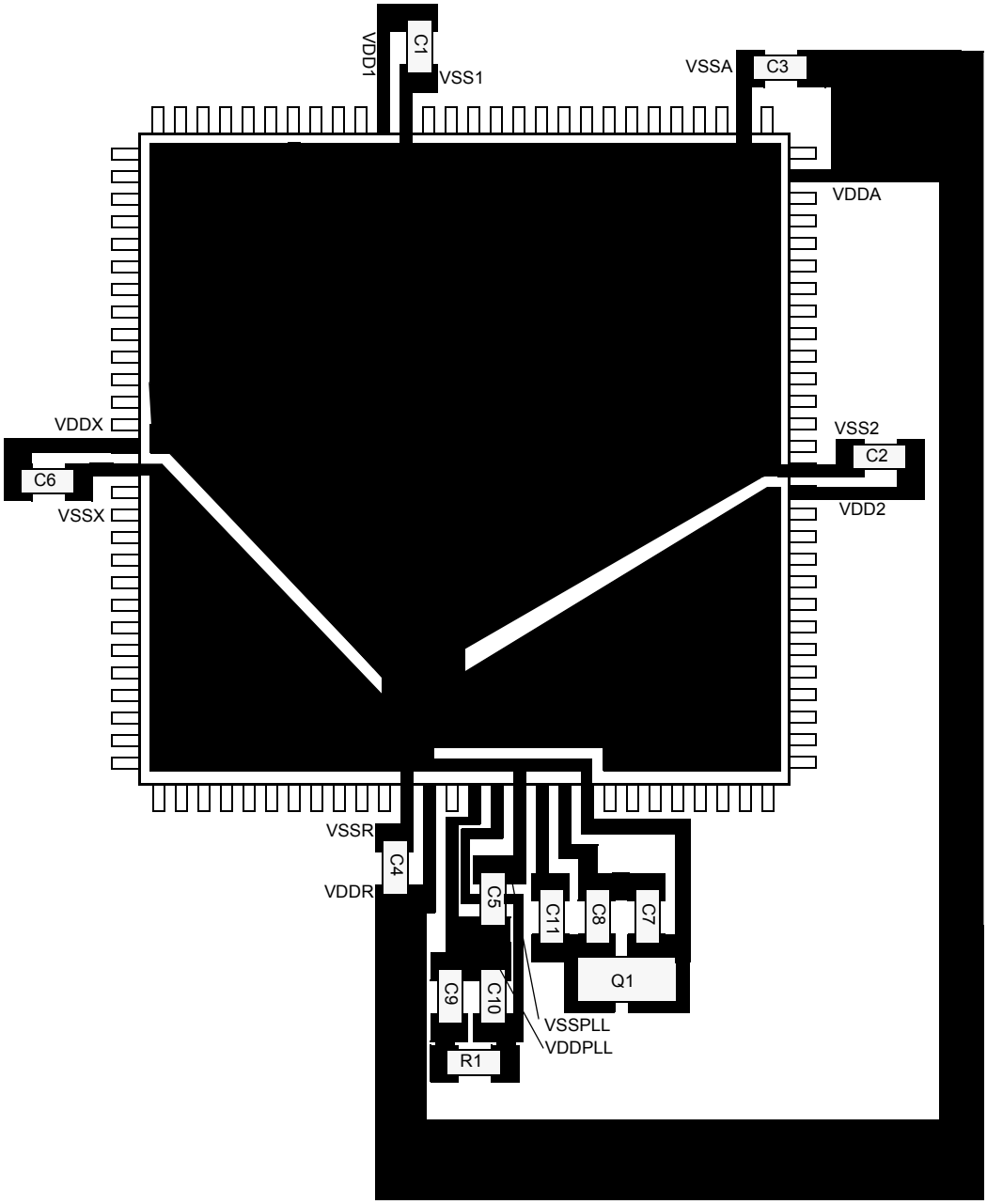
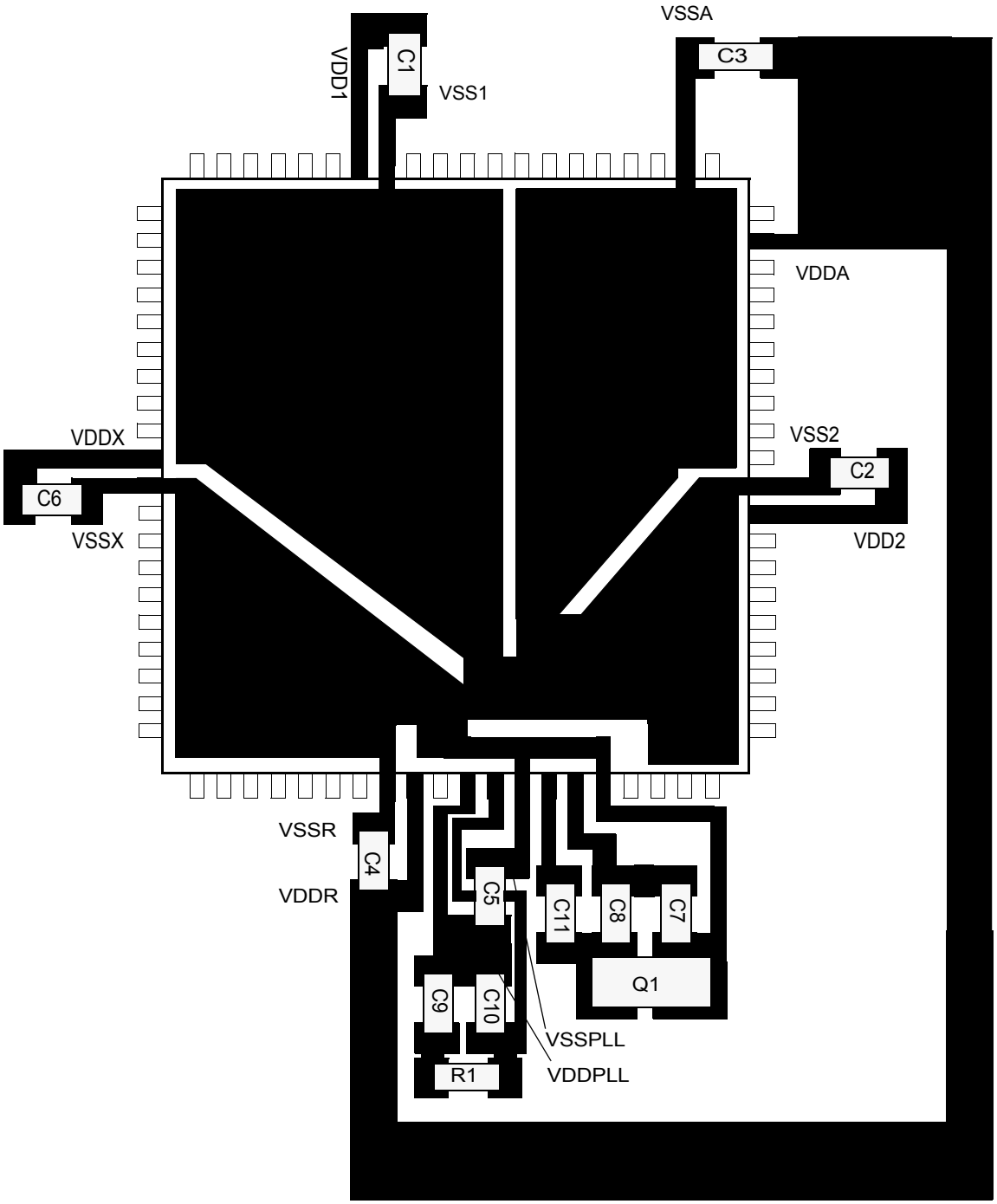


Figure 20-2 Recommended PCB Layout (80 QFP)

NOTE: Oscillator in Colpitts mode.



Appendix A Electrical Characteristics

A.1 General

NOTE: *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values cannot be guaranteed by Motorola and are subject to change without notice.*

NOTE: *The part is specified and tested over the 5V and 3.3V ranges. For the intermediate range, generally the electrical specifications for the 3.3V range apply, but the part is not tested in production test in the intermediate range.*

This supplement contains the most accurate electrical information for the MC9S12E-Family microcontroller available at the time of publication. The information should be considered **PRELIMINARY** and is subject to change.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

NOTE: *This classification will be added at a later release of the specification*

P: Those parameters are guaranteed during production testing on each individual device.

C: Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. They are regularly verified by production monitors.

T: Those parameters are achieved by design characterization on a small sample size from typical devices. All values shown in the typical column are within this category.

D: Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12E-Family utilizes several pins to supply power to the I/O ports, A/D converter, oscillator, PLL and internal logic.

The VDDA, VSSA pair supplies the A/D converter and D/A converter.
The VDDX, VSSX pair supplies the I/O pins
The VDDR, VSSR pair supplies the internal voltage regulator.
VDD1, VSS1, VDD2 and VSS2 are the supply pins for the internal logic.
VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.
VDD1 and VDD2 are internally connected by metal.
VDDA, VDDX, VDDR as well as VSSA, VSSX, VSSR are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDR and VDDX; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted.*
IDD5 denotes the sum of the currents flowing into the VDDA, VDDX and VDDR pins.
VDD is used for VDD1, VDD2 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL.
IDD is used for the sum of the currents flowing into VDD1 and VDD2.

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 3.3V/5V I/O pins

Those I/O pins have a nominal level of 3.3V or 5V depending on the application operating point. This group of pins is comprised of all port I/O pins, the analog inputs, BKGD pin and the RESET inputs.The internal structure of all those pins is identical, however some of the functionality may be disabled.

A.1.3.2 Analog Reference

This group of pins is comprised of the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5}, the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Insure external VDD5 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1 Absolute Maximum Ratings

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	-0.3	6.5	V
2	Internal Logic Supply Voltage[1]	V_{DD}	-0.3	3.0	V
3	PLL Supply Voltage (1)	V_{DDPLL}	-0.3	3.0	V
4	Voltage difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	-0.3	6.5	V
7	Analog Reference	V_{RH}, V_{RL}	-0.3	6.5	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	-0.3	3.0	V
9	TEST input	V_{TEST}	-0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins [2]	I_D	-25	+25	mA
11	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[3]	I_{DL}	-25	+25	mA
12	Instantaneous Maximum Current Single pin limit for TEST[4]	I_{DT}	-0.25	0	mA
13	Operating Temperature Range (packaged)	T_A	– 40	125	°C
14	Operating Temperature Range (junction)	T_J	– 40	140	°C
15	Storage Temperature Range	T_{stg}	– 65	155	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
2. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, V_{SSR} and V_{DDR} or V_{SSA} and V_{DDA}.
3. These pins are internally clamped to V_{SSPLL} and V_{DDPLL}
4. This pin is clamped low to V_{SSR}, but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	-	V
2	C	Machine Model (MM)	V_{MM}	200	-	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	-	V
4	C	Latch-up Current at 125°C positive negative	I_{LAT}	+100 -100	-	mA
5	C	Latch-up Current at 27°C positive negative	I_{LAT}	+200 -200	-	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: *Instead of specifying ambient temperature all parameters are specified for the more meaningful silicon junction temperature. For power dissipation calculations refer to* ***Section A.1.8 Power Dissipation and Thermal Characteristics****.*

Table A-4 Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	3.135	3.3/5	5.5	V
Internal Logic Supply Voltage[1]	V_{DD}	2.35	2.5	2.75	V
PLL Supply Voltage (1)	V_{DDPLL}	2.35	2.5	2.75	V
Voltage Difference VDDX to VDDA	Δ_{VDDX}	-0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.1	0	0.1	V
Oscillator	f_{osc}	0.5	-	16	MHz
Bus Frequency[2]	f_{bus}	0.25	-	25	MHz
Operating Junction Temperature Range	T_J	-40	-	140	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The given operating range applies when this regulator is disabled and the device is powered from an external source.
2. Some blocks e.g. ATD (conversion) and NVMs (program/erase) require higher bus frequencies for proper operation.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_{i} R_{DSON} \cdot I_{IO_i}^{2}$$

Which is the sum of all output currents on I/O ports associated with VDDX and VDDM.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in **Table A-8** and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_{i} R_{DSON} \cdot I_{IO_i}^{2}$$

Which is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-5 Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	–	–	54	°°C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	–	–	41	°C/W
3	T	Junction to Board LQFP112	θ_{JB}	–	–	31	°°C/W
4	T	Junction to Case LQFP112	θ_{JC}	–	–	11	°C/W
5	T	Junction to Package Top LQFP112	Ψ_{JT}	–	–	2	°C/W
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	–	–	51	°°C/W
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	–	–	41	°C/W
8	T	Junction to Board QFP80	θ_{JB}	–	–	27	°°C/W
9	T	Junction to Case QFP80	θ_{JC}	–	–	14	°C/W
10	T	Junction to Package Top QFP80	Ψ_{JT}	–	–	3	°C/W

NOTES:
1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-3
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 3.3V/5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

Table A-6 5V I/O Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD5}	-	-	V
	T	Input High Voltage	V_{IH}	-	-	VDD5 + 0.3	V
2	P	Input Low Voltage	V_{IL}	-	-	0.35*V_{DD5}	V
	T	Input Low Voltage	V_{IL}	VSS5 - 0.3	-	-	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high ohmic input mode)[1] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–2.5	-	2.5	µA
5	C	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –2mA	V_{OH}	V_{DD5} – 0.8	-	-	V
6	P	Output High Voltage (pins in output mode) Full Drive IOH = –10mA	V_{OH}	V_{DD5} – 0.8	-	-	V
7	C	Output Low Voltage (pins in output mode) Partial Drive IOL = +2mA	V_{OL}	-	-	0.8	V
8	P	Output Low Voltage (pins in output mode) Full Drive I_{OL} = +10mA	V_{OL}	-	-	0.8	V
9	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	-130	µA
10	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	-10	-	-	µA
11	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	130	µA
12	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	-	-	µA
13	D	Input Capacitance	C_{in}		6	-	pF
14	T	Injection current[2] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
15	P	Port AD Interrupt Input Pulse filtered[3]	t_{PIGN}			3	µs
16	P	Port AD Interrupt Input Pulse passed(3)	t_{PVAL}	10			µs

NOTES:
1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°C to 12°C in the temperature range from 50°C to 125°C.
2. Refer to **Section A.1.4 Current Injection**, for more details
3. Parameter only applies in STOP or Pseudo STOP mode.

Table A-7 Preliminary 3.3V I/O Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD5}	-	-	V
	T	Input High Voltage	V_{IH}	-	-	VDD5 + 0.3	V
2	P	Input Low Voltage	V_{IL}	-	-	0.35*V_{DD5}	V
	T	Input Low Voltage	V_{IL}	VSS5 - 0.3	-	-	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high ohmic input mode)[1] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–2.5	-	2.5	µA
5	C	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –0.75mA	V_{OH}	V_{DD5} – 0.4	-	-	V
6	P	Output High Voltage (pins in output mode) Full Drive I_{OH} = –4.5mA	V_{OH}	V_{DD5} – 0.4	-	-	V
7	C	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +0.9mA	V_{OL}	-	-	0.4	V
8	P	Output Low Voltage (pins in output mode) Full Drive I_{OL} = +5.5mA	V_{OL}	-	-	0.4	V
9	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	–60	µA
10	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	-6	-	-	µA
11	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	60	µA
12	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	6	-	-	µA
13	D	Input Capacitance	C_{in}		6	-	pF
14	T	Injection current[2] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
15	P	Port AD Interrupt Input Pulse filtered[3]	t_{PIGN}			3	µs
16	P	Port AD Interrupt Input Pulse passed(3)	t_{PVAL}	10			µs

NOTES:
1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°C to 12°C in the temperature range from 50°C to 125°C.
2. Refer to **Section A.1.4 Current Injection**, for more details
3. Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-8 Supply Current Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			65	mA
2	P P	Wait Supply current All modules enabled only RTI enabled	I_{DDW}			40 5	mA
3	 C C C C C C C	Pseudo Stop Current (RTI and COP enabled) [1, 2] -40°C 27°C 70°C 85°C 105°C 125°C 140°C	I_{DDPS}		 570 600 650 750 850 1200 1500		µA
4	 C P C C P C P C P	Pseudo Stop Current (RTI and COP disabled) [(1),(2)] -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDPS}		 370 400 450 550 600 650 800 850 1200	 500 1600 2100 5000	µA
5	 C P C C P C P C P	Stop Current [(2)] -40°C 27°C 70°C 85°C "C" Temp Option 100°C 105°C "V" Temp Option 120°C 125°C "M" Temp Option 140°C	I_{DDS}		 12 30 100 130 160 200 350 400 600	 100 1200 1700 5000	µA

NOTES:
1. PLL off
2. At those low power dissipation levels $T_J = T_A$ can be assumed

Appendix B Electrical Specifications

B.1 Voltage Regulator (VREG_3V3) Operating Characteristics

This section describes the characteristics of the on chip voltage regulator.

Table 20-2 VREG_3V3 - Operating Conditions

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	P	Input Voltages	$V_{VDDR,A}$	3.135	—	5.5	V
2	P	Regulator Current Reduced Power Mode Shutdown Mode	I_{REG}	— —	20 12	50 40	µA µA
3	P	Output Voltage Core Full Performance Mode Reduced Power Mode Shutdown Mode	V_{DD}	2.35 1.6 —	2.5 2.5 [1]	2.75 2.75 —	V V V
4	P	Output Voltage PLL Full Performance Mode Reduced Power Mode[2] Reduced Power Mode[3] Shutdown Mode	V_{DDPLL}	2.35 2.0 1.6 —	2.5 2.5 2.5 [4]	2.75 2.75 2.75 —	V V V V
5	P	Low Voltage Interrupt[5] Assert Level Deassert Level	V_{LVIA} V_{LVID}	4.1 4.25	4.37 4.52	4.66 4.77	V V
5	P	Low Voltage Reset[6] Assert Level Deassert Level	V_{LVRA} V_{LVRD}	2.25 —	— —	— 2.55	V V
7	C	Power-on Reset[7] Assert Level Deassert Level	V_{PORA} V_{PORD}	0.97 —	--- ---	— 2.05	V V

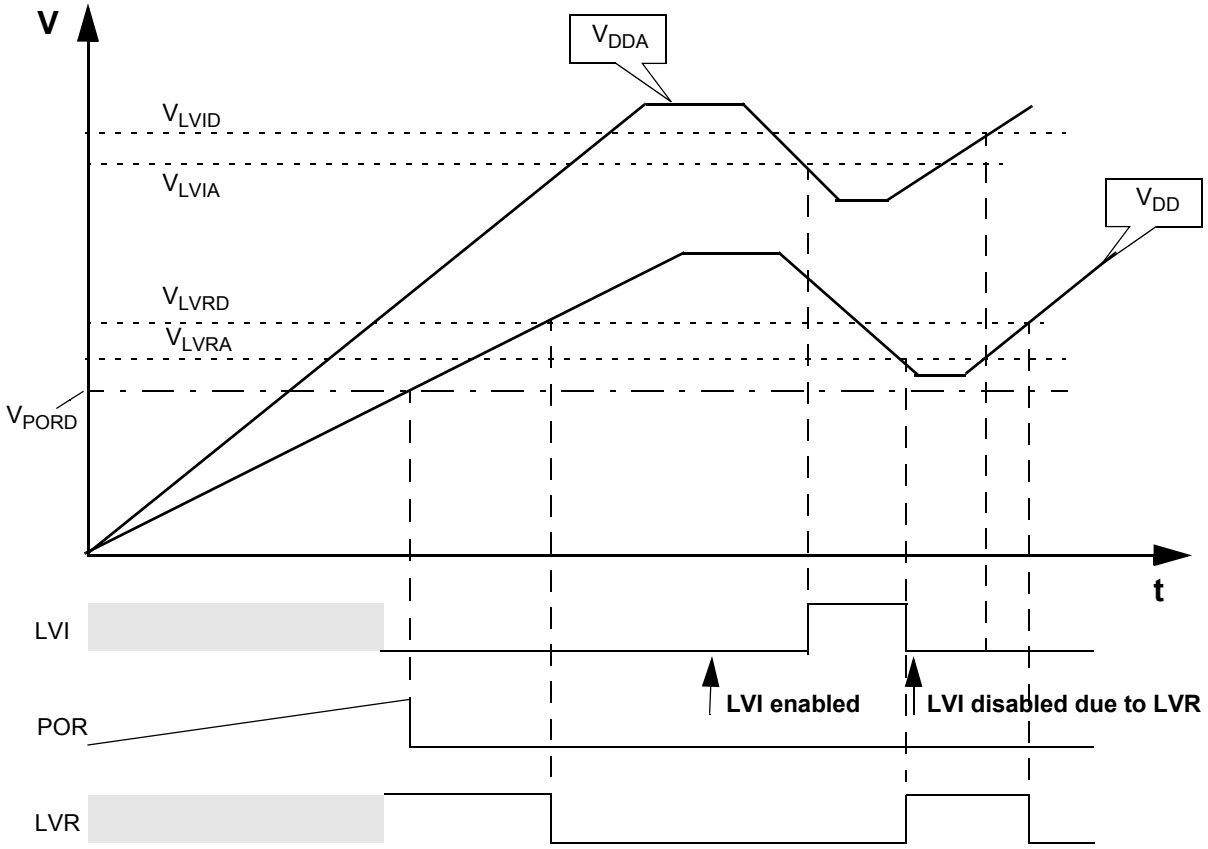
NOTES:
1. High Impedance Output
2. Current IDDPLL = 1mA (Colpitts Oscillator)
3. Current IDDPLL = 3mA (Pierce Oscillator)
4. High Impedance Output
5. Monitors V_{DDA}, active only in Full Performance Mode. Indicates I/O & ADC performance degradation due to low supply voltage.
6. Monitors V_{DD}, active only in Full Performance Mode. V_{LVRA} and V_{PORD} must overlap
7. Monitors V_{DD}. Active in all modes.

NOTE: *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values in this section cannot be guaranteed by Motorola and are subject to change without notice.*

B.2 Chip Power-up and LVI/LVR graphical explanation

Voltage regulator sub modules LVI (low voltage interrupt), POR (power-on reset) and LVR (low voltage reset) handle chip power-up or drops of the supply voltage. Their function is described in **Figure B-1**.

Figure B-1 Voltage Regulator - Chip Power-up and Voltage Drops (not scaled)



B.3 Output Loads

B.3.1 Resistive Loads

The on-chip voltage regulator is intended to supply the internal logic and oscillator circuits allows no external DC loads.

B.3.2 Capacitive Loads

The capacitive loads are specified in **Table B-1**. Ceramic capacitors with X7R dielectricum are required.

Table B-1 Voltage Regulator - Capacitive Loads

Num	Characteristic	Symbol	Min	Typical	Max	Unit
1	VDD external capacitive load	C_{DDext}	200	440	12000	nF
2	VDDPLL external capacitive load	$C_{DDPLLext}$	90	220	5000	nF

B.4 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

B.4.1 Startup

Table B-2 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table B-2 Startup Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	T	POR release level	V_{PORR}			2.07	V
2	T	POR assert level	V_{PORA}	0.97			V
3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
4	D	Startup from Reset	n_{RST}	192		196	n_{osc}
5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
6	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}
7	P	LVR release level	V_{LVRR}	2.25			V
8	P	LVR assert level	V_{LVRA}			2.55	V

B.4.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

B.4.1.2 LVR

The release level V_{LVRR} and the assert level V_{LVRA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the LVR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

B.4.1.3 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

B.4.1.4 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

B.4.1.5 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

B.4.1.6 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

B.4.2 Oscillator

The device features an internal Colpitts and Pierce oscillator. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the $\overline{\text{XCLKS}}$ signal which is sampled during reset. Pierce oscillator/external clock mode allows the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA}.

Table B-3 Oscillator Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1a	C	Crystal oscillator range (Colpitts)	f_{OSC}	0.5		16	MHz
1b	C	Crystal oscillator range (Pierce) [1]	f_{OSC}	0.5		40	MHz
2	P	Startup Current	i_{OSC}	100			µA
3	C	Oscillator start-up time (Colpitts)	t_{UPOSC}		8[2]	100[3]	ms
4	D	Clock Quality check time-out	t_{CQOUT}	0.45		2.5	s
5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency [4]	f_{EXT}	0.5		50	MHz
7	D	External square wave pulse width low(4)	t_{EXTL}	9.5			ns
8	D	External square wave pulse width high(4)	t_{EXTH}	9.5			ns
9	D	External square wave rise time(4)	t_{EXTR}			1	ns
10	D	External square wave fall time(4)	t_{EXTF}			1	ns
11	D	Input Capacitance (EXTAL, XTAL pins)	C_{IN}		7		pF
12	C	DC Operating Bias in Colpitts Configuration on EXTAL Pin	V_{DCBIAS}		1.1		V
13	P	EXTAL Pin Input High Voltage(4)	$V_{IH,EXTAL}$	$0.7*V_{DDPLL}$			V
	T	EXTAL Pin Input High Voltage(4)	$V_{IH,EXTAL}$			V_{DDPLL} + 0.3	V
14	P	EXTAL Pin Input Low Voltage(4)	$V_{IL,EXTAL}$			$0.3*V_{DDPLL}$	V
	T	EXTAL Pin Input Low Voltage(4)	$V_{IL,EXTAL}$	V_{SSPLL} - 0.3			V
15	C	EXTAL Pin Input Hysteresis(4)	$V_{HYS,EXTAL}$		250		mV

NOTES:
1. Depending on the crystal a damping series resistor might be necessary
2. f_{osc} = 4MHz, C = 22pF.
3. Maximum value is for extreme cases using high Q, low frequency crystals
4. Only valid if Pierce oscillator/external clock mode is selected

B.4.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

B.4.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

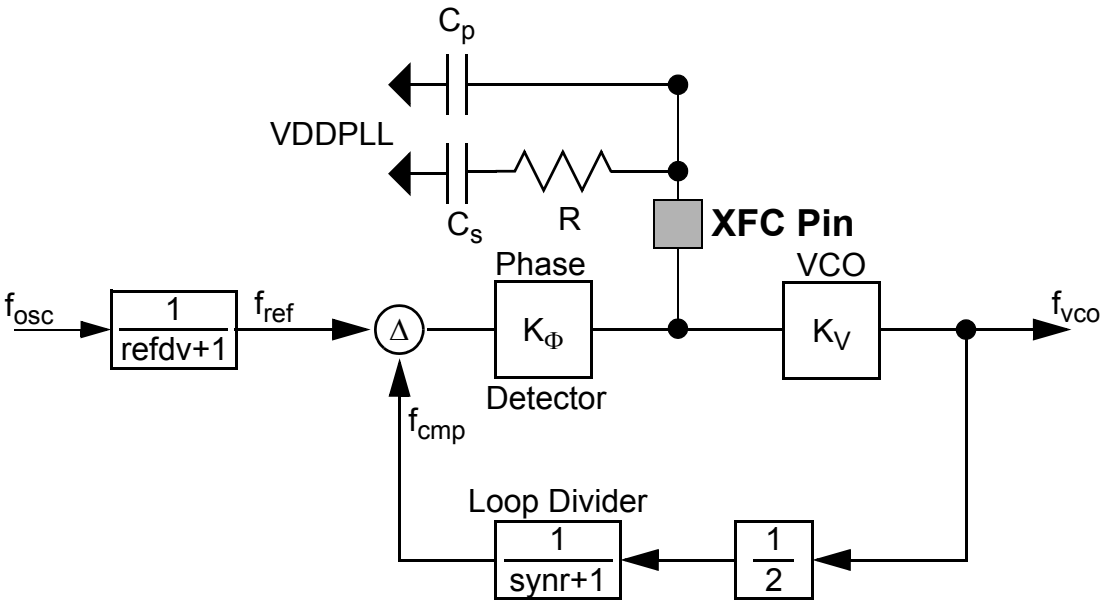


Figure B-2 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **Table B-4**.

The grey boxes show the calculation for f_{VCO} = 50MHz and f_{ref} = 1MHz. E.g., these frequencies are used for f_{OSC} = 4MHz and a 25MHz bus clock.

The VCO Gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}} = -100 \cdot e^{\frac{(60-50)}{-100}} = -90.48\text{MHz/V}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot \left(\zeta + \sqrt{1 + \zeta^2}\right)} \text{ Þ } \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10};(\zeta = 0.9)$$

$f_C < 25kHz$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (synr + 1) \quad = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth f_C=10kHz:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} \quad = 2*\pi*50*10kHz/(316.7Hz/\Omega)=9.9k\Omega=\sim 10k\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R};(\zeta = 0.9) \quad = 5.19nF =\sim 4.7nF$$

The capacitance C_p should be chosen in the range of:

$$C_s / 20 \leq C_p \leq C_s / 10 \quad C_p = 470pF$$

B.4.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure B-2**. With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure B-3**.

NOTE: *This section is under construction*

The basic functionality of the PLL is shown in **Figure B-2**. With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted

accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure B-3**.

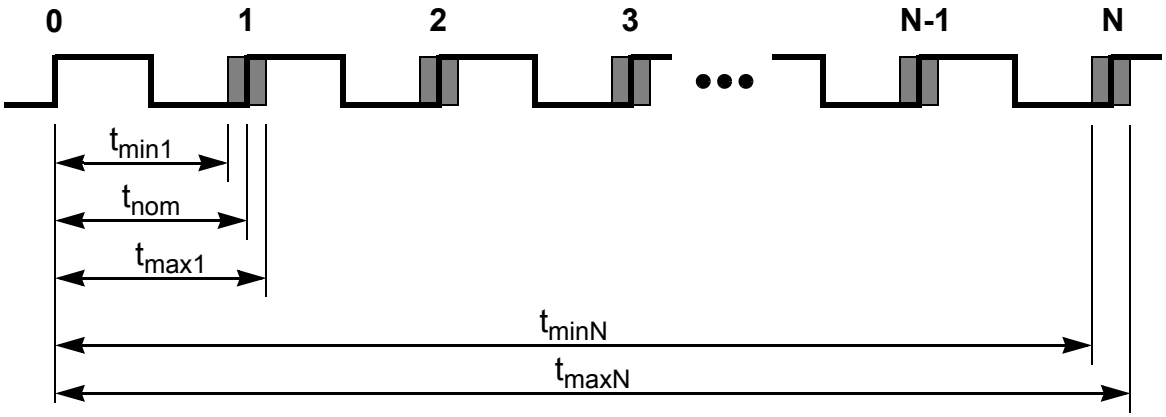


Figure B-3 Jitter Definitions

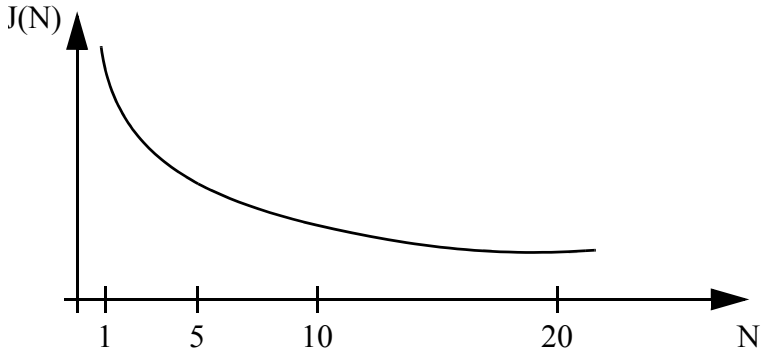
The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$



This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table B-4 PLL Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		50	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3		4	%[1]
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%(1)
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%(1)
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6		8	%(1)
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}		0.5		ms
8	D	PLLON Acquisition mode stabilization delay (2)	t_{acq}		0.3		ms
9	D	PLLON Tracking mode stabilization delay (2)	t_{al}		0.2		ms
10	D	Fitting parameter VCO loop gain	K_1		-100		MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		60		MHz
12	D	Charge pump current acquisition mode	$\| i_{ch} \|$		38.5		µA
13	D	Charge pump current tracking mode	$\| i_{ch} \|$		3.5		µA
14	C	Jitter fit parameter 1(2)	j_1			1.1	%
15	C	Jitter fit parameter 2(2)	j_2			0.13	%

NOTES:
1. % deviation from target frequency
2. f_{OSC} = 4MHz, f_{BUS} = 25MHz equivalent f_{VCO} = 50MHz: REFDV = #$03, SYNR = #$018, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.

B.5 Flash NVM

B.5.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV register. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in **Table B-5** are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

B.5.1.1 Single Word Programming

The programming time for single word programming is dependent on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

B.5.1.2 Row Programming

Flash programming where up to 32 words in a row can be programmed consecutively by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm}$$

Row programming is more than 2 times faster than single word programming.

B.5.1.3 Sector Erase

Erasing a 512 byte Flash sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup times can be ignored for this operation.

B.5.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup times can be ignored for this operation.

B.5.1.5 Blank Check

The time it takes to perform a blank check on the Flash is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table B-5 NVM Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5		50[1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46[2]		74.5[3]	µs
5	D	Flash Burst Programming consecutive word	t_{bwpgm}	20.4[2]		31[3]	µs
6	D	Flash Burst Programming Time for 32 Words	t_{brpgm}	678.4[2]		1035.5[3]	µs
7	P	Sector Erase Time	t_{era}	20[4]		26.7[3]	ms
8	P	Mass Erase Time	t_{mass}	100[4]		133[3]	ms
9	D	Blank Check Time Flash per block	t_{check}	11[5]		32778[6]	t_{cyc}

NOTES:
1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.
3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f bus. Refer to formulae in Sections A.3.1.1 - A.3.1.4 for guidance.
4. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}.
5. Minimum time, if first word in the array is not blank
6. Maximum time to complete check on an erased block.

B.5.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at <2ppm defects over lifetime at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

NOTE: *All values shown in **Table B-6** are target values and subject to further extensive characterization.*

Table B-6 NVM Reliability Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Data Retention at an average junction temperature of T_{Javg} = 85°C	t_{NVMRET}	15			Years
2	C	Data Retention at a junction temperature of T_J = 140°C	t_{NVMRET}	10			Years
3	C	Flash number of Program/Erase cycles	n_{FLPE}	10,000			Cycles

B.6 SPI Characteristics

This section provides electrical parametrics and ratings for the SPI.

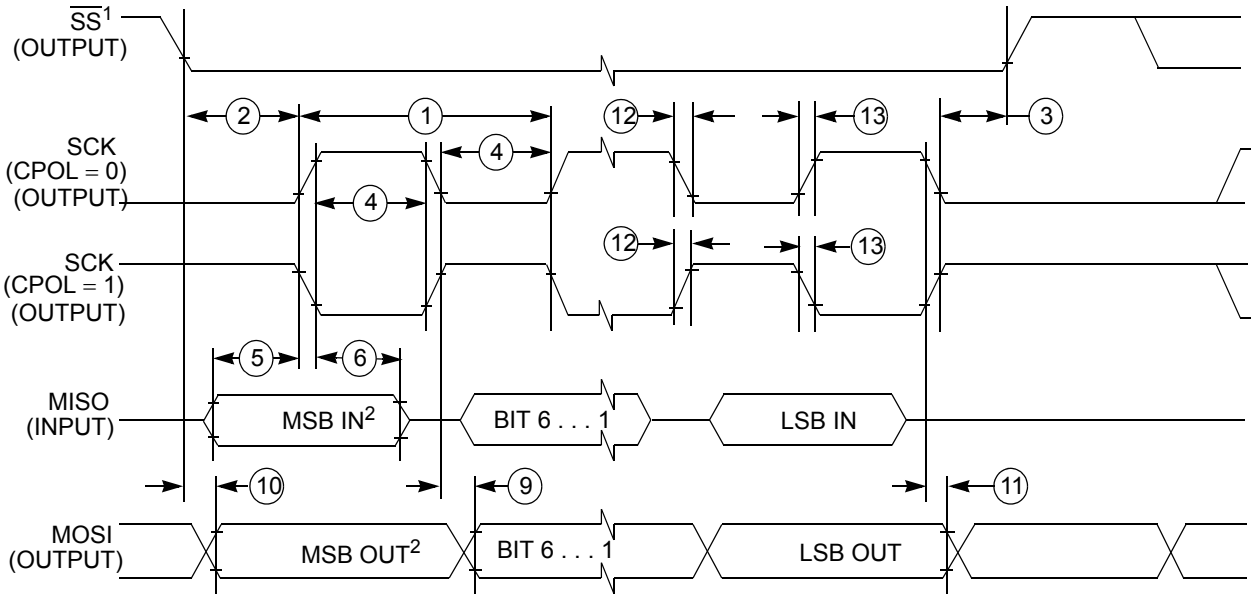
In **Table B-7** the measurement conditions are listed.

Table B-7 Measurement Conditions

Description	Value	Unit
Drive mode	full drive mode	—
Load capacitance C_{LOAD}, on all outputs	50	pF
Thresholds for delay measurement points	(20% / 80%) VDDX	V

B.6.1 Master Mode

In **Figure B-4** the timing diagram for master mode with transmission format CPHA=0 is depicted.

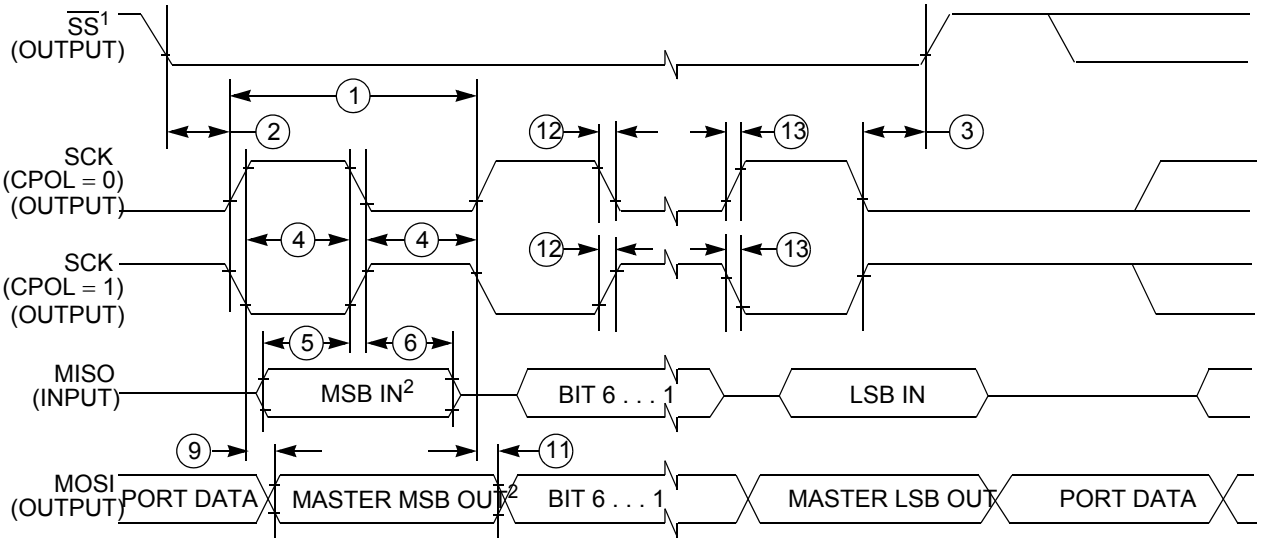


1.if configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure B-4 SPI Master Timing (CPHA=0)

In **Figure B-5** the timing diagram for master mode with transmission format CPHA=1 is depicted.



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure B-5 SPI Master Timing (CPHA=1)

In **Table B-8** the timing characteristics for master mode are listed.

Table B-8 SPI Master Mode Timing Characteristics

Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1	P	SCK Frequency	f_{sck}	1/2048	—	1/2	f_{bus}
1	P	SCK Period	t_{sck}	2	—	2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	—	1/2	—	t_{sck}
3	D	Enable Lag Time	t_{lag}	—	1/2	—	t_{sck}
4	D	Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5	D	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	D	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
9	D	Data Valid after SCK Edge	t_{vsck}	—	—	30	ns
10	D	Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	15	ns
11	D	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	D	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	D	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

B.6.2 Slave Mode

In **Figure B-6** the timing diagram for slave mode with transmission format CPHA=0 is depicted.

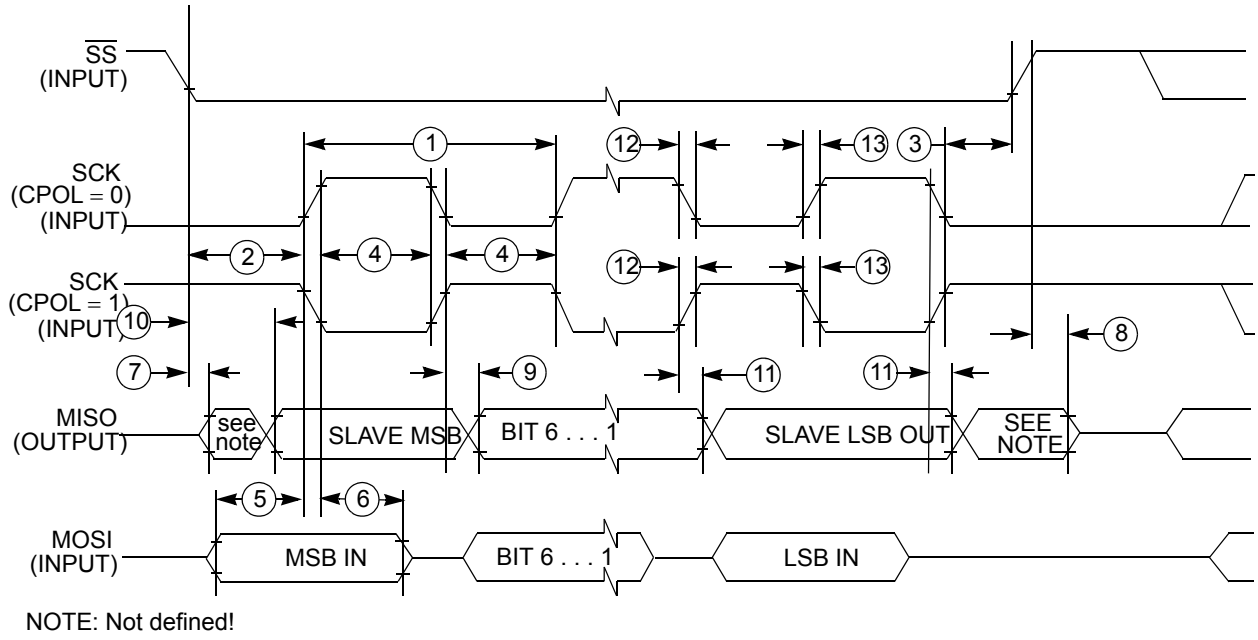


Figure B-6 SPI Slave Timing (CPHA=0)

In **Figure B-7** the timing diagram for slave mode with transmission format CPHA=1 is depicted.

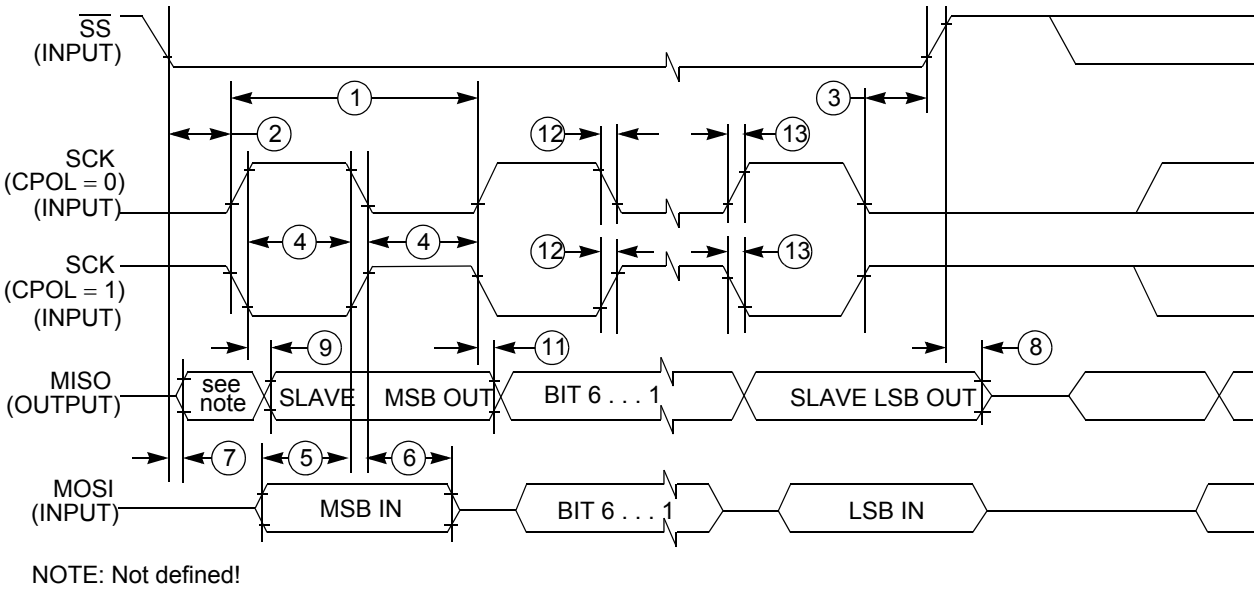


Figure B-7 SPI Slave Timing (CPHA=1)

In **Table B-9** the timing characteristics for slave mode are listed.

Table B-9 SPI Slave Mode Timing Characteristics

Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1	P	SCK Frequency	f_{sck}	DC	—	1/4	f_{bus}
1	P	SCK Period	t_{sck}	4	—	∞	t_{bus}
2	D	Enable Lead Time	t_{lead}	4	—	—	t_{bus}
3	D	Enable Lag Time	t_{lag}	4	—	—	t_{bus}
4	D	Clock (SCK) High or Low Time	t_{wsck}	4	—	—	t_{bus}
5	D	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	D	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
7	D	Slave Access Time (time to data active)	t_a	—	—	20	ns
8	D	Slave MISO Disable Time	t_{dis}	—	—	22	ns
9	D	Data Valid after SCK Edge	t_{vsck}	—	—	30 + t_{bus} [1]	ns
10	D	Data Valid after $\overline{SS}$ fall	t_{vss}	—	—	30 + t_{bus} [1]	ns
11	D	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	D	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	D	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

NOTES:
1. t_{bus} added due to internal synchronization delay

B.7 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

The ATD is specified and tested for both the 3.3V and 5V range. For ranges between 3.3V and 5V the ATD accuracy is generally the same as in the 3.3V range but is not tested in this range in production test.

B.7.1 ATD Operating Characteristics - 5V Range

The **Table B-10** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
VSSA ≤ VRL ≤ VIN ≤ VRH ≤ VDDA. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table B-10 5V ATD Operating Characteristics

Conditions are shown in **Table A-4** unless otherwise noted. Supply Voltage 5V-10% <= VDDA <=5V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 VRL VRH	 VSSA VDDA/2		 VDDA/2 VDDA	 V V
2	C	Differential Reference Voltage[1]	VRH-VRL	4.75	5.0	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} Conv, Time at 4.0MHz[3] ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10} T_{CONV10}	 14 7 3.5		 28 14 7	 Cycles µs µs
5	D	ATD 8-Bit Conversion Period Clock Cycles(1) Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Stop Recovery Time (V_{DDA}=5.0 Volts)	t_{SR}			20	µs
7	P	Reference Supply current	I_{REF}			0.375	mA

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 4.75V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.
3. Reduced accuracy see **Table B-13** and **Table B-14**.

B.7.2 ATD Operating Characteristics - 3.3V Range

The **Table B-11** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
VSSA ≤ VRL ≤ VIN ≤ VRH ≤ VDDA. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table B-11 3.3V ATD Operating Characteristics

Conditions are shown in **Table A-4** unless otherwise noted; Supply Voltage 3.3V-10% <= V_{DDA} <= 3.3V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage	$V_{RH}-V_{RL}$	3.0	3.3	3.6	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[1] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} Conv, Time at 4.0MHz[2] ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10} T_{CONV10}	 14 7 3.5		 28 14 7	 Cycles µs µs
5	D	ATD 8-Bit Conversion Period Clock Cycles(1) Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Recovery Time (V_{DDA}=3.3 Volts)	t_{REC}			20	µs
7	P	Reference Supply current	I_{REF}			0.250	mA

NOTES:
1. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.
2. Reduced accuracy see **Table B-13** and **Table B-14**.

B.7.3 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

B.7.3.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** and **Table A-7**in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance are allowed.

B.7.3.2 Source capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

B.7.3.3 Current injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF ($FF in 8-bit mode) for analog inputs greater than VRH and $000 for values less than VRL unless the current is higher than specified as disruptive conditions.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.
   The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table B-12 ATD Electrical Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Max input Source Resistance	R_S	-	-	1	KΩ
2	T	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}			 10 15	pF
3	C	Disruptive Analog Input Current	I_{NA}	-2.5		2.5	mA
4	C	Coupling Ratio positive current injection	K_p			10^{-4}	A/A
5	C	Coupling Ratio negative current injection	K_n			10^{-2}	A/A

B.7.4 ATD accuracy - 5V Range

Table B-13 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table B-13 5V ATD Conversion Performance

Conditions are shown in **Table A-4** unless otherwise noted $V_{REF} = V_{RH} - V_{RL}$ = 5.12V. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV f_{ATDCLK} = 2.0MHz							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	10-Bit Resolution	LSB		5		mV
2	P	10-Bit Differential Nonlinearity	DNL	–1		1	Counts
3	P	10-Bit Integral Nonlinearity	INL	–2.0		2.0	Counts
4	P	10-Bit Absolute Error[1]	AE	-2.5		2.5	Counts
5	C	10-Bit Absolute Error at f_{ATDCLK}= 4MHz	AE		±7.0		Counts
6	P	8-Bit Resolution	LSB		20		mV
7	P	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
8	P	8-Bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
9	P	8-Bit Absolute Error(1)	AE	-1.5	±1.0	1.5	Counts

NOTES:
1. These values include quantization error which is inherently 1/2 count for any A/D converter.

B.7.5 ATD accuracy - 3.3V Range

Table B-14 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table B-14 3.3V ATD Conversion Performance

Conditions are shown in **Table A-4** unless otherwise noted $V_{REF} = V_{RH} - V_{RL}$ = 3.328V. Resulting to one 8 bit count = 13mV and one 10 bit count = 3.25mV f_{ATDCLK} = 2.0MHz							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	10-Bit Resolution	LSB		3.25		mV
2	P	10-Bit Differential Nonlinearity	DNL	–1.5		1.5	Counts
3	P	10-Bit Integral Nonlinearity	INL	–3.5	±1.5	3.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-5	±2.5	5	Counts
5	C	10-Bit Absolute Error at f_{ATDCLK}= 4MHz	AE		±7.0		Counts
6	P	8-Bit Resolution	LSB		13		mV
7	P	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
8	P	8-Bit Integral Nonlinearity	INL	–1.5	±1.0	1.5	Counts
9	P	8-Bit Absolute Error(1)	AE	-2.0	±1.5	2.0	Counts

NOTES:
1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure B-8**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

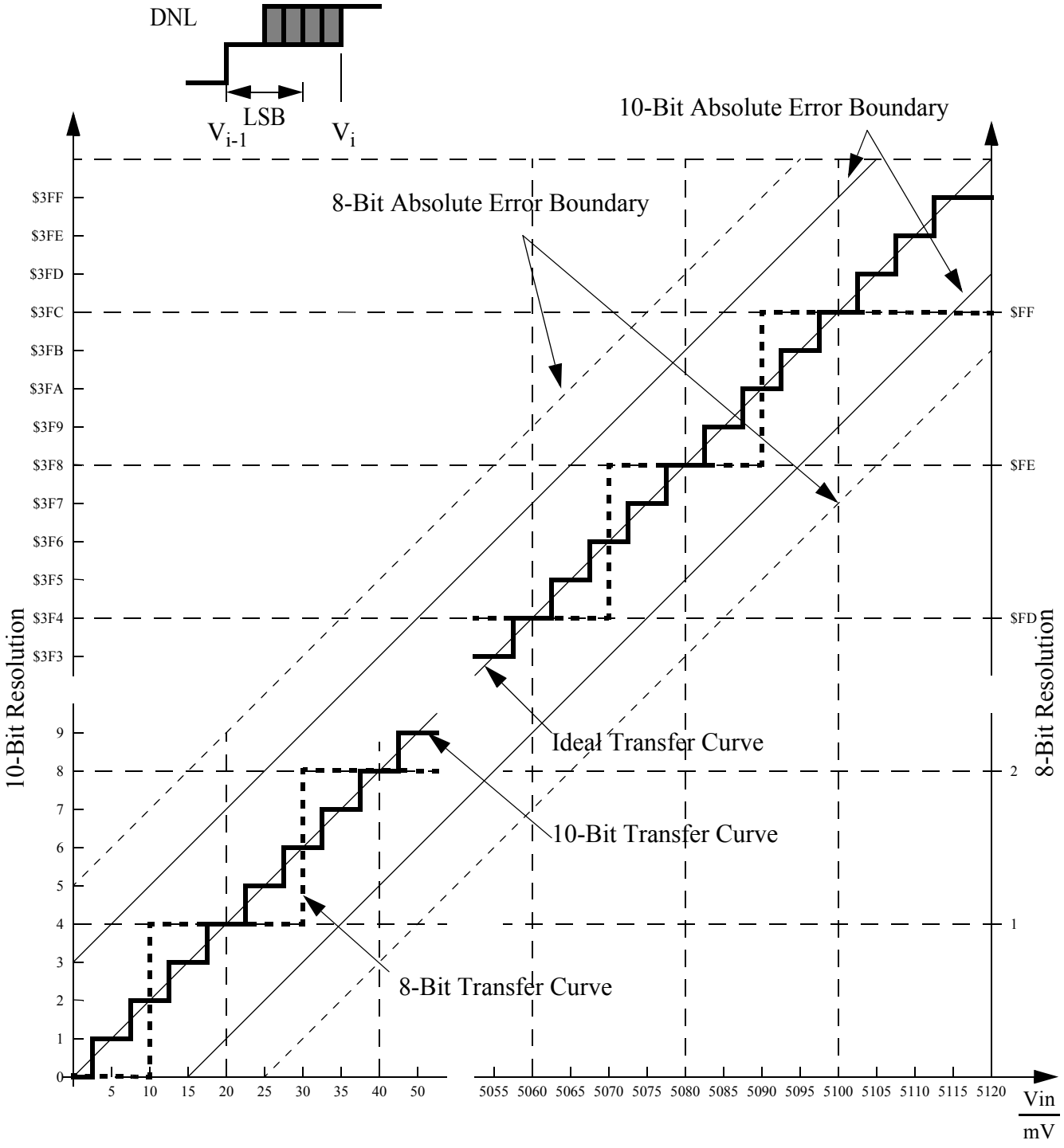


Figure B-8 ATD Accuracy Definitions

NOTE:Figure B-8 *shows only definitions, for specification values refer to* ***Table B-13*** *and* ***Table B-14****.*

B.8 DAC Characteristics

This section describes the characteristics of the digital to analog converter.

B.8.1 DAC Operating Characteristics

Table B-15 DAC Electrical Characteristics (Operating)

Num	C	Characteristic	Condition	Symbol	Min	Typ	Max	Unit
1	D	DAC Supply		V_{DDA}	3.135	—	5.5	V
2	D	DAC Supply Current	Running	I_{DDArun}	—	—	3.5	mA
	D		Stop (low power)	I_{DDstop}	—	—	1.0	mA
3	D	Reference Potential	Low	V_{SSA}	V_{SSA}	—	V_{SSA}	V
	D		High	V_{REF}	$V_{DDA}/2$	—	V_{DDA}	V
4	D	Reference Supply Current	V_{REF} to V_{SSA}	I_{REF}	—	—	400	mA
5	D	Input Current, Channel Off[1]		I_{OFF}	-200	—	1	μA
6	D	Operating Temperature Range		T	-40	—	125	^0C

Table B-16 DAC Timing/Performance Characteristics

Num	C	Parameters	Condition	Symbol	Min	Typ	Max	Unit
1	D	DAC Operating Frequency	V_{DDA} = 3.0V V_{REF} = TBD	f_{BUS}	—	—	25	MHz
	D		V_{DDA} = 5.5V V_{REF} = TBD	f_{BUS}	—	—	25	
2	D	Integral Non-Linearity		INL	—	0.25	—	Count
3	D	Differential Non-Linearity		DNL	—	0.10	—	Count
4	D	Resolution		RES	—	—	8	Bit
5	D	Settling Time		T_S	5	—	10	μs
6	P	Absolute Accuracy		ABS_{ACC}	-1	—	1	Count
7	D	Offset Error		ERR		+/-2.5		mV

Appendix C External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure C-1** with the actual timing values shown on table **Table C-1**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

Figure C-1 General External Bus Timing

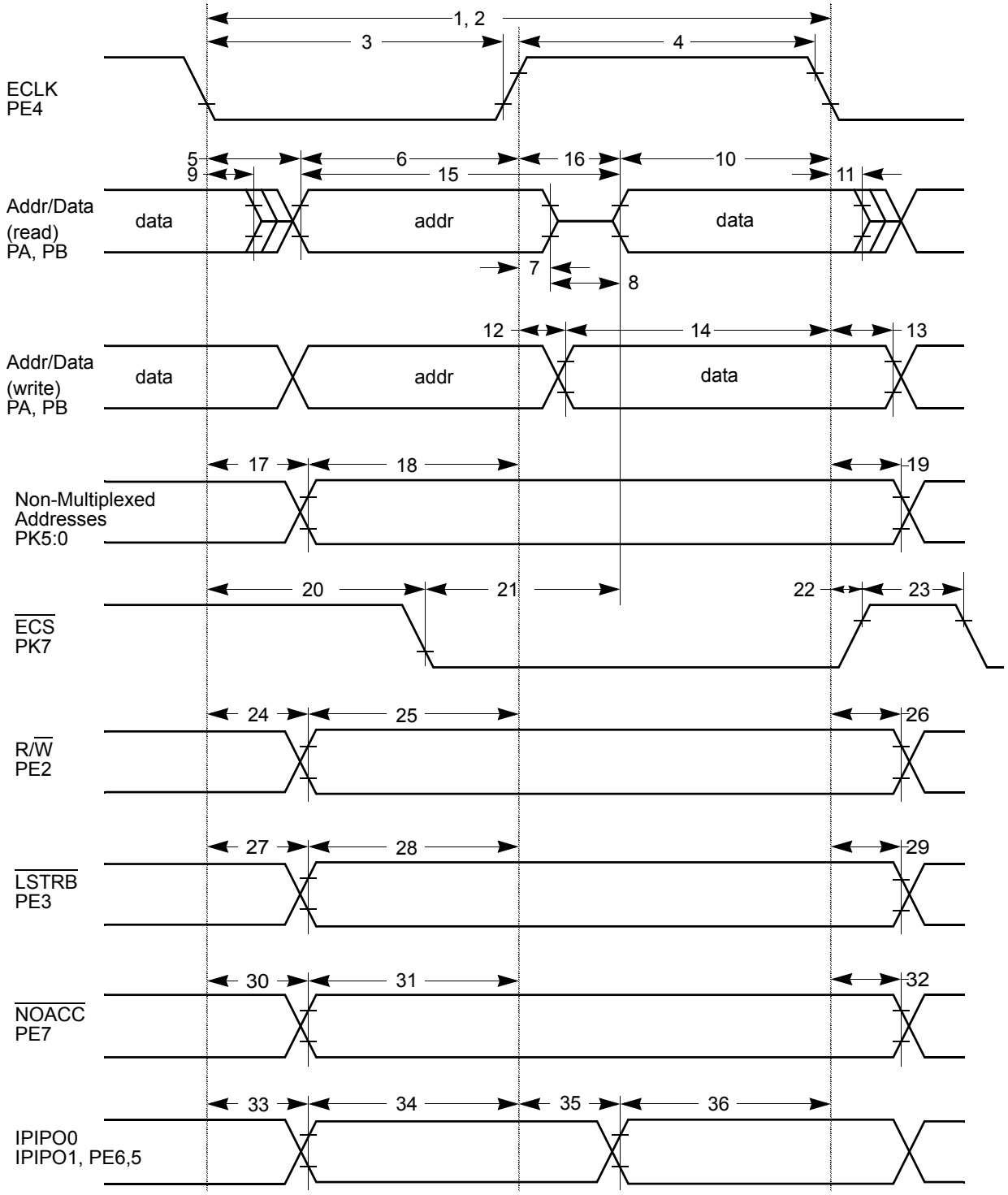


Table C-1 Expanded Bus Timing Characteristics (5V Range)

Conditions are 4.75V < VDDX < 5.25V, Junction Temperature -40°C to +140°C, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Frequency of operation (E-clock)	f_o	0		25.0	MHz
2	P	Cycle time	t_{cyc}	40			ns
3	D	Pulse width, E low	PW_{EL}	19			ns
4	D	Pulse width, E high[1]	PW_{EH}	19			ns
5	D	Address delay time	t_{AD}			8	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	11			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	13			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			7	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time(1) (PW_{EH}–t_{DDW})	t_{DSW}	12			ns
15	D	Address access time(1) (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	19			ns
16	D	E high access time(1) (PW_{EH}–t_{DSR})	t_{ACCE}	6			ns
17	D	Non-multiplexed address delay time	t_{NAD}			6	ns
18	D	Non-muxed address valid to E rise (PW_{EL}–t_{NAD})	t_{NAV}	14			ns
19	D	Non-multiplexed address hold time	t_{NAH}	2			ns
20	D	Chip select delay time	t_{CSD}			16	ns
21	D	Chip select access time(1) (t_{cyc}–t_{CSD}–t_{DSR})	t_{ACCS}	11			ns
22	D	Chip select hold time	t_{CSH}	2			ns
23	D	Chip select negated time	t_{CSN}	8			ns
24	D	Read/write delay time	t_{RWD}			7	ns
25	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	14			ns
26	D	Read/write hold time	t_{RWH}	2			ns
27	D	Low strobe delay time	t_{LSD}			7	ns
28	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	14			ns
29	D	Low strobe hold time	t_{LSH}	2			ns
30	D	NOACC strobe delay time	t_{NOD}			7	ns
31	D	NOACC valid time to E rise (PW_{EL}–t_{NOD})	t_{NOV}	14			ns

Table C-1 Expanded Bus Timing Characteristics (5V Range)

Conditions are 4.75V < VDDX < 5.25V, Junction Temperature -40°C to +140°C, C_{LOAD} = 50pF							
32	D	NOACC hold time	t_{NOH}	2			ns
33	D	IPIPO[1:0] delay time	t_{P0D}	2		7	ns
34	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	11			ns
35	D	IPIPO[1:0] delay time(1) (PW_{EH}-t_{P1V})	t_{P1D}	2		25	ns
36	D	IPIPO[1:0] valid time to E fall	t_{P1V}	11			ns

NOTES:
1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

Table C-2 Expanded Bus Timing Characteristics (3.3V Range)

Conditions are VDDX=3.3V+/-10%, Junction Temperature -40°C to +140°C, C_{LOAD} = 50pF

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Frequency of operation (E-clock)	f_o	0		16.0	MHz
2	P	Cycle time	t_{cyc}	62.5			ns
3	D	Pulse width, E low	PW_{EL}	30			ns
4	D	Pulse width, E high[1]	PW_{EH}	30			ns
5	D	Address delay time	t_{AD}			16	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	16			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	15			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			15	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time(1) (PW_{EH}–t_{DDW})	t_{DSW}	15			ns
15	D	Address access time(1) (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	29			ns
16	D	E high access time(1) (PW_{EH}–t_{DSR})	t_{ACCE}	15			ns
17	D	Non-multiplexed address delay time	t_{NAD}				ns
18	D	Non-muxed address valid to E rise (PW_{EL}–t_{NAD})	t_{NAV}				ns
19	D	Non-multiplexed address hold time	t_{NAH}				ns
20	D	Chip select delay time	t_{CSD}				ns
21	D	Chip select access time(1) (t_{cyc}–t_{CSD}–t_{DSR})	t_{ACCS}				ns
22	D	Chip select hold time	t_{CSH}				ns
23	D	Chip select negated time	t_{CSN}				ns
24	D	Read/write delay time	t_{RWD}			14	ns
25	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	16			ns
26	D	Read/write hold time	t_{RWH}	2			ns
27	D	Low strobe delay time	t_{LSD}			14	ns
28	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	16			ns
29	D	Low strobe hold time	t_{LSH}	2			ns
30	D	NOACC strobe delay time	t_{NOD}			14	ns
31	D	NOACC valid time to E rise (PW_{EL}–t_{NOD})	t_{NOV}	16			ns

Table C-2 Expanded Bus Timing Characteristics (3.3V Range)

Conditions are VDDX=3.3V+/-10%, Junction Temperature -40°C to +140°C, C_{LOAD} = 50pF

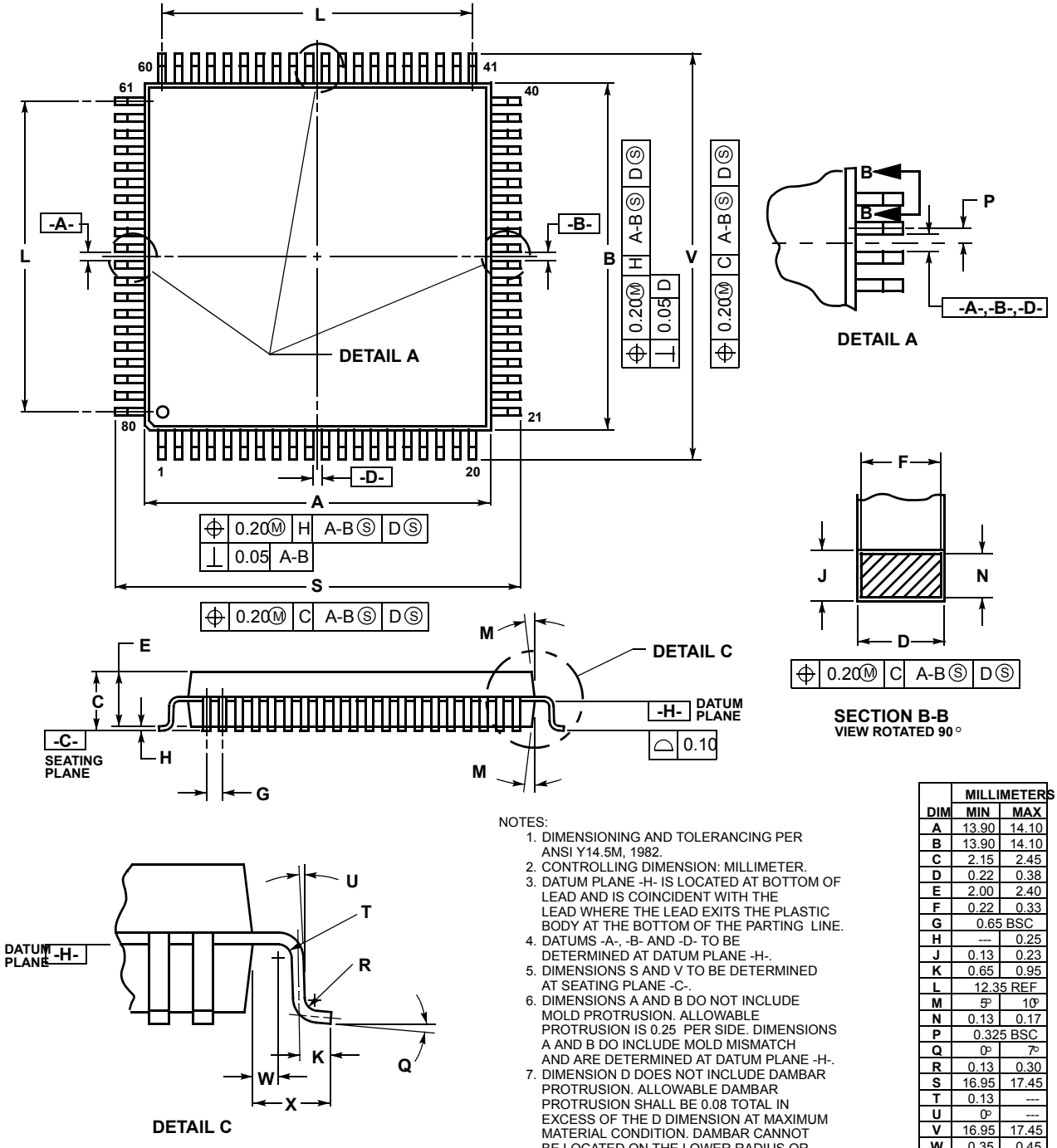
32	D	NOACC hold time	t_{NOH}	2			ns
33	D	IPIPO[1:0] delay time	t_{P0D}	2		14	ns
34	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	16			ns
35	D	IPIPO[1:0] delay time(1) (PW_{EH}-t_{P1V})	t_{P1D}	2		25	ns
36	D	IPIPO[1:0] valid time to E fall	t_{P1V}	11			ns

NOTES:

1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

Appendix D Package Information

D.1 80-pin QFP package

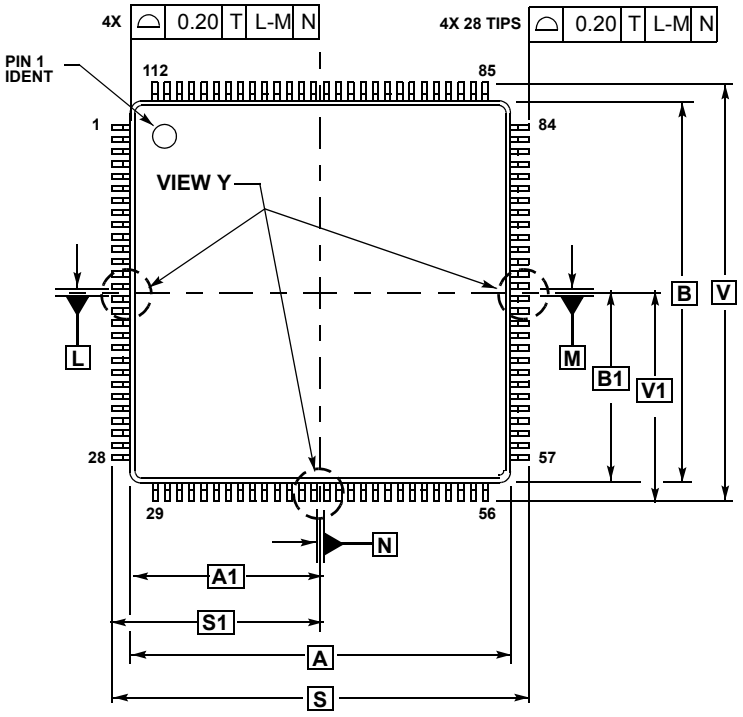


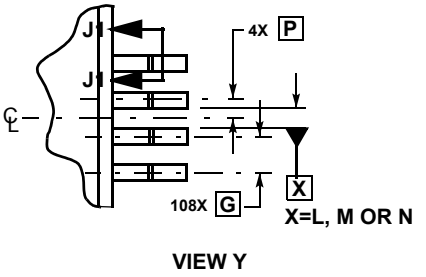
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

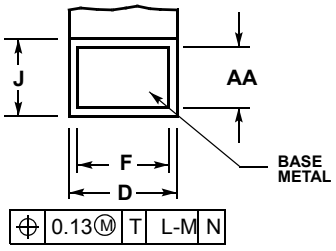
	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

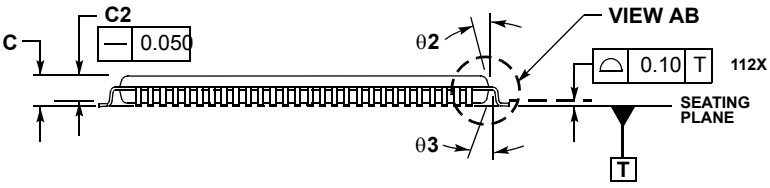
Figure D-1 80-pin QFP Mechanical Dimensions (case no. 841B)

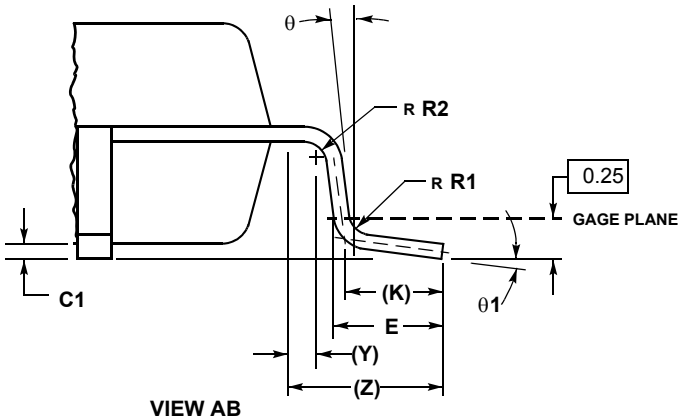
D.2 112-pin LQFP package











NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0 °	8 °
θ1	3 °	7 °
θ2	11 °	13 °
θ3	11 °	13 °

Device User Guide End Sheet

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