DDX-2000/2060

All-Digital High Efficiency Power Amplifier

FEATURES

- HIGH OUTPUT CAPABILITY
  2x35W into 8 Ω @ <1% THD+N
  1x70W into 4 Ω @ <1% THD+N
- SINGLE SUPPLY (+9V to +30V)
- HIGH EFFICIENCY, >88%
- DIGITAL VOLUME CONTROL, ANTI-CLIPPING AND AUTOMATIC MUTE
- THERMAL OVERLOAD AND SHORT CIRCUIT PROTECTION

BENEFITS

- COMPLETE SURFACE MOUNT DESIGN
- SMALL PACKAGE -NO HEAT SINK
- POWER SUPPLY SAVINGS
- ALL DIGITAL - NO DAC

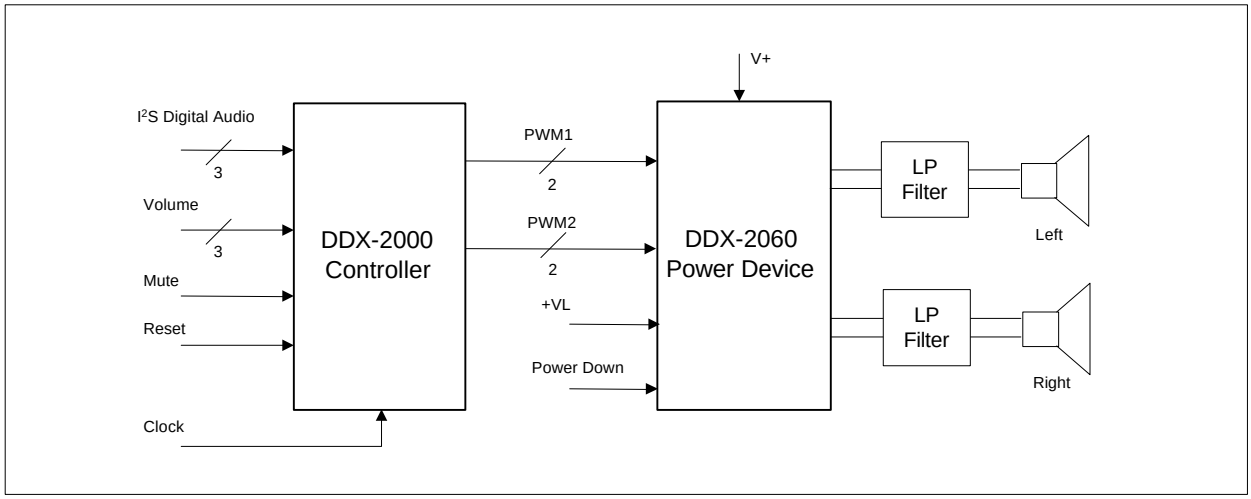
APPLICATIONS

- DIGITAL POWERED SPEAKERS
- PC SOUND CARDS
- CAR AUDIO
- SURROUND SOUND SYSTEMS
- DIGITAL AUDIO COMPONENTS

GENERAL DESCRIPTION

The DDX-2000 Controller and DDX-2060 Power Device is an all-digital stereo amplifier chip set that can provide up to 35 watts per channel of audio power at very high efficiency. The DDX-2000 Controller includes two channels of DDX processing, digital volume control, mute and special processing to reduce distortion associated with signal clipping. The controller accepts standard PCM serial formats and operates from an external 256*Fs clock or from a crystal. The DDX-2060 Power Device is a dual channel Class-D H-Bridge power device that has a logic interface, integrated bridge driver, high efficiency MOSFET output transistors and protection circuitry.

The benefits of this system are the all-digital design that eliminates the need for a digital to analog converter (DAC) and the high efficiency operation derived from the use of Apogee's patented damped ternary pulse width modulation (PWM). This approach provides an efficiency advantage over conventional Class-D designs and up to three times the efficiency of typical Class A/B amplifiers with music input signals.



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November 2001
DOC #1000002-09

Absolute Maximum Ratings [1]

DDX-2000

SYMBOL	PARAMETER	VALUE	UNIT
VL	Power supply voltage	-0.3V to +4.6V	V
Note [2]	Logic Inputs	-0.3V to +6.0V	V
Tstg	Storage temperature range	-40 to +150	°C

DDX-2060

SYMBOL	PARAMETER	VALUE	UNIT
VCC	Power supply voltage	40V	V
VL	Input logic reference	5.5V	V
Tj	Operating junction temperature range	-40 to +150	°C
Tstg	Storage temperature range	-40 to +150	°C

Recommended Operating Conditions [3]

DDX-2000

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VL	Power supply voltage		3.3		V
VIH Note 2	Logic inputs, High	2.0		5.5	V
VIL	Logic inputs, Low			0.8	V
Fs	PCM Input Sample Rate	32		48	KHz
T_A	Ambient Temperature	0		70	°C

DDX-2060

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCC	Power supply voltage	10.0		28.0	V
VL	Input logic reference		3.3		V
VIH	Logic inputs, High	1.7			V
VIL	Logic inputs, Low			0.8	V
IOL	Output Sink current, open-drain FAULT and TWARN		1		mA
T_A	Ambient Temperature	0		70	°C

Thermal Data

DDX-2000

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
θ_{JA}	Thermal resistance junction-ambient			110	°C/W

DDX-2060

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
θ_{JC}	Thermal resistance junction-case (thermal pad)			2.5	°C/W
T_j	Thermal shut-down junction temperature		150		°C
T_h	Thermal shut-down hysteresis		25		°C

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. SCLK, SDATA, LRCLK, VMODE, VCLK/UP, VDATA/DN, SMODE, nRST, ACE, MUTE are 5V input tolerant.
3. Performance not guaranteed beyond recommended operating conditions.

Electrical Characteristics[1]

Refer to circuit Fig. 5. VCC=28V, f=1kHz, TA=25C, RL=8 Ω, and measurement bandwidth 22kHz.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Po	Output power	THD+N <1%		35		Wrms
	Overvoltage Protection Threshold		30	35		V
	Undervoltage Protection Threshold			7	9	V
I_L	VL supply current for DDX-2000	VL= +3.3V		90	100	mA
I_{PD}	Vcc supply current in Powerdown			1	3	mA
I_Q	Vcc quiescent current (Hi-Z State)	Hi-Z State		26		mA
I_{cc}	Vcc supply current	2-Chan. switching at 384KHz.		68		mA
I_{sc}	Short circuit current limit		3.0	5.0	6.5	A
THD+N	Total Harmonic Distortion+Noise	Po=1.0 Wrms Po= 30 Wrms		.08 .33	.18 .50	%
SNR	Signal-to-Noise Ratio	A-weighted		93		dB
η	Efficiency	Po=2 x 20W		87		%
PSRR	Power Supply Rejection Ratio	Vrip= 1 Vrms, 120Hz, -60 db Input		60		dB

1. Characteristics are for the DDX-2060 power device driven by DDX-2000 processor.

DDX-2000 Pin Function Description

Audio Serial Interface (I^2S)

Pin Name	Pin No.	Description
SCLK [1]	1	Input serial clock
SDATA [1]	2	Input serial data
LRCLK [1, 2]	3	Input Left/Right
SMODE [1, 2]	20	Serial Mode Select (0=Left Justified, 1= I^2S. See Figure 3)

Gain/Volume Interface

Pin Name	Pin No.	Description
VMODE [1, 2]	39	Volume Mode Select
VCLK/UP [1, 2]	40	Volume Data Clock or Increment Up
VDATA/DN [1, 2]	41	Volume Serial Data In or Increment Down
ACE [1, 2]	5	Anti-Clipping Enable, Active Hi

System Clocking

Pin Name	Pin No.	Description
XI	11	256*fs Oscillator/External 256*fs clock input
XO	10	256*fs Oscillator
INLP	16	PLL Filter
OUTLP	17	PLL Filter

DDX Output Signals/Control

Pin Name	Pin No.	Description
MUTE [1, 3]	38	Active Hi, sets outputs to damped state
OUTLA	33	Left channel output A
OUTLB	32	Left channel output B
OUTRA	26	Right channel output A
OUTRB	25	Right channel output B

Power Supplies/Miscellaneous

Pin Name	Pin No.	Description
VL	4, 13, 15, 27, 29, 44	Power
GND	9, 12, 14, 18, 19, 28, 34, 35, 37, 42, 43	Ground
nRST [1, 2, 4]	6, 7	System Reset, active low. Both pins must be connected for proper operation.
NC	8, 21, 22, 23, 24, 30, 31, 36	No Connect. Must be left open.

1. Denotes 5V input tolerance.
2. Denotes 50k internal pullup.
3. Denotes 50k internal pulldown.
4. Denotes TTL Schmitt Input Buffer. Vt+ = 2.0V max. Vt- = 0.7V min. Typical hysteresis is 0.5V.

DDX 2060 Pin Function Description

PWM Inputs

	Pin No.	Description
	29	Left A logic input signal
INLB		Left B logic input signal
INRA		Right A logic input signal
INRB		Right B logic input signal

Control/Miscellaneous

Pin Name		Description
PWRDN		Power Down (0=Shutdown, 1= Normal).
TRI-	26	Tri- TS Hi-
FAULT [1]	27	
TWARN [1]	28	(0=Warning IC >= 130°C, 1=Normal).
CONFIG [3]		Configuration (0=Normal, 1=Parallel operation for mono).
NC		Do not connect.

Power O

Pin Name	Pin No.	
OUTPL	16, 17	
OUTNL	10, 11	
OUTPR	8, 9	
OUTNR	2, 3	

Pin Name	Pin No.	
VCC[1P, 1N, 2P, 2N]	4, 7, 12, 15	
PGND[1P, 1N, 2P, 2N]	5, 6, 13, 14	
VREG1	21, 22	
VREG2	33, 34	
VSIG	35, 36	Positive supply.
	23	Logic reference voltage.
	19	Logic reference ground.
	1	Substrate ground.
	20	Internal regulator ground.

1. -drain.

2. ase with the input.

Connect CONFIG Pin 24 to VREG1 Pins 21,22 to implement parallel operation for mono.

FIG. 5A - Typical Application Circuit (Signal Processing section)

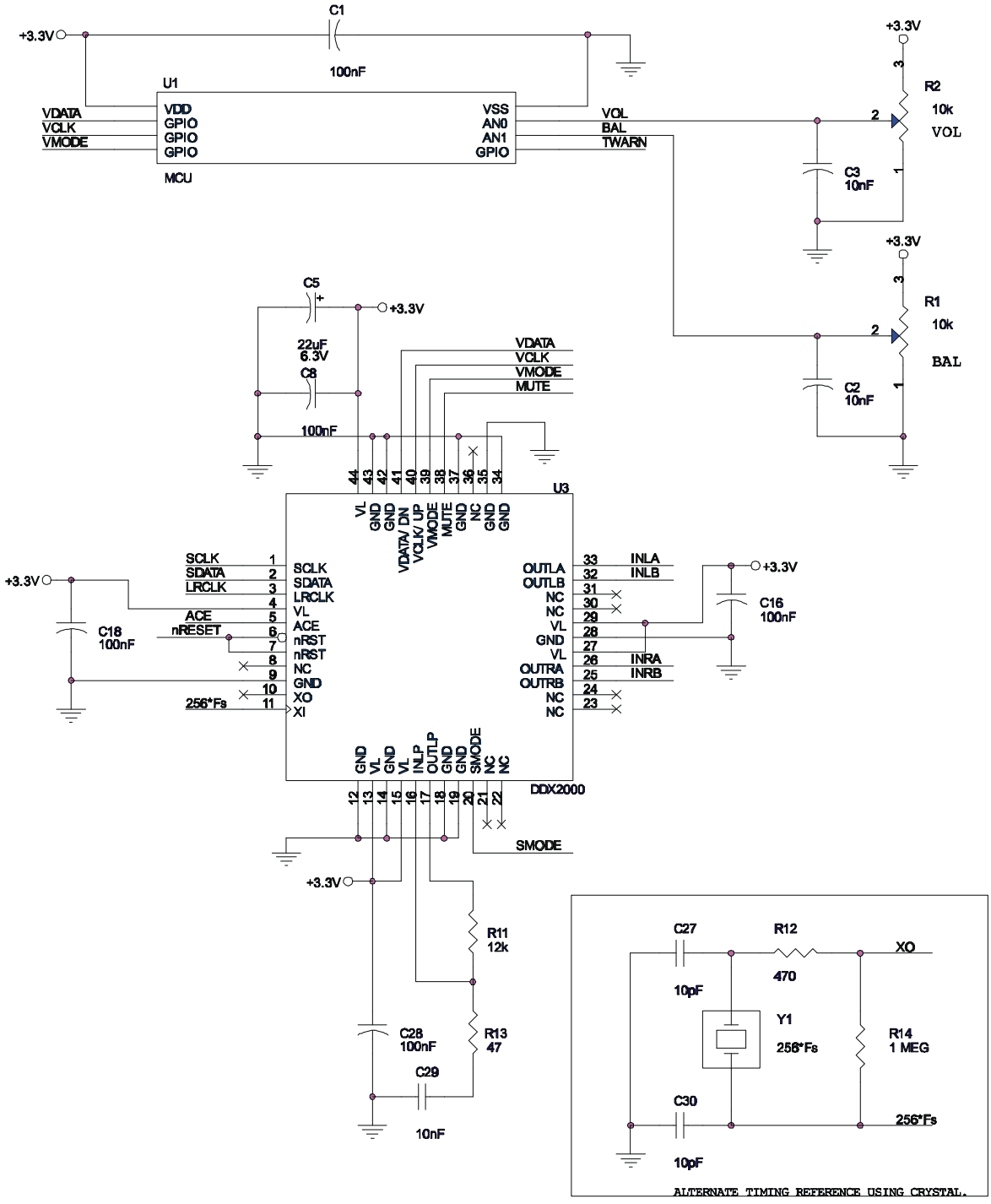
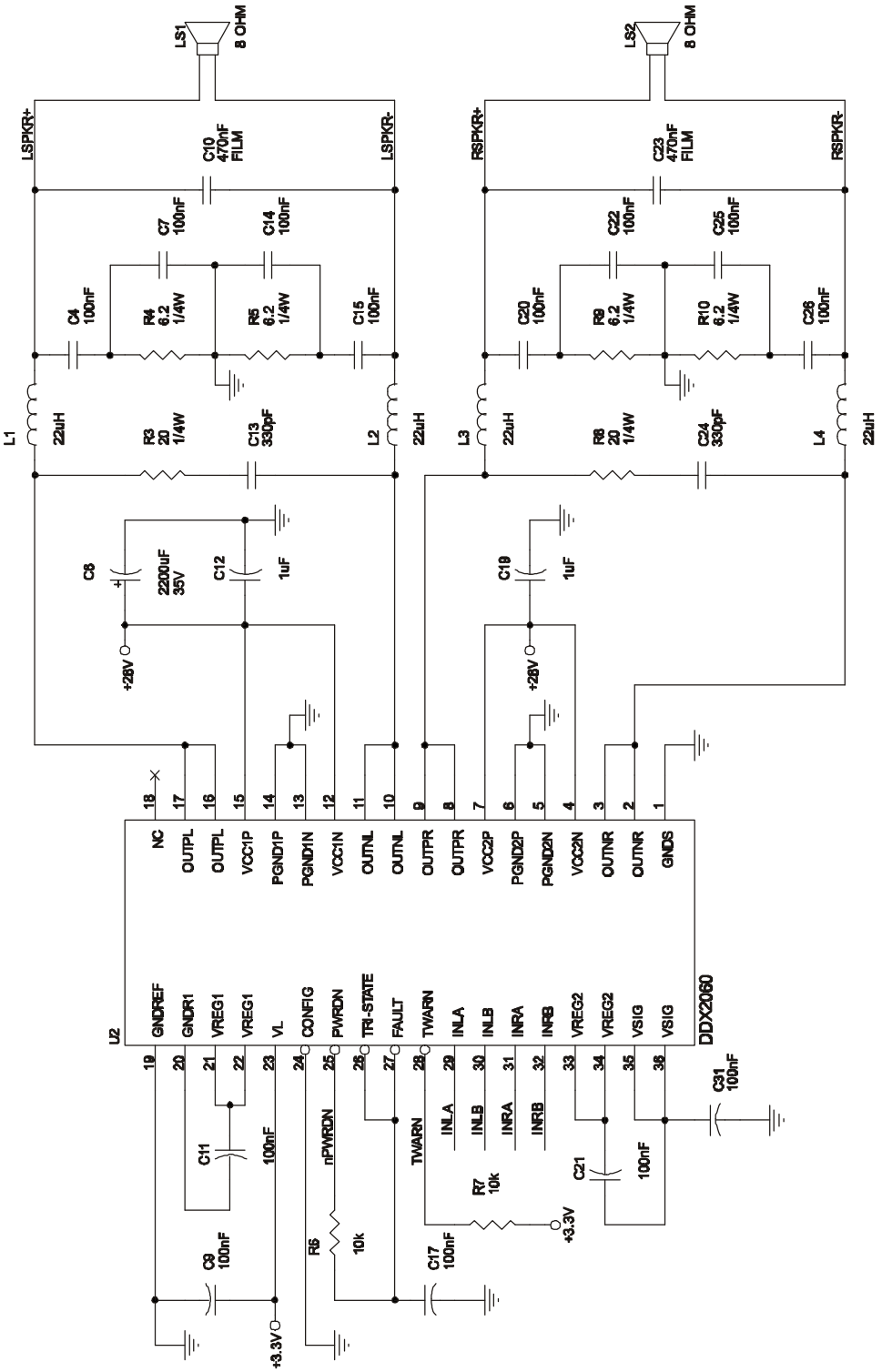


FIG. 5B - Typical Application Circuit (Power section)



Typical Performance Characteristics at Vcc = 28V, 8 Ohm load.

Fig 6: Efficiency vs Output Power

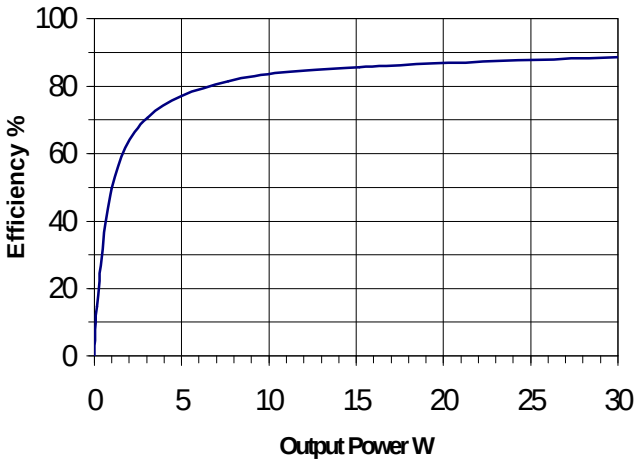


Fig 7: Frequency response

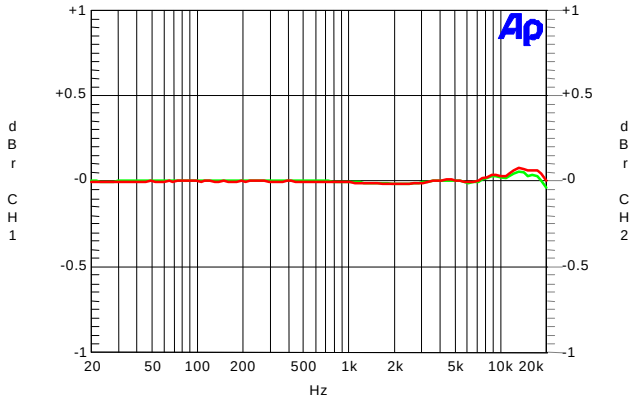


Fig 8: THD+N vs Frequency

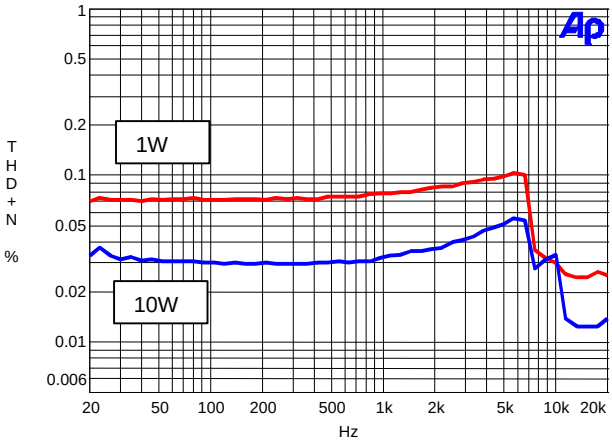
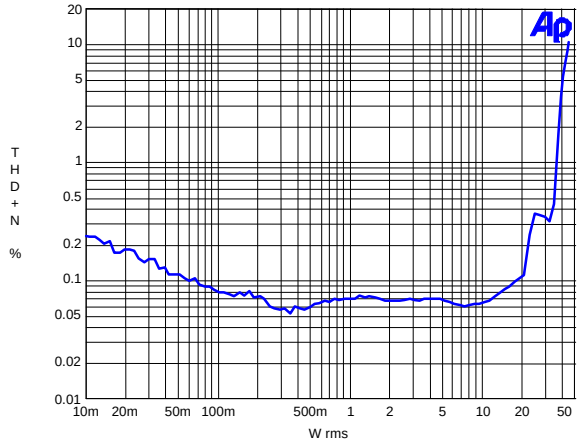


Fig 9: THD+N vs Outpwr at 1 KHz
(w/ ANTICLIPPING DISABLED)



Typical Performance Characteristics at Vcc = 24V, 4 Ohm load.

Fig 10: THD+N vs Frequency

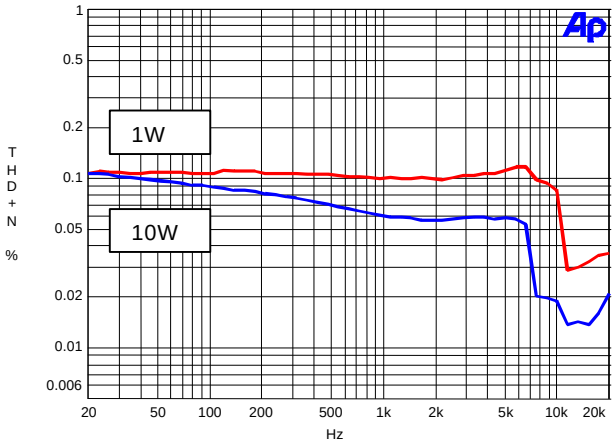
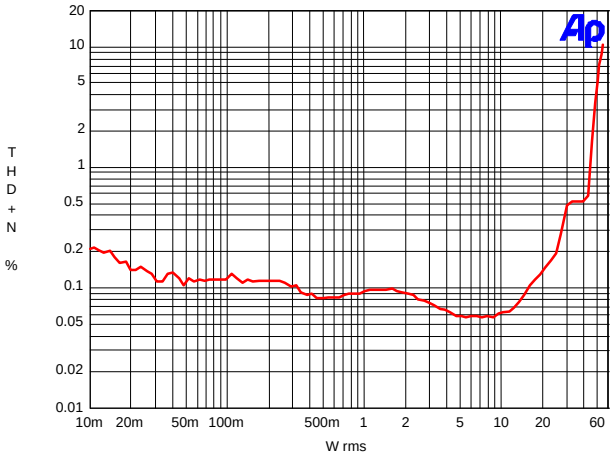


Fig 11: THD+N vs Outpwr at 1 KHz
(w/ ANTICLIPPING DISABLED)



Typical Performance Characteristics at Vcc = 28V, 4 Ohm load, configured for Mono.

Fig 12: THD+N vs Frequency

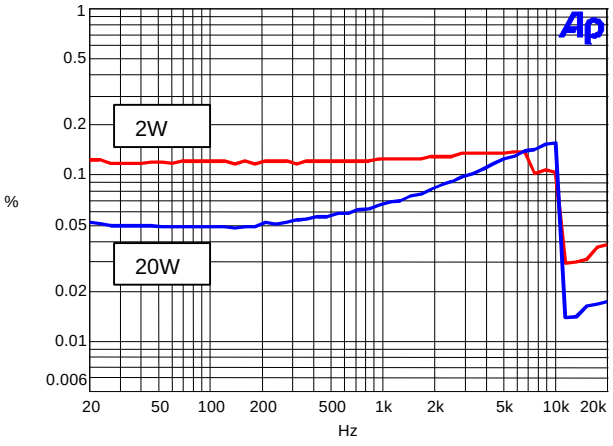
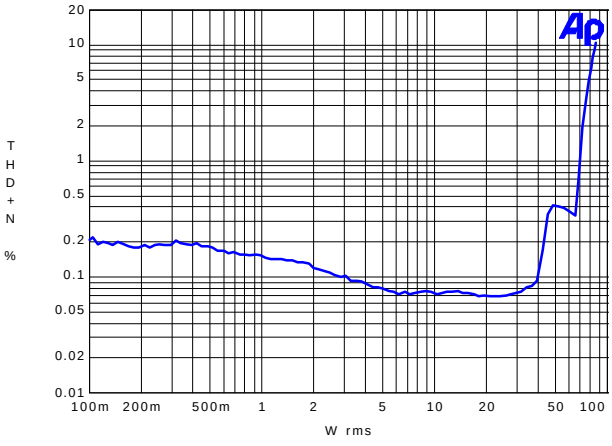


Fig 13: THD+N vs Outpwr at 1 KHz
(w/ ANTICLIPPING DISABLED)



SYSTEM OVERVIEW

The DDX-2000/2060 is an all-digital 2-channel amplifier chip set that delivers up to 35 watts per channel at very high efficiency. The system consists of a DDX-2000 Controller, DDX-2060 Power Device and an output filter. The DDX-2000 Controller accepts standard digital audio data and converts it to PWM logic level signals. The device also includes digital volume, muting and anti-clipping functions. The DDX-2060 is a dual channel H-Bridge that converts DDX-2000 PWM timing signals to power at the load. A passive low pass filter prior to the load attenuates the modulation carrier. The DDX-2060 is protected against over-voltage, thermal and short circuit conditions.

DDX-2000 CONTROLLER

The DDX-2000 Controller is a 3.3V digital integrated circuit that converts serial PCM digital audio signals into Apogee's patented damped ternary outputs. The device supports two modes of digital volume control, mute and anti-clipping functions. A block diagram of the device is shown in Figure 1.

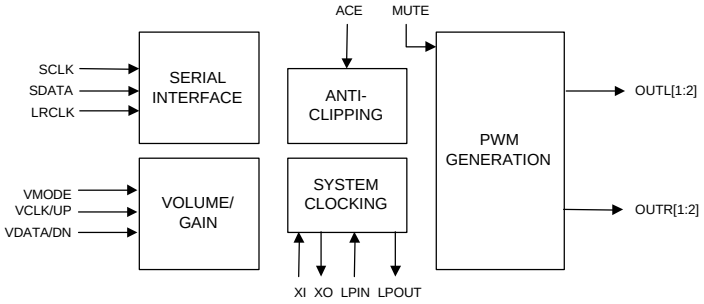


Figure 1 - DDX-2000 Functional Diagram

Audio Serial Interface

The DDX-2000 audio serial input was designed to interface with standard digital audio components such as S/PDIF receivers, surround sound decoders and digital signal processors. Serial data input is controlled by three input pins: serial clock (SCLK), serial data (SDATA), and left/right clock (LRCLK) in either I^2S or left justified formats as controlled by the serial mode pin (SMODE). The serial data formats and timing diagram are shown in Figure 3. The DDX-2000 utilizes serial data words of 16 bits and accepts data words up to 24 bits.

Volume Interface

The volume level of the DDX2000 PWM outputs can be adjusted by setting the left and right volume registers (VOLL and VOLR). These registers are seven bits with a step size of approximately -0.75 dB providing an adjustment range of –82.5 dB to +12.0 dB. Table 1 shows the volume level as a function of the register values. Following power-on-reset both volume registers are set to 0x26 or -15.75 dB.

The volume registers, VOLL and VOLR, can be set with a serial data load using a micro-controller or similar device (serial mode) or by incrementing the volume register using control pins (toggle mode). This functionality is controlled using the volume mode select pin (VMODE) and two multifunction pins; volume clock/volume up (VCLK/UP) and the volume data/volume down (VDATA/DN).

Table 1 – Volume Control

Volume Register (VOLL, VOLR) hexadecimal	Volume (dB)
0x00, 0x80	+12.0
0x01, 0x81	+11.25
0x02, 0x82	+10.5
. . .	. . .
0x10, 0x90	0.0
0x11, 0x91	-0.75
0x12, 0x92	-1.5
. . .	. . .
0x7e, 0xfe	-82.5
0x7f, 0xff	Mute

When the VMODE is logic-high (internally pulled-up) the device operates in toggle mode. The volume registers (both VOLL and VOLR) can be incremented either up or down by bringing the inputs VCLK/UP or VDATA/DN low. The volume register will increment at approximately 5 steps per second, for the first 1.4 seconds and then increase to approximately 10 steps per second until the upper or lower volume limits are reached or the input is released.

A serial mode volume change is initiated by bringing VMODE pin low. Serial data is input on

VDATA/DN and is latched on the rising edge of the VCLK/UP input as shown in Figure 4. After all eight bits are received VMODE must be brought high to latch the volume register. Note, each channel volume register must be written independently, (see Table 1).

For applications that provide digital volume control prior to the DDX-2000, the attenuation register can be set to 0 dB by pulling both the VCLK/UP and VDATA/DN to ground, leaving VMODE high.

The DDX-2000 includes an anti-clipping function to improve audio quality when using the internal volume control set to greater than 0 dB. This function dynamically adjusts the volume level to significantly reduce distortion associated with signal clipping. This function is enabled by setting the anti-clipping enable (ACE) pin high. When enabled, the maximum distortion will be limited regardless of the volume. For applications where maximum power is desired, the ACE may be disabled and the output power and distortion will increase for volume settings which exceed 0 dB.

System Clocking

The DDX-2000 operates from a master clock source whose frequency is 256 times the input LRCLK sample rate (256*fs). The device can accommodate sample rates from below 32 kHz to above 48 kHz. Either external clock sources or the built in oscillator may be used.

In designs that recover the clock (e.g., S/PDIF), the 256*fs output can be utilized for the master system clock to provide synchronous operation. For systems that operate asynchronously, i.e., the crystal clock is not exactly matched to the incoming serial data stream, the DDX-2000 will automatically accommodate sample frequency mismatch up to 0.2 %.

The accuracy of the master input clock will determine amplifier system performance. To meet the specified performance, random clock jitter must be less than 400pS p-p.

DDX Output Control

Asserting the MUTE input (logic-high), the DDX-2000 will command the zero state (load damping) which short-circuits the load to ground. The device also includes an automatic mute function which is activated upon receipt of 2048 consecutive zero data words on both the left and right serial inputs. Automatic transition from mute will occur on the first non-zero input word.

DDX-2060 POWER DEVICE

The DDX-2060 Power Device is a dual channel H-Bridge that can deliver over 35 watts per channel of audio output power. The DDX-2060 includes; a logic interface, integrated bridge drivers, high efficiency MOSFET outputs and protection circuitry. Two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a bridge configuration, according to Apogee's patented damped ternary PWM. The DDX-2060 includes over-current, thermal, and over-voltage protection and under-voltage lockout with automatic recovery. A thermal warning status is also provided.

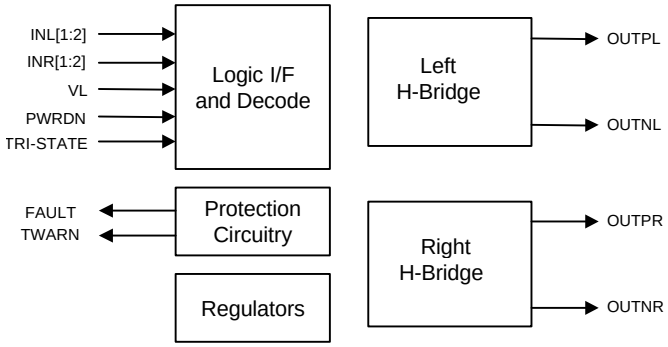


Figure 2 - DDX-2060 Block Diagram

Logic Interface and Decode

The DDX-2060 power outputs are controlled using two logic level timing signals. In order to provide a proper logic interface, the VL input must operate from the DDX-2000 logic supply.

Protection Circuitry

The DDX-2060 includes protection circuitry for over-current, over-voltage, and thermal overload conditions. A thermal warning pin TWARN is activated low (open-drain MOSFET) when the IC temperature exceeds 130°C, in advance of the thermal shutdown protection. When a fault condition is detected (logical OR of over-current, over-voltage, and thermal), an internal fault

signal acts to immediately disable the output power MOSFETs, placing both H-bridges in a high impedance state. At the same time an open-drain MOSFET connected to the FAULT pin is switched on. There are two possible modes subsequent to activating a fault. The first is a SHUT-DOWN mode. With FAULT (pull-up resistor) and TRI-STATE pins independent, an activated fault will disable the device, signaling low at the FAULT output. The device may subsequently be reset to normal operation by toggling the TRI-STATE pin from High-Low-High using an external logic signal. The second is an AUTOMATIC recovery mode. This is depicted in the application circuit, Figure 5B. The FAULT and TRI-STATE pins are shorted together and connected to a time constant circuit comprising R6 and C17. An activated FAULT will force a reset on the TRI-STATE pin causing normal operation to resume following a delay determined by the time constant of the circuit. If the fault condition is still presented, the circuit operation will continue repeating until such time as the fault condition is removed. An increase in the time constant of the circuit will produce a lower recovery frequency tending toward safer operation. Note, the automatic recovery mode may produce audible artifacts in a loudspeaker when a fault is activated. Care must be taken in the overall system design so as not to exceed the protection thresholds under normal operation.

Power Outputs

The DDX-2060 power and output pins are duplicated to provide a low impedance path for the devices bridged outputs. All duplicate power, ground and output pins must be connected for proper operation. The PWRDN or TRI-STATE pins should be used to set all MOSFETS to the Hi-Z state during power-up until the logic power supply, VL, is well established.

Parallel Output/High Current Operation

The DDX-2060 outputs can be connected in parallel for mono operation to increase the output current to a load. In this configuration the device can provide over 70W into 4 Ω. This mode is enabled with the CONFIG pin connected to VREG1 and the inputs combined INLA=INLB, INRA=INRB and outputs combined OUTLA=OUTLB, OUTRA=OUTRB.

ADDITIONAL INFORMATION

Output Filter

A passive two-pole low pass filter is used on the DDX-2060 power outputs to reconstruct the audio signal. System performance can be significantly affected by the output filter design and choice of components. Good audio performance can be obtained with low cost, solenoid type inductors having a DCR <.05 Ω and a 2A minimum rating. Output filter capacitors should be the following types: Common-mode capacitors should be 50V ceramic, X7R dialetric or 50V film types. Differential capacitors should be 50V or greater film types. A filter design for 8 Ω loads is shown in the Typical Application Circuit Fig. 5B for reference.

Power Dissipation/Heat Sink Requirements

The DDX-2060 is a high efficiency dual channel design intended for audio applications up to 35 Watts per channel. The power dissipation of the device will depend primarily on the supply voltage, load impedance, and output modulation level.

The DDX-2060 surface mount package includes an exposed thermal pad on the bottom of the device to provide a direct thermal path from the integrated circuit to the PCB. This pad must be soldered to a low thermal impedance path at circuit ground potential for proper operation, e.g. a PCB ground plane. For continuous duty rated applications, careful consideration must be made to the overall thermal design.

Performance Measurements

Class D amplifiers produce measurable switching distortion outside the audio bandwidth. Apogee's DDX amplifier uses patented PWM modulation that significantly reduces the size of these products compared to typical Class D designs. However, in order to obtain accurate performance measurements in the audio bandwidth (i.e., 20Hz to 20kHz) additional filtering is required. The Typical Performance data was taken using a brick wall filter with a break frequency of 20kHz. This type of filter is often provided with audio measurement systems.

INTERFACE TIMING

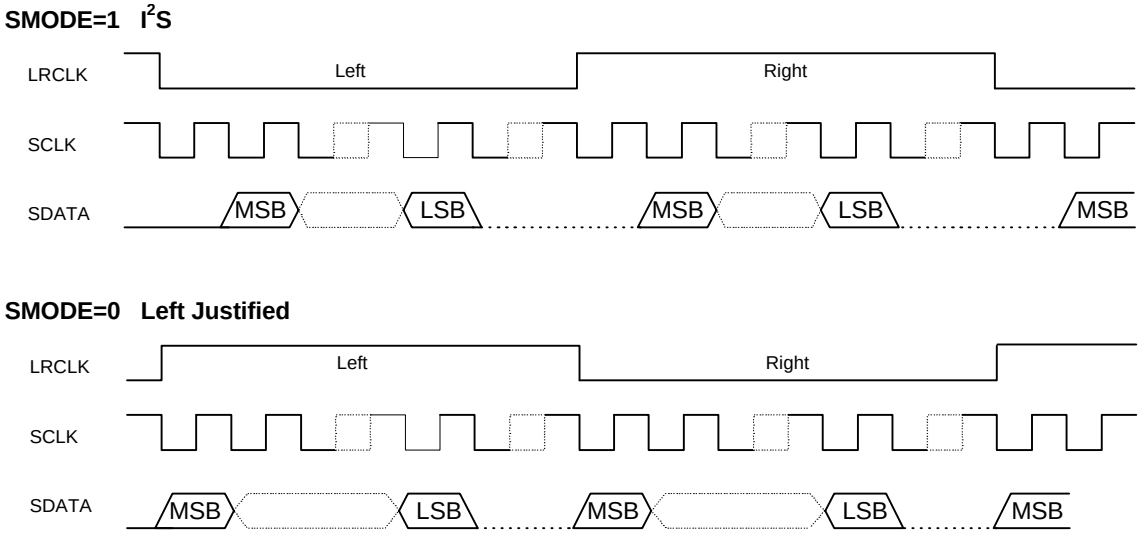
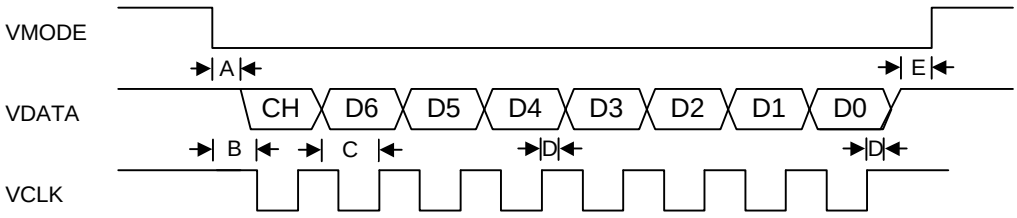


Figure 3 - Audio Serial Interface



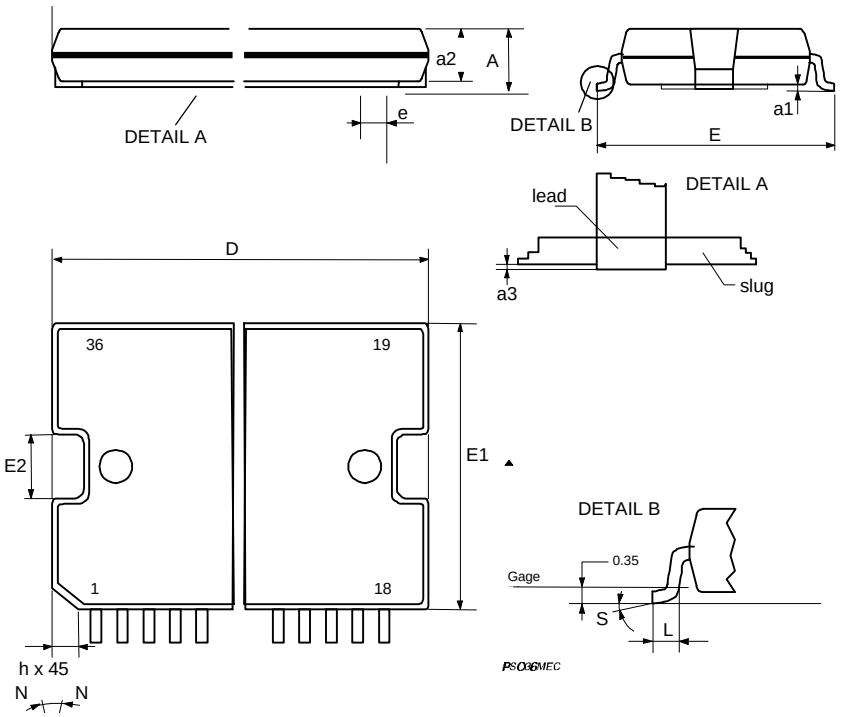
Notes:

A) VDATA hold time from VMODE > 75 ns
B) VCLK hold time from VMODE > 75 ns
C) VDATA setup to VCLK > 50 ns
D) VDATA hold from VCLK > 25 ns
E) VDATA setup to VMODE > 75 ns
F) VCLK HIGH TIME, CLK LOWTIME > 100 ns
G) CH = Channel select. Left=0, Right=1.
H) Volume register (MSB=D6, LSB=D0).

Figure 4 - Serial Volume Load Timing

PHYSICAL DIMENSIONS

Dimensions shown in mm



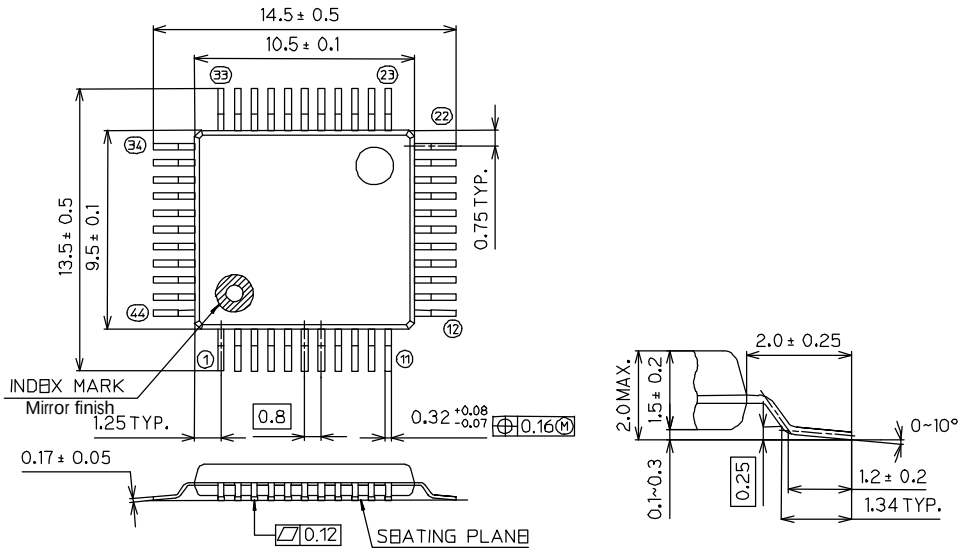
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.141
a1	0.10		0.30	0.004		0.012
a2			3.30			0.130
a3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D (1)	15.80		16.00	0.622		0.630
D1	9.40		9.80	0.370		0.385
E	13.90		14.50	0.547		0.570
e		0.65			0.0256	
e3		11.05			0.435	
E1 (1)	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
E4	2.90		3.20	0.114		0.126
G	0		0.10	0		0.004
H	15.50		15.90	0.610		0.626
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	1		0°(max.)			
S	8		°(max.)			

(1): "D" and "E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
- Critical dimensions are "a3", "E" and "G".

DDX-2060 - 36 Pin Power Package

PHYSICAL DIMENSIONS

Dimensions shown in mm



DDX-2000 - 44 Pin Quad Plastic Flat Package

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