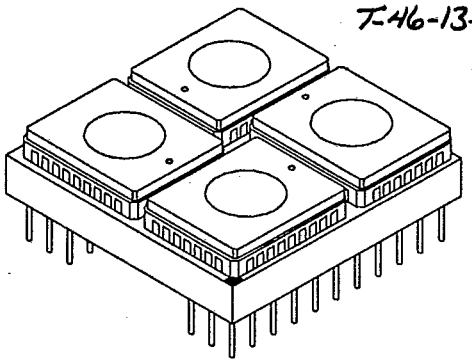
Dense-Pac Microsystems, Inc.

DPV12832V

128K X 32 UVEPROM VERSAPAC

T-46-13-29



DESCRIPTION:

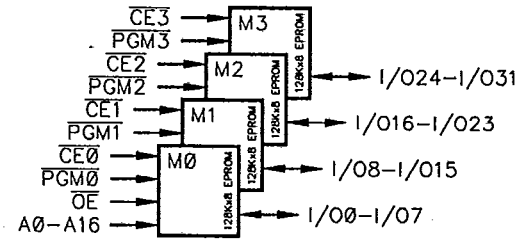
The DPV12832V is a 66-pin Pin Grid Array (PGA) consisting of four 128K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matching thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

The pins have been arranged around a central 0.6" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing four 0.1µf decoupling capacitors (important for proper operation).

FEATURES:

- Organizations Available:
  512K X 8, 265K X 16 or 128K X 32
- Access Times: -200, -250ns
- Fully Static Operation - No clock or refresh required
- Single Byte and Page Mode Programming
- Programming Voltage 12.5 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm (0.2ms Pulses Typ.)
- Common Data Inputs and Outputs
- Power Consumption:
  440µW (Standby)
  660mW (Active)
- TTL-compatible Inputs and Outputs
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions (EEPROM, SRAM and MIXED)
- Module Weight is 15 grams

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{CE0}$ - $\overline{CE3}$	Chip Enables
$\overline{PGM0}$ - $\overline{PGM3}$	Program Enables
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
V_{PP}	Programming Voltage
N.C.	No Connect

PIN-OUT DIAGRAM

1	I/O8	12	$\overline{PGM1}$	23	I/O15				34	I/024	45	VDD	56	I/031
2	I/09	13	$\overline{CE1}$	24	I/014				35	I/025	46	$\overline{CE3}$	57	I/030
3	I/010	14	VSS	25	I/013				36	I/026	47	$\overline{PGM3}$	58	I/029
4	A13	15	I/011	26	I/012				37	A6	48	I/027	59	I/028
5	A14	16	A10	27	$\overline{OE}$				38	A7	49	A3	60	A0
6	A15	17	A11	28	N.C.		(TOP VIEW)		39	VPP	50	A4	61	A1
7	A16	18	A12	29	$\overline{PGM0}$				40	A8	51	A5	62	A2
8	N.C.	19	VDD	30	I/07				41	A9	52	$\overline{PGM2}$	63	I/023
9	I/00	20	$\overline{CE0}$	31	I/06				42	I/016	53	$\overline{CE2}$	64	I/022
10	I/01	21	N.C.	32	I/05				43	I/017	54	VSS	65	I/021
11	I/02	22	I/03	33	I/04				44	I/018	55	I/019	66	I/020

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ABSOLUTE MAXIMUM RATINGS[1]			
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [2]	-0.6 to +7.0	V
$V_{I/O}$	Input/Output Voltage [2]	-0.6 to +7.0	V
V_{PP}	Programming Voltage [2]	-0.6 to +13.0	V

RECOMMENDED OPERATING RANGE[2]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage[4]	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+1.0	V
V_{IL}	Input LOW Voltage	-0.3		0.8	V
V_{PP}	V_{PP} Supply Voltage[5]	12.25	12.5	12.75	V

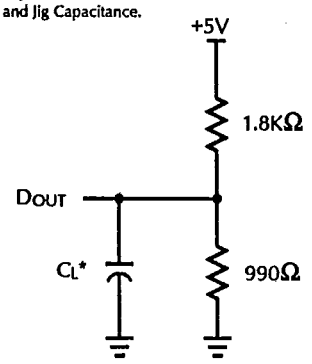
CAPACITANCE [3]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	15	pF	V_{IN} = 0V
C_{ADR}	Address Input	50		
C_{OE}	Output Enable	50		
$C_{I/O}$	Data Input/Output	25		
C_{PGM}	Program	15		

AC TEST CONDITIONS: Including Programming	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Time	≤ 20ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

Output Load		
Float	C_L	Parameters Measured
1	100 pF	except t_{DF} and t_{DFP}
2	5 pF	t_{DF} and t_{DFP}

Figure 1. Output Load

* Including Scope and Jig Capacitance.



DC OPERATING CHARACTERISTICS[6]: Over operating ranges									
Symbol	Characteristics	Test Conditions	X8		X16		X32		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = V_{DD}	-8	8	-8	8	-8	8	µA
I_{OUT}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{IN} = V_{DD} or V_{SS}	-8	8	-4	4	-2	2	µA
I_{CC1}	V_{DD} Active Current, Read	V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA		25		50		100	mA
I_{CC2}	V_{DD} Operating Current, Read	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA Cycle = min. Duty = 100%		30		60		120	mA
I_{SB1}	V_{DD} Standby Current I_{OUT} = 0mA	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}		5		5		5	mA
I_{SB2}	V_{DD} Standby Current	$\overline{CE}$ = V_{DD} ± 0.3V V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		80		80		80	µA
I_{PP1}	V_{PP} Supply Current Byte Write	$\overline{CE}$, $\overline{PGM}$ = V_{IL}, $\overline{OE}$ = V_{IH}		40		80		160	mA
I_{PP2}	V_{PP} Supply Current Page Write	$\overline{CE}$, $\overline{OE}$ = V_{IH}, $\overline{PGM}$ = V_{IL}, V_{PP} = V_{DD}		50		100		200	mA
I_{PP3}	V_{PP} Supply Current Read	$\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}, I_{OUT} > 0mA		80		80		80	µA
V_{OL}	Output LOW Voltage	I_{OUT} = 2.1mA		0.45		0.45		0.45	V
V_{OH1}	Output HIGH Voltage	I_{OUT} = -400µA	2.4		2.4		2.4		V
V_{IL}	Input LOW Level		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
V_{IH}	Input HIGH Level		2.2	V_{DD}+1	2.2	V_{DD}+1	2.2	V_{DD}+1	V

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FUNCTIONS AND PIN CONNECTIONS

Mode	Function	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	I/O0 - I/O31	Power
Read Operations	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	X	X	H			High Impedance	
	Standby	X	H	X			High Impedance	
Program Operations	Program	L	L	H	12.5V	6V	Data In	Standby
	Program Inhibit	H	H	X			High Impedance	
	Page Programming	L	H	H			High Impedance	
(T_A = +25 ± 5°C)	Program Verify	H	L	L			Data Out	

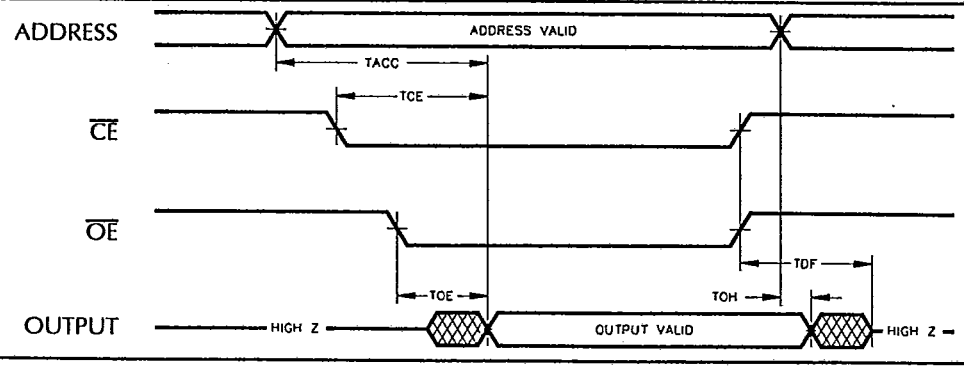
AC OPERATING CONDITIONS AND CHARACTERISTICS: Over operating ranges

No.	Symbol	Parameter	-200 Min.	-200 Max.	-250 Min.	-250 Max.	Unit
1	t_{ACC}	Address Access Time		200		250	ns
2	t_{CE}	Chip Enable to Output Valid [7]		200		250	ns
3	t_{OE}	Output Enable to Output Valid [7, 8]		70		100	ns
4	t_{DF}	$\overline{OE}$ or $\overline{CE}$ HIGH to Output Float [3, 9]	0	50	0	60	ns
5	t_{OH}	Output Hold from Address	0		0		ns

AC PROGRAMMING CONDITIONS AND CHARACTERISTICS[11]: Over operating ranges

No.	Symbol	Parameter	Min.	Max.	Unit
6	t_{AS}	Address Set-up Time	2		µs
7	t_{CES}	Chip Enable Set-up Time	2		µs
8	t_{OES}	Output Enable Set-up Time	2		µs
9	t_{DS}	Data Set-up Time	2		µs
10	t_{VCS}	V_{DD} Set-up Time [10]	2		µs
11	t_{VPS}	V_{PP} Set-up Time [10]	2		µs
12	t_{AH}	Address Hold Time	0		µs
13	t_{OEH}	Output Enable Hold Time	2		µs
14	t_{DH}	Data Hold Time	2		µs
15	t_{CEP}	Chip Enable to Data Valid		150	ns
16	t_{DFP}	Output Enable HIGH Output Float Delay [3]	0	130	ns
17	t_{PW}	Programming Pulse Width [10]	0.19	0.21	ms
18	t_{OPW}	Over Programming Pulse Width [11]	0.19	5.25	ms
19	t_{AHL}	Address Latch Hold Time	2		µs
20	t_{LW}	Output Enable Pulse Width During Data Latch	1		µs
21	t_{PGMS}	Page Programming Setup Time	2		µs
22	t_{CEH}	Chip Enable Hold Time	2		µs

READ TIMING



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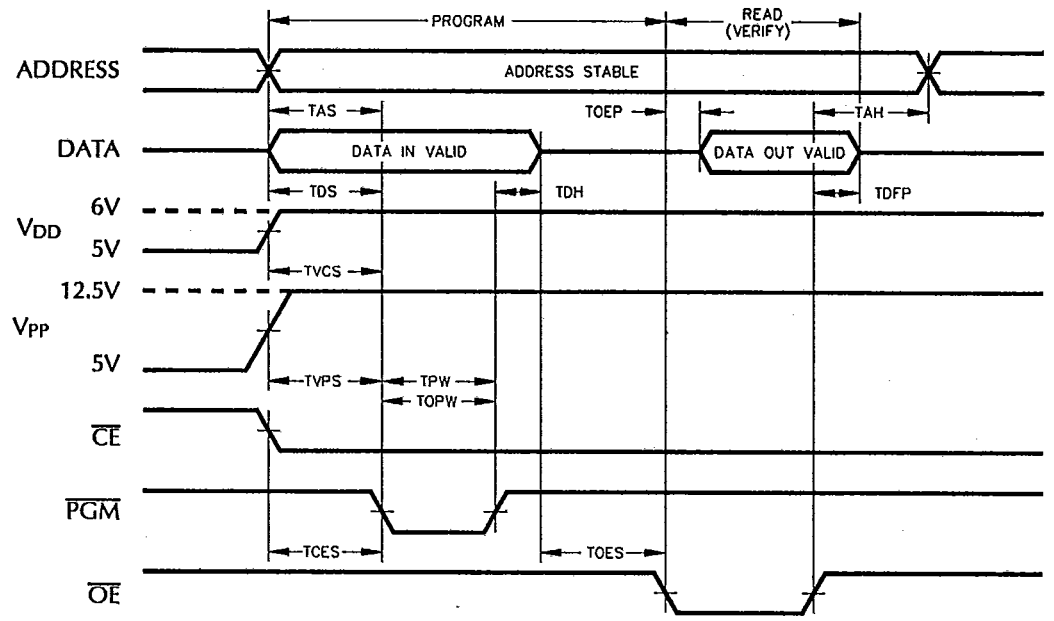
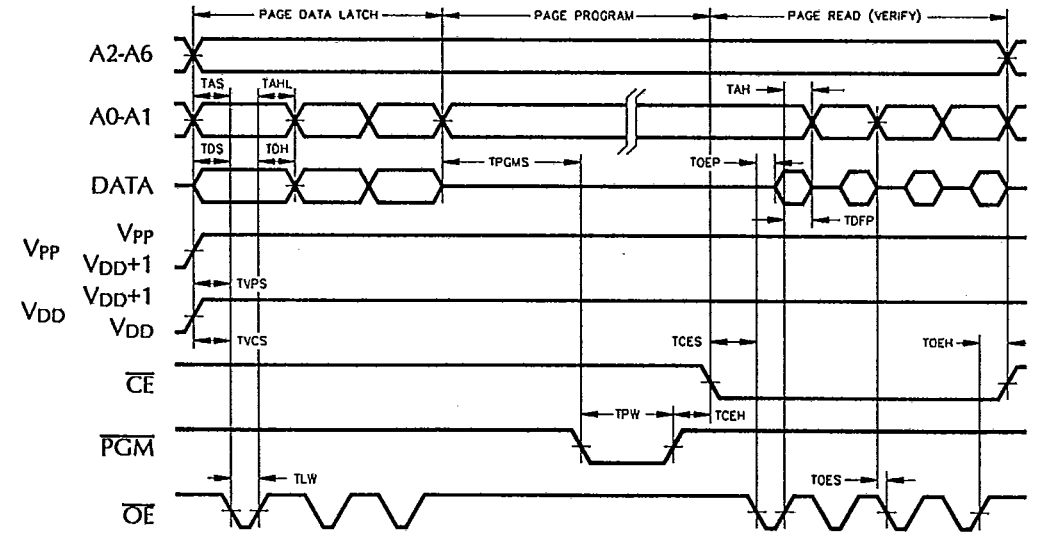
BYTE PROGRAMMING TIMING [4]



PROGRAMMING TIMING [4]



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PROGRAMMING AND ERASING INFORMATION

Programming

Upon delivery from Dense-Pac, or after erasure *(See Erasure section)*, the DPV12832V contains "1's" in every location, and read data is in the high state. "0's" are written into the DPV12832V through the procedure of programming. A 0.1µF capacitor between V_{PP} and V_{SS} is required to prevent excessive voltage transients during programming which could damage the device. Programming modes require +6.0V and +12.5V to be applied to V_{DD} and V_{PP} respectively.

Individual bytes or address locations can be selected and programmed by using the byte mode programming algorithm shown in Figure 2. In byte programming mode, $\overline{CE}$ is set at V_{IL} and $\overline{OE}$ is set at V_{IH}. After the applied address and input data signals are stable, programming is accomplished by a 0.2ms V_{IL} pulse on the $\overline{PGM}$ pin *(refer to the Byte Mode Programming Timing Diagram)*.

The DPV12832V's fast page mode programming algorithm *(shown in Figure 3)* provides a great reduction in programming time by writing four bytes simultaneously. Each of these four bytes may contain different data. In page programming mode, $\overline{CE}$ and $\overline{PGM}$ are at V_{IH} while input data is strobed into internal holding registers by V_{IL} pulses on the $\overline{OE}$ pin. The EPROM is then programmed by a 0.2ms V_{IL} pulse on the $\overline{PGM}$ pin while $\overline{CE}$ and $\overline{OE}$ are held at V_{IH} *(refer to the Page Programming Timing Diagram)*.

System design consideration must be taken to avoid inadvertent page mode programming which can occur when $\overline{CE}$ and $\overline{OE}$ are at V_{IH} and $\overline{PGM}$ is at V_{IL}. A programming adapter for programming on standard EPROM programmers is available, contact Dense-Pac sales for more information.

Erasure

To clear all locations of their programmed contents it is necessary to expose the DPV12832V to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase a DPV12832V. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å) with an intensity of 12,000µW/cm^2] for 21 minutes.

The DPV12832V and similar devices can be erased by light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light or sunlight will eventually erase the DPV12832V. After programming, the package windows should be covered by an opaque label or substance, to prevent inadvertent erasure.

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NOTES:

1. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. All voltages are with respect to V_{SS}.
3. This parameter is guaranteed and not 100% tested.
4. V_{DD} must be applied either coincident with or before V_{PP} and removed either coincident with or after V_{PP}.
5. V_{PP} must not be greater than 13.0V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with V_{PP} = 13.0V. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from 5.0V to 13.0V or vice-versa.
6. t_A = -55°C to +125°C, V_{DD} = 5.0V ± 0.5V, and V_{PP} = V_{DD} reading. t_A = +25°C ± 5°C, V_{DD} = 6.0V ± 0.25V, V_{PP} = 12.5V ± 0.3V programming.
7. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the following edge of $\overline{CE}$ without impact on t_{CE}.
8. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the following Address is valid without impact on t_{ACC}.
9. T_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
10. Initial Program Pulse Width Tolerance is 0.2ms ± 5%.
11. The length of the overprogram pulse may vary from 0.19ms to 5.25ms as a function of the iteration counter value X.

Figure 2. Programming Flow Chart

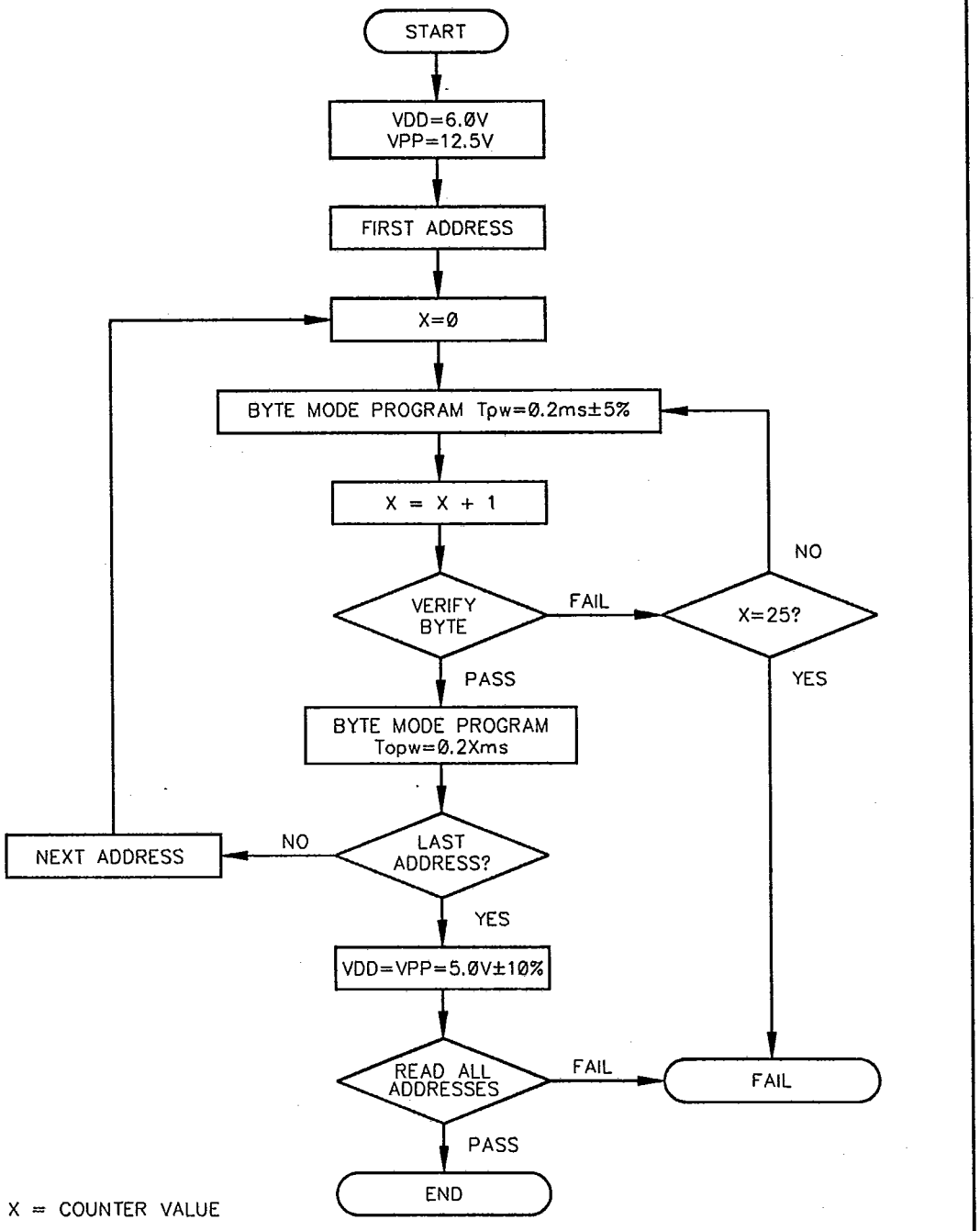
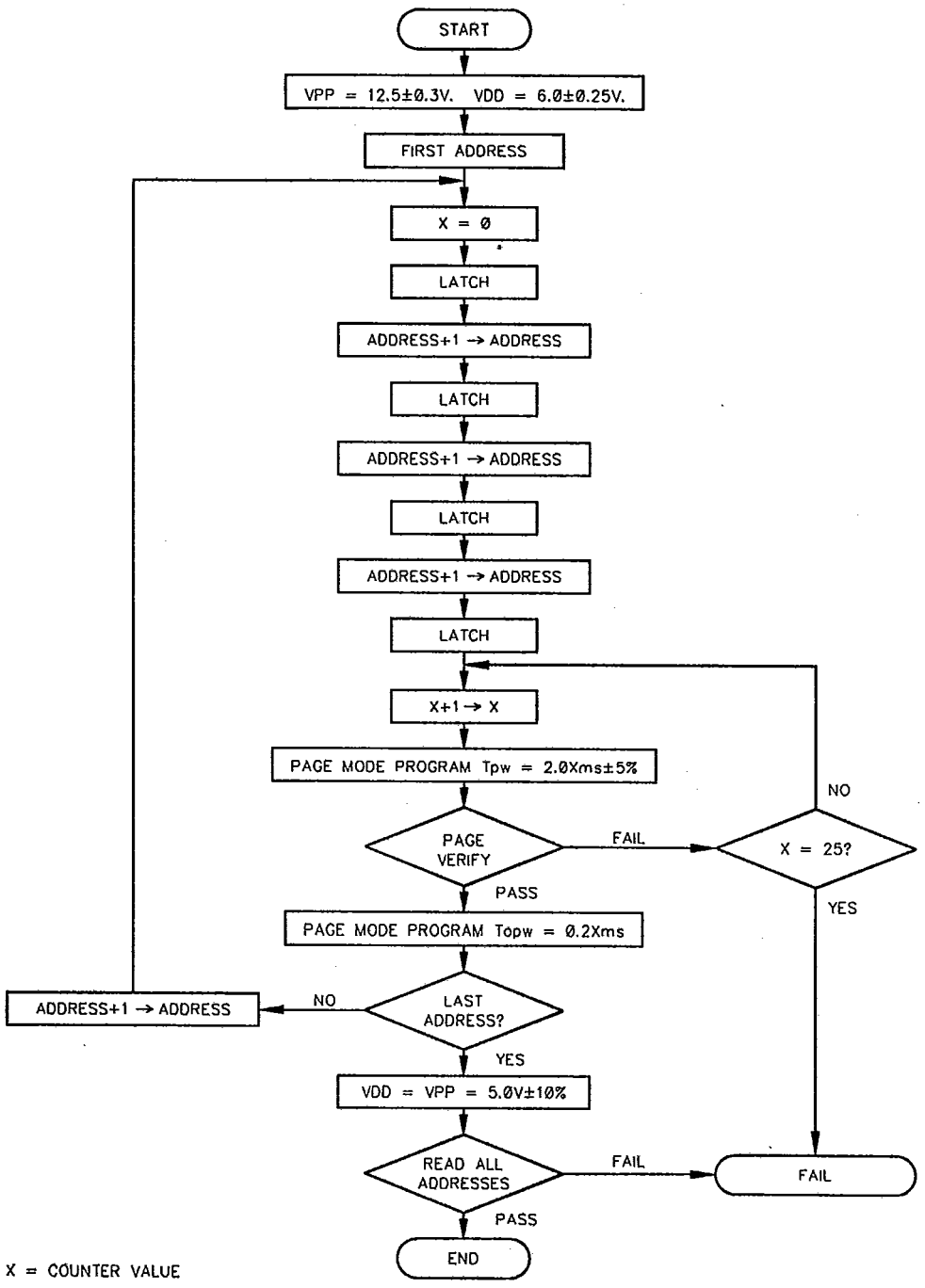


Figure 3. High Performance Page Programming Flow Chart



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DPV12832V

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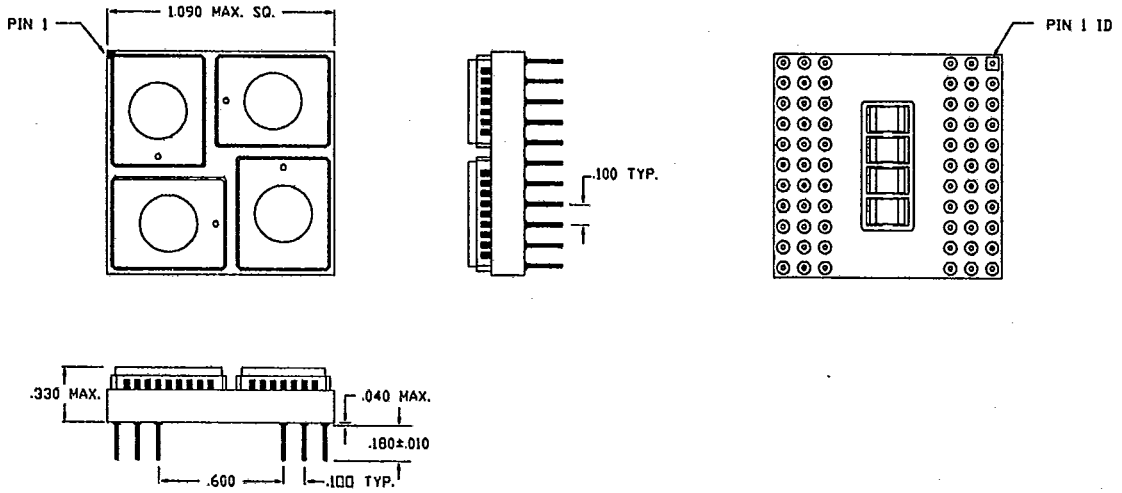
ORDERING INFORMATION

DP V12832 V – XXX X
PREFIX DEVICE TYPE PACKAGE SPEED GRADE

C	COMMERCIAL	0° to +70°C
I	INDUSTRIAL	−40° to +85°C
M	MILITARY	−55° to +125°C
B *	MIL−PROCESSED	−55° to +125°C
200	200ns	
250	250ns	
V	66−PIN PGA VERSAPAC	
UVEPROM 512KX8, 256KX16 OR 128KX32		

* B grade modules are not built with 883 devices.

MECHANICAL DIAGRAMS



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