19-2736; Rev 0; 1/03

MAXIM

14-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

General Description

The MAX1156/MAX1158/MAX1174 14-bit, low-power, successive-approximation analog-to-digital converters (ADCs) feature automatic power-down, a factory-trimmed internal clock, and a byte-wide parallel interface. The devices operate from a single +4.75V to +5.25V analog supply and feature a separate digital supply input for direct interface with +2.7V to +5.25V digital logic.

The MAX1156 accepts a 0 to +10V analog input voltage range. The MAX1158 accepts a ±10V bipolar analog input voltage range, while the MAX1174 accepts a ±5V bipolar analog input voltage range. All devices consume no more than 26.5mW at a sampling rate of 135ksps when using an external reference, and 31mW when using the internal +4.096V reference. AutoShutdown™ reduces supply current to 0.4mA (typ) at 10ksps.

The MAX1156/MAX1158/MAX1174 are ideal for high-performance, battery-powered, data-acquisition applications. Excellent AC performance (THD = -100dB) and DC accuracy (±1LSB INL) make the MAX1156/MAX1158/MAX1174 ideal for industrial process control, instrumentation, and medical applications.

The MAX1156/MAX1158/MAX1174 are available in a 20-pin TSSOP package and are fully specified over the -40°C to +85°C extended temperature range and the 0°C to +70°C commercial temperature range.

Applications

Temperature Sensing and Monitoring

Industrial Process Control

I/O Modules

Data-Acquisition Systems

Precision Instrumentation

Pin Configuration appears at end of data sheet.

AutoShutdown is a trademark of Maxim Integrated Products, Inc.

Features

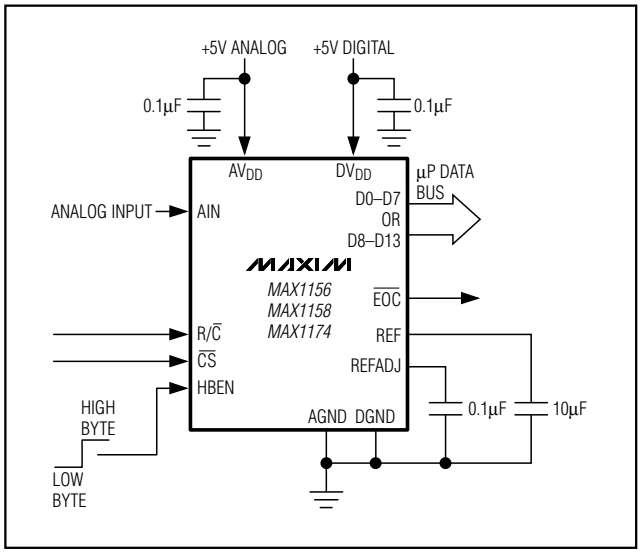
- **Byte-Wide Parallel Interface**
- **Analog Input Voltage Range: ±10V, ±5V, 0 to 10V**
- **Single +4.75V to +5.25V Analog Supply Voltage**
- **Interface with +2.7V to +5.25V Digital Logic**
- **±1LSB INL (max)**
- **±1LSB DNL (max)**
- **Low Supply Current (max)**
  - **2.9mA (External Reference)**
  - **3.8mA (Internal Reference)**
  - **5µA AutoShutdown Mode**
- **Small Footprint**
- **20-Pin TSSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INPUT VOLTAGE RANGE
MAX1156ACUP	0°C to +70°C	20 TSSOP	0 to +10V
MAX1156BCUP	0°C to +70°C	20 TSSOP	0 to +10V
MAX1156AEUP	-40°C to +85°C	20 TSSOP	0 to +10V
MAX1156BEUP	-40°C to +85°C	20 TSSOP	0 to +10V

Ordering Information continued at end of data sheet.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
AIN to AGND .....-16.5V to +16.5V
REF, REFADJ to AGND.....-0.3V to (AV_{DD} + 0.3V)
$\overline{CS}$, R/$\overline{C}$, HBEN to DGND .....-0.3V to +6V
D_, $\overline{EOC}$ to DGND .....-0.3V to (DV_{DD} + 0.3V)
Maximum Continuous Current into any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 10.9mW/°C above +70°C) 879mW
Operating Temperature Range
MAX11_ _ _CUP.....0°C to +70°C
MAX11_ _ _EUP.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = +5V ±5%, external reference = +4.096V, C_{REF} = 10µF, C_{REFADJ} = 0.1µF, V_{REFADJ} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution	RES			14			Bits
Differential Nonlinearity	DNL	No missing codes over temperature		-1		+1	LSB
Integral Nonlinearity	INL	MAX11_ _A		-1		+1	LSB
		MAX11_ _B		-2		+2	
Transition Noise		RMS noise, external reference			0.32		LSB_{RMS}
		Internal reference			0.34		
Offset Error				-10	0	+10	mV
Gain Error					0	±0.2	%FSR
Offset Drift					16		µV/°C
Gain Drift					±1		ppm/°C
AC ACCURACY (f_{IN} = 1kHz, V_{AIN} = full range, 135ksps)							
Signal-to-Noise Plus Distortion	SINAD			81	85		dB
Signal-to-Noise Ratio	SNR			82	85		dB
Total Harmonic Distortion	THD				-100	-86	dB
Spurious-Free Dynamic Range	SFDR			87	103		dB
ANALOG INPUT							
Input Range	V_{AIN}	MAX1156		0		+10	V
		MAX1158		-10		+10	
		MAX1174		-5		+5	
Input Resistance	R_{AIN}	MAX1156/MAX1174	Normal operation	5.3	6.9	9.2	kΩ
		MAX1156	Shutdown mode	5.3			
		MAX1174	Shutdown mode	3.0			
		MAX1158	Normal operation	7.8	10	13.0	
			Shutdown mode	6.0			

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +5V ±5%, external reference = +4.096V, C_{REF} = 10µF, C_{REFADJ} = 0.1µF, V_{REFADJ} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current	I_{AIN}	MAX1156, 0 ≤ V_{AIN} ≤ +10V		-0.1		+2.0	mA
		MAX1158, -10V ≤ V_{AIN} ≤ +10V	Normal operation	-1.8		+1.2	
			Shutdown mode	-1.8		+1.8	
		MAX1174, -5V ≤ V_{AIN} ≤ +5V	Normal operation	-1.8		+0.4	
			Shutdown mode	-1.8		+1.8	
Input Current Step at Power-Up	I_{PU}	MAX1158, V_{AIN} = +10V, shutdown mode to operating mode			0.5	0.7	mA
		MAX1174, V_{AIN} = +5V, shutdown mode to operating mode			1	1.4	
Input Capacitance	C_{IN}				10		pF
INTERNAL REFERENCE							
REF Output Voltage	V_{REF}			4.056	4.096	4.136	V
REF Output Tempco					±35		ppm/°C
REF Short-Circuit Current	I_{REF-SC}				±10		mA
EXTERNAL REFERENCE							
REF and REFADJ Input Voltage Range				3.8		4.2	V
REFADJ Buffer Disable Threshold				AV_{DD} - 0.4		AV_{DD} - 0.1	V
REF Input Current	I_{REF}	Normal mode, f_{SAMPLE} = 135ksps			60	100	µA
		Shutdown mode (Note 1)			±0.1	±10	
REFADJ Input Current	I_{REFADJ}	REFADJ = AV_{DD}			16		µA
DIGITAL INPUTS/OUTPUTS							
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA, DV_{DD} = +2.7V to +5.25V, AV_{DD} = +5.25V		DV_{DD} - 0.4			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA, DV_{DD} = +2.7V to +5.25V, AV_{DD} = +5.25V				0.4	V
Input High Voltage	V_{IH}			0.7 × DV_{DD}			V
Input Low Voltage	V_{IL}					0.3 × DV_{DD}	V
Input Leakage Current		Digital input = DV_{DD} or 0V		-1		+1	µA
Input Hysteresis	V_{HYST}				0.2		V
Input Capacitance	C_{IN}				15		pF
Three-State Output Leakage	I_{OZ}					±10	µA
Three-State Output Capacitance	C_{OZ}				15		pF

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ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +5V ±5%, external reference = +4.096V, C_{REF} = 10µF, C_{REFADJ} = 0.1µF, V_{REFADJ} = AV_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Analog Supply Voltage	AV_{DD}			4.75		5.25	V
Digital Supply Voltage	DV_{DD}			2.70		5.25	V
Analog Supply Current	I_{AVDD}	External reference, 135ksps	MAX1156			2.9	mA
			MAX1158/MAX1174		4	5.3	
		Internal reference, 135ksps	MAX1156			3.8	
			MAX1158/MAX1174		5.2	6.2	
Shutdown Supply Current	I_{SHDN}	Shutdown mode (Note 1), digital input = DV_{DD} or 0V			0.5	5	µA
		Standby mode			3.7		mA
Digital Supply Current	I_{DVDD}					0.75	mA
Power-Supply Rejection		AV_{DD} = DV_{DD} = +4.75V to +5.25V			1		LSB

TIMING CHARACTERISTICS (Figures 1 and 2)

(AV_{DD} = +4.75V to +5.25V ±5%, DV_{DD} = +2.7V to AV_{DD}, external reference = +4.096V, C_{REF} = 10µF, C_{REFADJ} = 0.1µF, V_{REFADJ} = AV_{DD}, C_{LOAD} = 20pF, T_A = T_{MIN} to T_{MAX}.)

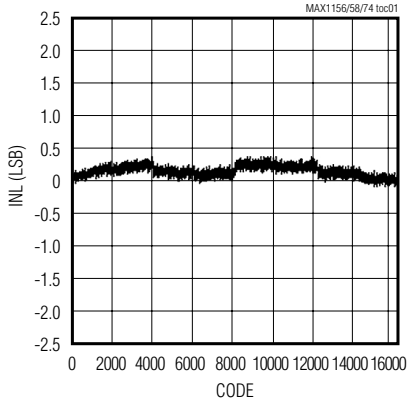
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Sampling Rate	$f_{SAMPLE-MAX}$					135	ksps
Acquisition Time	t_{ACQ}			2			µs
Conversion Time	t_{CONV}					4.7	µs
$\overline{CS}$ Pulse Width High	t_{CSH}	(Note 2)		40			ns
$\overline{CS}$ Pulse Width Low	t_{CSL}	(Note 2)	DV_{DD} = +4.75V to +5.25V	40			ns
			DV_{DD} = +2.7V to +5.25V	60			
R/$\overline{C}$ to $\overline{CS}$ Fall Setup Time	t_{DS}			0			ns
R/$\overline{C}$ to $\overline{CS}$ Fall Hold Time	t_{DH}	DV_{DD} = +4.75V to +5.25V		40			ns
		DV_{DD} = +2.7V to +5.25V		60			
$\overline{CS}$ to Output Data Valid	t_{DO}	DV_{DD} = +4.75V to +5.25V				40	ns
		DV_{DD} = +2.7V to +5.25V				80	
$\overline{EOC}$ Fall to $\overline{CS}$ Fall	t_{DV}			0			ns
$\overline{CS}$ Rise to $\overline{EOC}$ Rise	t_{EOC}	DV_{DD} = +4.75V to +5.25V				40	ns
		DV_{DD} = +2.7V to +5.25V				80	
Bus Relinquish Time	t_{BR}	DV_{DD} = +4.75V to +5.25V				40	ns
		DV_{DD} = +2.7V to +5.25V				80	
HBEN Transition to Output Data Valid	$t_{DO}1$	DV_{DD} = +4.75V to +5.25V				40	ns
		DV_{DD} = +2.7V to +5.25V				80	

Note 1: Maximum specification is limited by automated test equipment.
Note 2: To ensure best performance, finish reading the data and wait t_{BR} before starting a new acquisition.

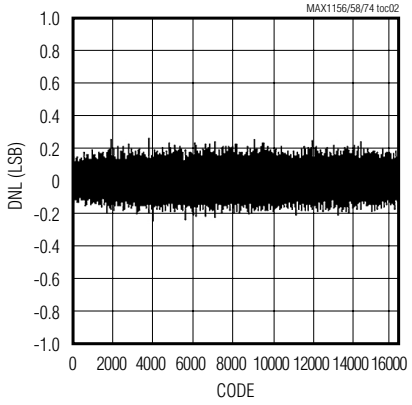
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = +5V, external reference = +4.096V, C_{REF} = 10µF, C_{REFADJ} = 0.1µF, V_{REFADJ} = AV_{DD}, C_{LOAD} = 20pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (*Typical Application Circuit*)

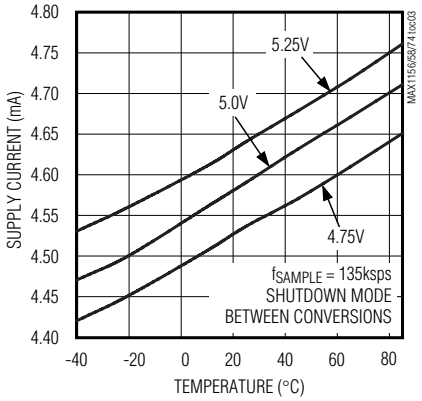
INL vs. CODE



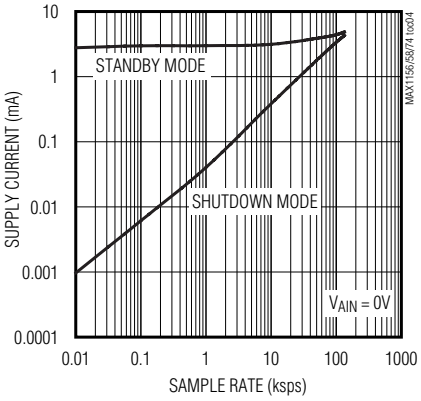
DNL vs. CODE



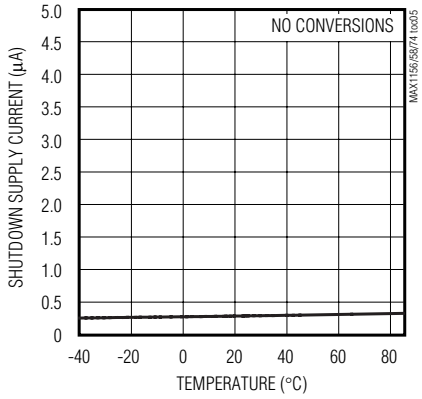
SUPPLY CURRENT (AV_{DD} + DV_{DD}) vs. TEMPERATURE



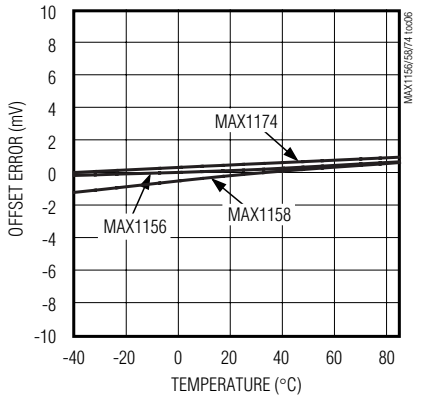
SUPPLY CURRENT (AV_{DD} + DV_{DD}) vs. SAMPLE RATE



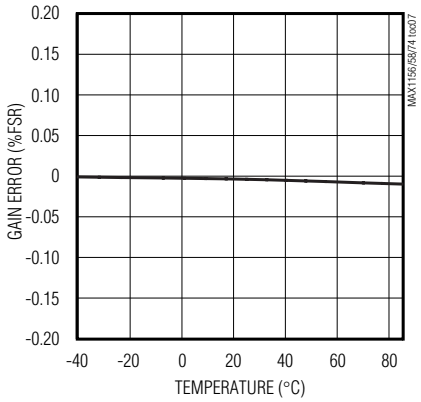
SHUTDOWN CURRENT (AV_{DD} + DV_{DD}) vs. TEMPERATURE



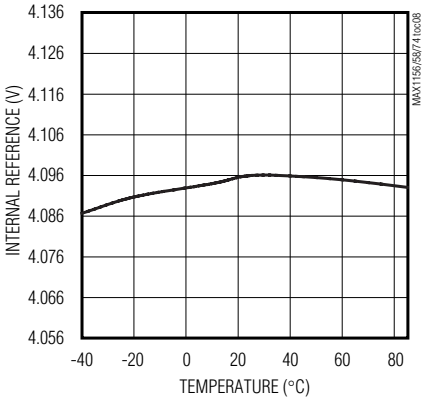
OFFSET ERROR vs. TEMPERATURE



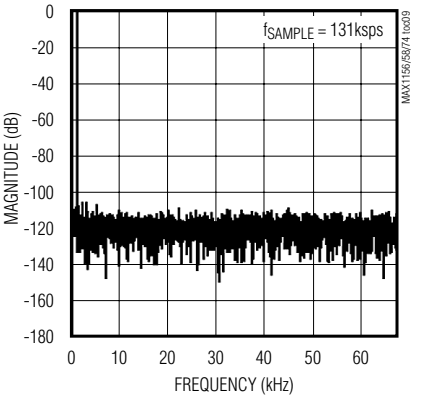
GAIN ERROR vs. TEMPERATURE



INTERNAL REFERENCE vs. TEMPERATURE



FFT AT 1kHz

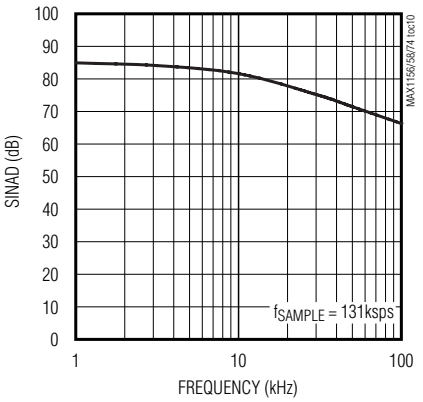


14-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

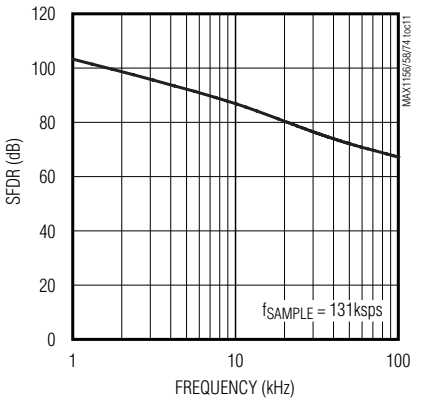
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = +5V, external reference = +4.096V, C_{REF} = 10µF, C_{REFADJ} = 0.1µF, V_{REFADJ} = AV_{DD}, C_{LOAD} = 20pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (*Typical Application Circuit*)

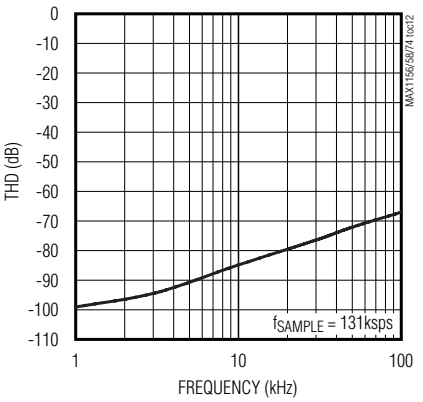
SINAD vs. FREQUENCY



SFDR vs. FREQUENCY



THD vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	D4/D12	Three-State Digital Data Output
2	D5/D13	Three-State Digital Data Output. D13 is the MSB.
3	D6/0	Three-State Digital Data Output
4	D7/0	Three-State Digital Data Output
5	R/$\overline{C}$	Read/Convert Input. Power up and put the MAX1156/MAX1158/MAX1174 in acquisition mode by holding R/$\overline{C}$ low during the first falling edge of $\overline{CS}$. During the second falling edge of $\overline{CS}$, the level on R/$\overline{C}$ determines whether the reference and reference buffer power down or remain on after conversion. Set R/$\overline{C}$ high during the second falling edge of $\overline{CS}$ to power down the reference and buffer, or set R/$\overline{C}$ low to leave the reference and buffer powered up. Set R/$\overline{C}$ high during the third falling edge of $\overline{CS}$ to put valid data on the bus.
6	$\overline{EOC}$	End of Conversion. $\overline{EOC}$ drives low when conversion is complete.
7	AV_{DD}	Analog Supply Input. Bypass with a 0.1µF capacitor to AGND.
8	AGND	Analog Ground. Primary analog ground (star ground).
9	AIN	Analog Input
10	AGND	Analog Ground. Connect pin 10 to pin 8.
11	REFADJ	Reference Buffer Output. Bypass REFADJ with a 0.1µF capacitor to AGND for internal reference mode. Connect REFADJ to AV_{DD} to select external reference mode.
12	REF	Reference Input/Output. Bypass REF with a 10µF capacitor to AGND for internal reference mode. External reference input when in external reference mode.

Pin Description (continued)

PIN	NAME	FUNCTION
13	HBEN	High-Byte Enable Input. Used to multiplex the 14-bit conversion result. 1: Most significant byte available on the data bus. 0: Least significant byte available on the data bus.
14	$\overline{CS}$	Convert Start. The first falling edge of $\overline{CS}$ powers up the device and enables acquire mode when R/$\overline{C}$ is low. The second falling edge of $\overline{CS}$ starts conversion. The third falling edge of $\overline{CS}$ loads the result onto the bus when R/$\overline{C}$ is high.
15	DGND	Digital Ground
16	DV_{DD}	Digital Supply Voltage. Bypass with a 0.1µF capacitor to DGND.
17	D0/D8	Three-State Digital Data Output. D0 is the LSB.
18	D1/D9	Three-State Digital Data Output
19	D2/D10	Three-State Digital Data Output
20	D3/D11	Three-State Digital Data Output

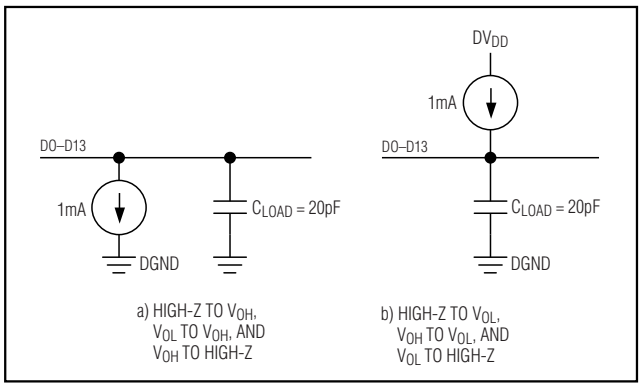


Figure 1. Load Circuits

Detailed Description

Converter Operation

The MAX1156/MAX1158/MAX1174 use a successive-approximation (SAR) conversion technique with an inherent track-and-hold (T/H) stage to convert an analog input into a 14-bit digital output. Parallel outputs provide a high-speed interface to microprocessors (µPs). The *Functional Diagram* shows a simplified internal architecture of the MAX1156/MAX1158/MAX1174. Figure 3 shows a typical application circuit for the MAX1156/MAX1158/MAX1174.

Analog Input

Input Scaler

The MAX1156/MAX1158/MAX1174 have an input scaler, which allows conversion of true bipolar input voltages and input voltages greater than the power supply, while operating from a single +5V analog supply. The input scaler attenuates and shifts the analog input to match the input range of the internal DAC. The MAX1156 has a unipolar input voltage range of 0 to +10V. The MAX1158 input voltage range is ±10V while the MAX1174 input voltage range is ±5V. Figure 4 shows the equivalent input circuit of the MAX1156/MAX1158/MAX1174. This circuit limits the current going into or out of AIN to less than 1.8mA.

Track and Hold (T/H)

In track mode, the internal hold capacitor acquires the analog signal (see Figure 4). In hold mode, the T/H switches open and the capacitive DAC samples the analog input. During the acquisition, the analog input (AIN) charges capacitor C_{HOLD}. The acquisition ends on the second falling edge of $\overline{CS}$. At this instant, the T/H switches open. The retained charge on C_{HOLD} represents a sample of the input. In hold mode, the capacitive DAC adjusts during the remainder of the conversion time to restore node T/H OUT to zero within the limits of 14-bit resolution. Force $\overline{CS}$ low to put valid data on the bus after conversion is complete.

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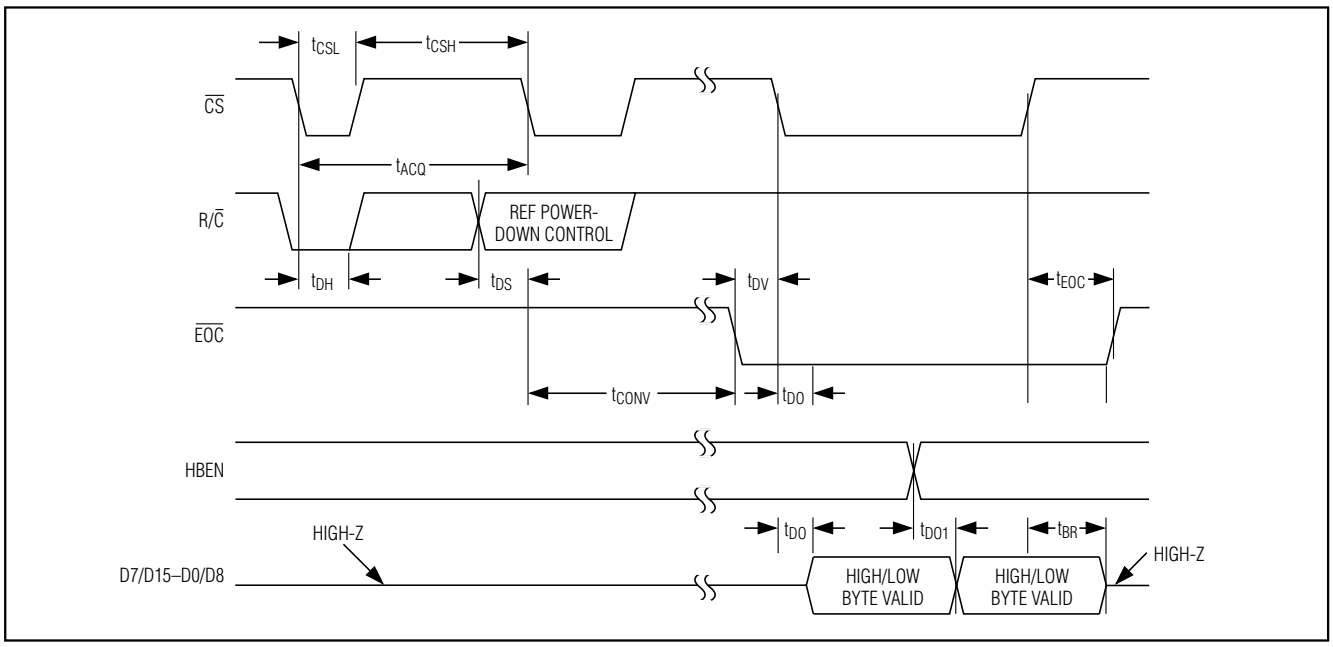

Figure 2. MAX1156/MAX1158/MAX1174 Timing Diagram

Power-Down Modes

Select standby mode or shutdown mode with the R/$\overline{C}$ bit during the second falling edge of $\overline{CS}$ (see the *Selecting Standby or Shutdown Mode* section). The MAX1156/MAX1158/MAX1174 automatically enter either standby mode (reference and buffer on) or shutdown (reference and buffer off) after each conversion, depending on the status of R/$\overline{C}$ during the second falling edge of $\overline{CS}$.

Internal Clock

The MAX1156/MAX1158/MAX1174 generate an internal conversion clock to free the microprocessor from the burden of running the SAR conversion clock. Total conversion time (t_{CONV}) after entering hold mode (second falling edge of $\overline{CS}$) to end of conversion ($\overline{EOC}$) falling is 4.7µs (max).

Applications Information

Starting a Conversion

$\overline{CS}$ and R/$\overline{C}$ control acquisition and conversion in the MAX1156/MAX1158/MAX1174 (see Figure 2). The first falling edge of $\overline{CS}$ powers up the device and puts it in acquire mode if R/$\overline{C}$ is low. The convert start is ignored if R/$\overline{C}$ is high. The MAX1156/MAX1158/MAX1174 need at least 12ms (C_{REFADJ} = 0.1µF, C_{REF} = 10µF) for the internal reference to wake up and settle before starting the conversion, if powering up from shutdown.

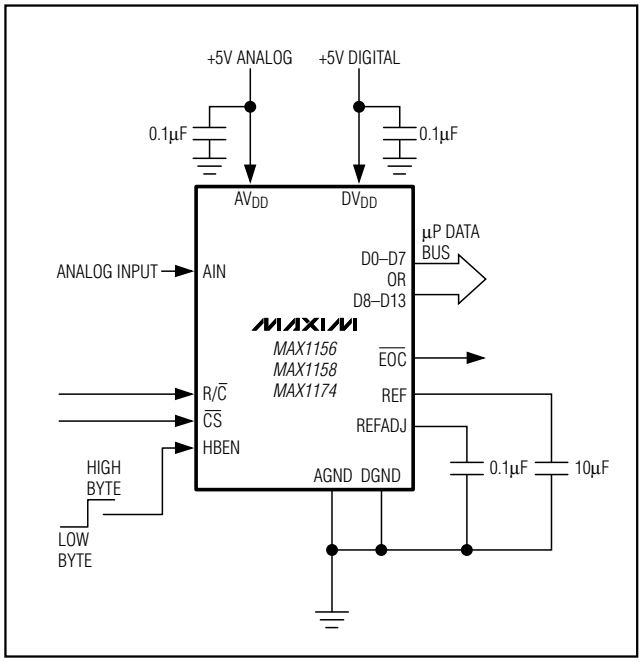

Figure 3. Typical Application Circuit for the MAX1156/MAX1158/MAX1174

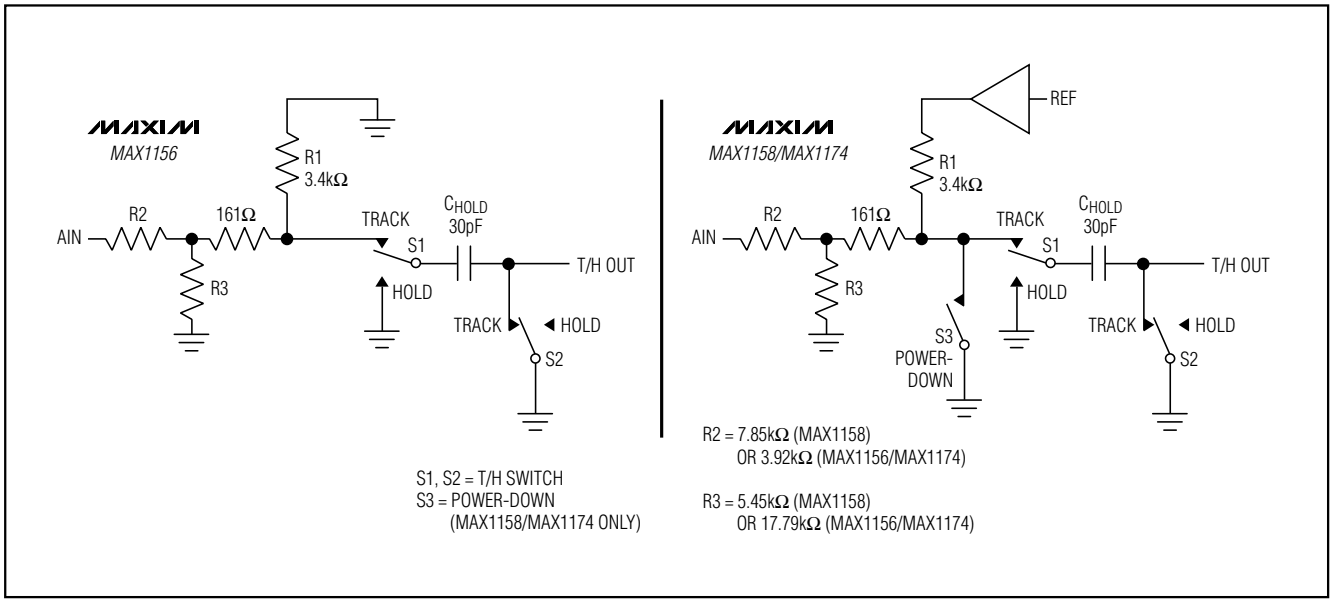

Figure 4. Equivalent Input Circuit

Selecting Standby or Shutdown Mode

The MAX1156/MAX1158/MAX1174 have a selectable standby or low-power shutdown mode. In standby mode, the ADC's internal reference and reference buffer do not power down between conversions, eliminating the need to wait for the reference to power up before performing the next conversion. Shutdown mode powers down the reference and reference buffer after completing a conversion. The reference and reference buffer require a minimum of 12ms (C_{REFADJ} = 0.1µF, C_{REF} = 10µF) to power up and settle from shutdown.

The state of R/$\overline{C}$ at the second falling edge of $\overline{CS}$ selects which power-down mode the MAX1156/MAX1158/MAX1174 enter upon conversion completion. Holding R/$\overline{C}$ low causes the MAX1156/MAX1158/MAX1174 to enter standby mode. The reference and buffer are left on after the conversion completes. R/$\overline{C}$ high causes the MAX1156/MAX1158/MAX1174 to enter shutdown mode and power down the reference and buffer after conversion (see Figures 5 and 6). Set the voltage at R/$\overline{C}$ high during the second falling edge of $\overline{CS}$ to realize the lowest current operation.

Standby Mode

While in standby mode, the supply current is less than 3.7mA (typ). The next falling edge of $\overline{CS}$ with R/$\overline{C}$ low causes the MAX1156/MAX1158/MAX1174 to exit standby mode and begin acquisition. The reference and reference buffer remain active to allow quick turn-on time.

Shutdown Mode

In shutdown mode, the reference and reference buffer are shut down between conversions. Shutdown mode reduces supply current to 0.5µA (typ) immediately after the conversion. The next falling edge of $\overline{CS}$ with R/$\overline{C}$ low causes the reference and buffer to wake up and enter acquisition mode. To achieve 14-bit accuracy, allow 12ms (C_{REFADJ} = 0.1µF, C_{REF} = 10µF) for the internal reference to wake up.

Internal and External Reference

Internal Reference

The internal reference of the MAX1156/MAX1158/MAX1174 is internally buffered to provide +4.096V output at REF. Bypass REF to AGND and REFADJ to AGND with 10µF and 0.1µF, respectively. Sink or source current at REFADJ to make fine adjustments to the internal reference. The input impedance of REFADJ is nominally 5kΩ. Use the circuit of Figure 7 to adjust the internal reference to ±1.5%.

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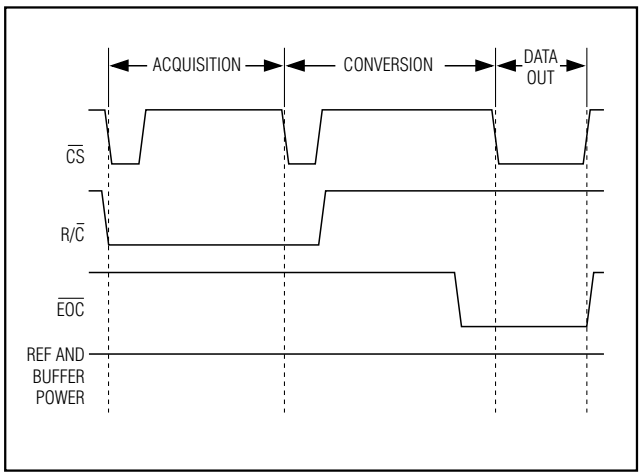

Figure 5. Selecting Standby Mode

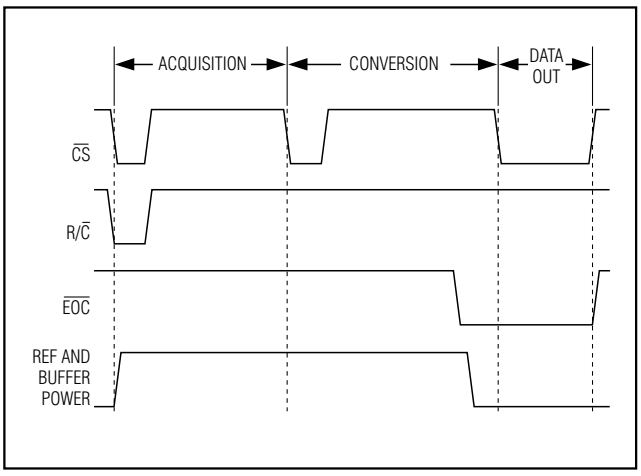

Figure 6. Selecting Shutdown Mode

External Reference

An external reference can be placed at either the input (REFADJ) or the output (REF) of the MAX1156/MAX1158/MAX1174's internal buffer amplifier. Using the buffered REFADJ input makes buffering the external reference unnecessary. The input impedance of REFADJ is typically 5kΩ. The internal buffer output must be bypassed at REF with a 10µF capacitor.

Connect REFADJ to AV_{DD} to disable the internal buffer. Directly drive REF using an external 3.8V to 4.2V reference. During conversion, the external reference must be able to drive 100µA of DC load current and have an output impedance of 10Ω or less.

For optimal performance, buffer the reference through an op amp and bypass REF with a 10µF capacitor. Consider the MAX1156/MAX1158/MAX1174's equivalent input noise (0.32LSB) when choosing a reference.

Reading the Conversion Result

$\overline{EOC}$ is provided to flag the microprocessor when a conversion is complete. The falling edge of $\overline{EOC}$ signals that the data is valid and ready to be output to the bus. D0–D13 are the parallel outputs of the MAX1156/MAX1158/MAX1174. These three-state outputs allow for direct connection to a microcontroller I/O bus. The outputs remain high-impedance during acquisition and conversion. Data is loaded onto the output bus with the third falling edge of $\overline{CS}$ with R/$\overline{C}$ high (after t_{DO}). Bringing $\overline{CS}$ high forces the output bus back to high impedance. The MAX1156/MAX1158/MAX1174 then wait for the next falling edge of $\overline{CS}$ to start the next conversion cycle (see Figure 2).

HBEN toggles the output between the high/low byte. The low byte is loaded onto the output bus when HBEN is low and the high byte is on the bus when HBEN is high. The two MSBs of the high byte are always zero.

Transfer Function

Figures 8, 9, and 10 show the MAX1156/MAX1158/MAX1174 output transfer functions. The MAX1158 and MAX1174 outputs are coded in offset binary, while the MAX1156 is coded in standard binary.

Input Buffer

Most applications require an input buffer amplifier to achieve 14-bit accuracy and prevent loading the source. Switch the channels immediately after acquisition, rather than near the end of or after a conversion, when the input signal is multiplexed. This allows more time for the input buffer amplifier to respond to a large step-change in input signal. The input amplifier must have a high enough slew rate to complete the required output voltage change before the beginning of the acquisition time. Figure 11 shows an example of this circuit using the MAX427.

Figures 12a and 12b show how the MAX1158 and MAX1174 analog input current varies depending on whether the chip is operating or powered down. The part is fully powered down between conversions if the voltage at R/$\overline{C}$ is set high during the second falling edge of $\overline{CS}$. The input current abruptly steps to the powered up value at the start of acquisition. This step in the input current can disrupt the ADC input, depending on the driving circuit's output impedance at high frequencies. If the driving circuit cannot fully settle by

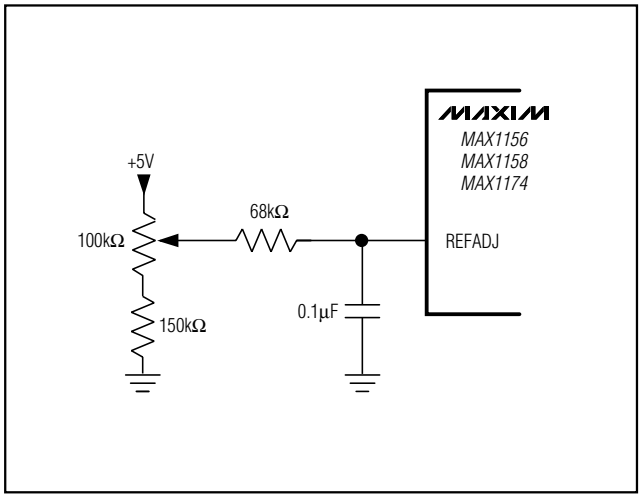

Figure 7. MAX1156/MAX1158/MAX1174 Reference Adjust Circuit

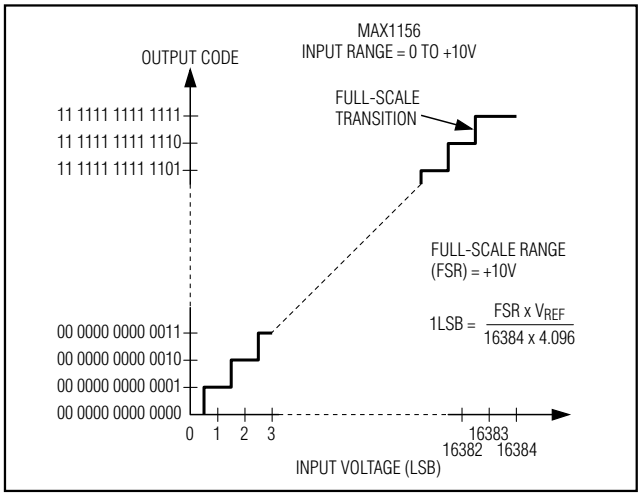

Figure 8. MAX1156 Transfer Function

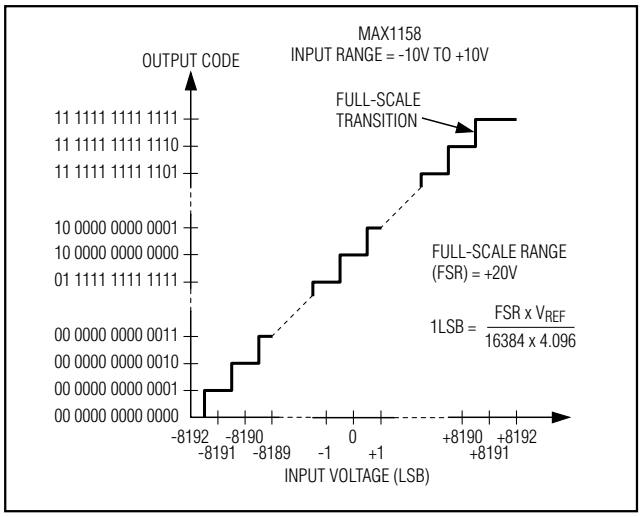

Figure 9. MAX1158 Transfer Function

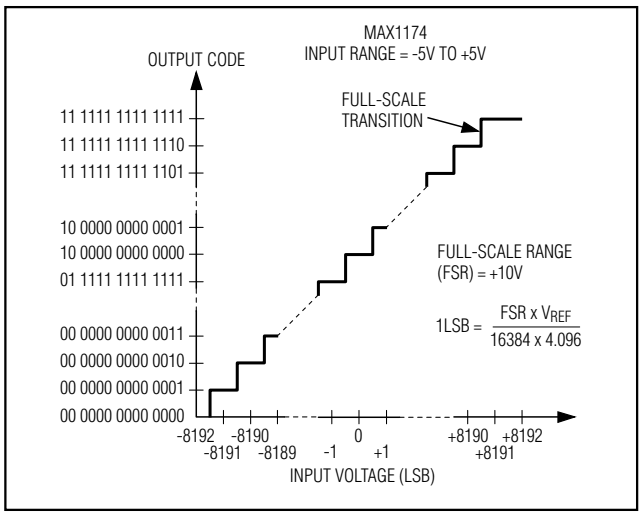

Figure 10. MAX1174 Transfer Function

the end of acquisition, the accuracy of the system can be compromised. To avoid this situation, increase the acquisition time, use a driving circuit that can settle within t_{ACQ}, or leave the MAX1158/MAX1174 powered up by setting the voltage at R/$\overline{C}$ low during the second falling edge of $\overline{CS}$.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Do not run analog and digital lines parallel to each other, and do not layout digital signal paths underneath the ADC package. Use separate analog and digital ground planes with only one point connecting the two ground systems (analog and digital) as close to the device as possible.

Route digital signals far away from sensitive analog and reference inputs. If digital lines must cross analog lines, do so at right angles to minimize coupling digital noise onto the analog lines. If the analog and digital sections share the same supply, isolate the digital and analog

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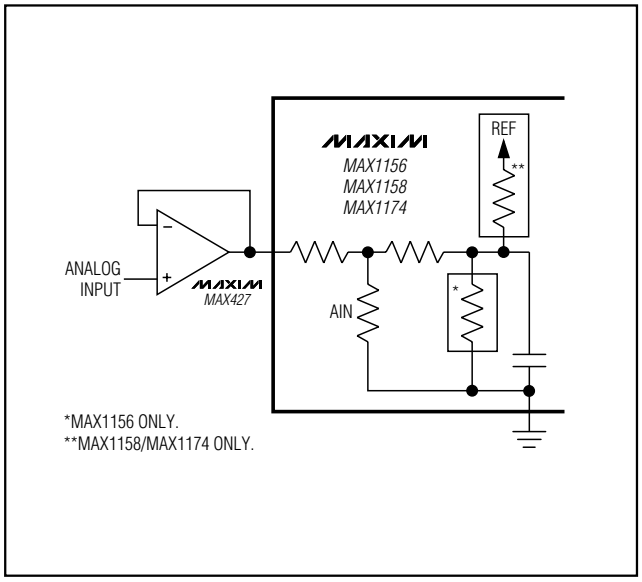

Figure 11. MAX1156/MAX1158/MAX1174 Fast-Settling Input Buffer

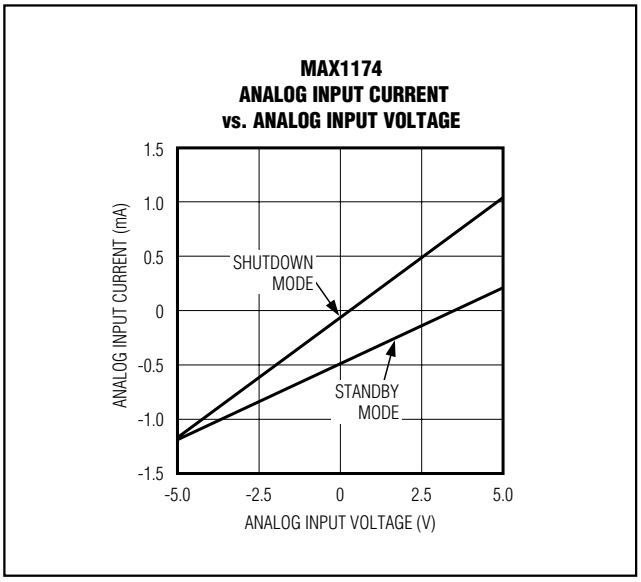

Figure 12a. MAX1174 Analog Input Current

supply by connecting them with a low value (10Ω) resistor or ferrite bead.

The ADC is sensitive to high-frequency noise on the AV_{DD} supply. Bypass AV_{DD} to AGND with a 0.1µF capacitor in parallel with a 1µF to 10µF low-ESR capacitor with the smallest capacitor closest to the device. Keep capacitor leads short to minimize stray inductance.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1156/MAX1158/MAX1174 are measured using the endpoint method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step-width and the ideal value of 1LSB. A DNL error specification of 1LSB guarantees no missing codes and a monotonic transfer function.

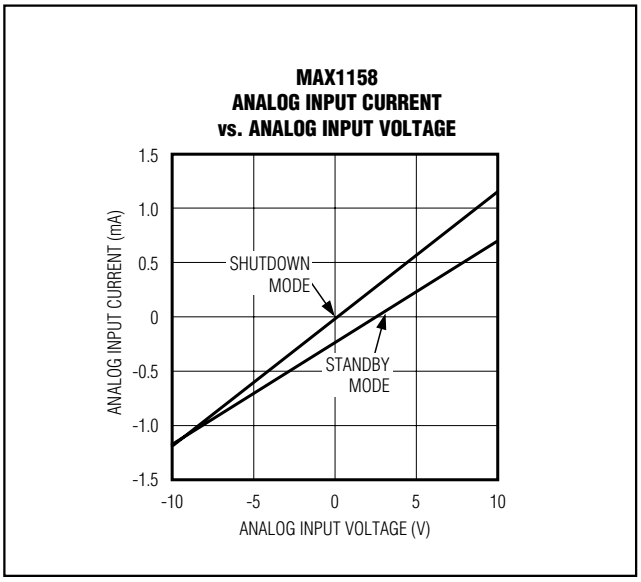

Figure 12b. MAX1158 Analog Input Current

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)\ dB$$

where N = 14 bits.

In reality, there are other noise sources besides quantization noise; thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals.

$$SINAD(dB) = 20 \times \log\left[\frac{Signal_{RMS}}{(Noise + Distortion)_{RMS}}\right]$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}\right]$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest frequency component.

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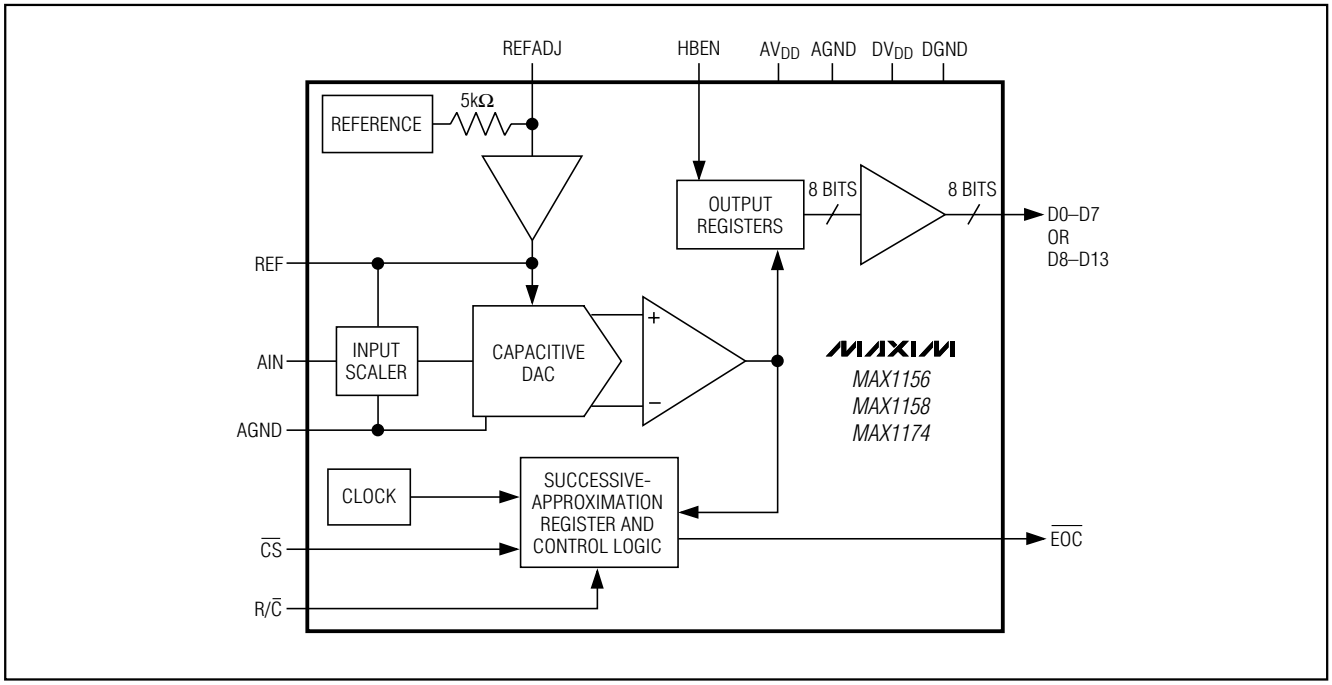
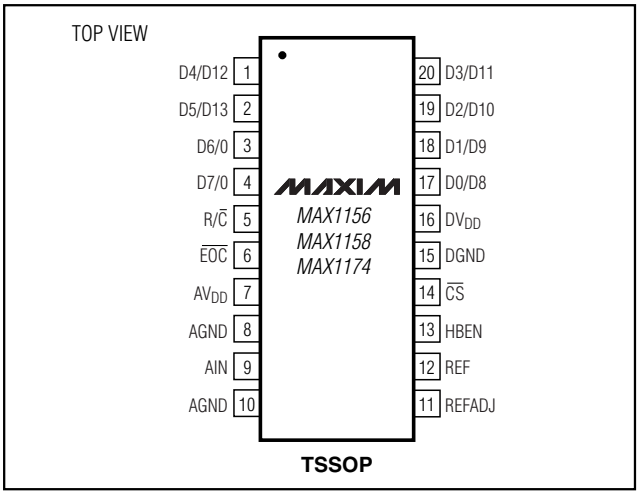
Functional Diagram



Pin Configuration



TSSOP

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	INPUT VOLTAGE RANGE
MAX1158ACUP	0°C to +70°C	20 TSSOP	±10V
MAX1158BCUP	0°C to +70°C	20 TSSOP	±10V
MAX1158AEUP	-40°C to +85°C	20 TSSOP	±10V
MAX1158BEUP	-40°C to +85°C	20 TSSOP	±10V
MAX1174ACUP	0°C to +70°C	20 TSSOP	±5V
MAX1174BCUP	0°C to +70°C	20 TSSOP	±5V
MAX1174AEUP	-40°C to +85°C	20 TSSOP	±5V
MAX1174BEUP	-40°C to +85°C	20 TSSOP	±5V

Chip Information

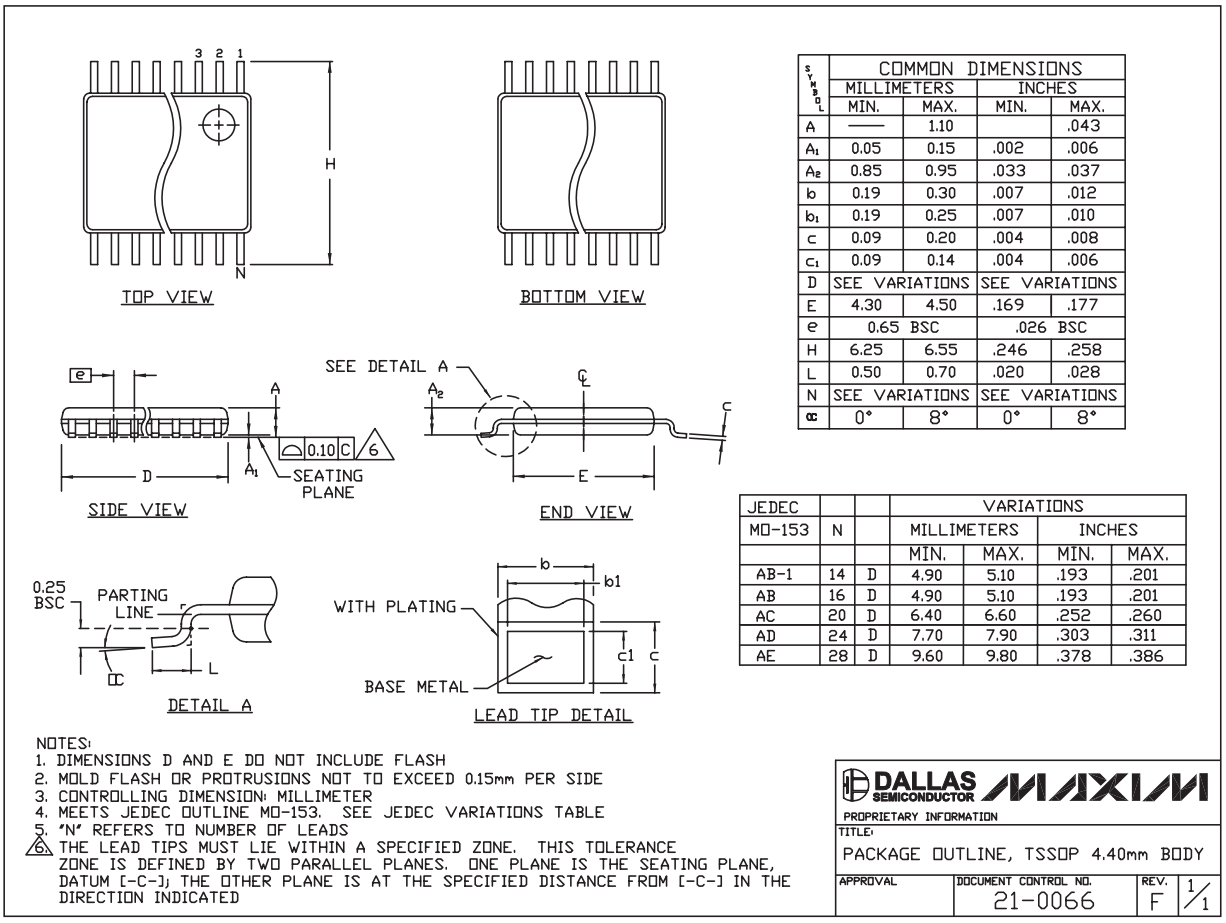
TRANSISTOR COUNT: 15,383

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1