

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT21 Dual 4-input AND gate

Product specification
File under Integrated Circuits, IC06

December 1990

Dual 4-input AND gate

74HC/HCT21

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT21 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT21 provide the 4-input AND function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|---|--|---------|-----|------|
| | | | HC | HCT | |
| t_{PHL}/t_{PLH} | propagation delay nA, nB, nC, nD to nY | $C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$ | 10 | 12 | ns |
| C_I | input capacitance | | 3.5 | 3.5 | pF |
| C_{PD} | power dissipation capacitance per package | notes 1 and 2 | 15 | 16 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

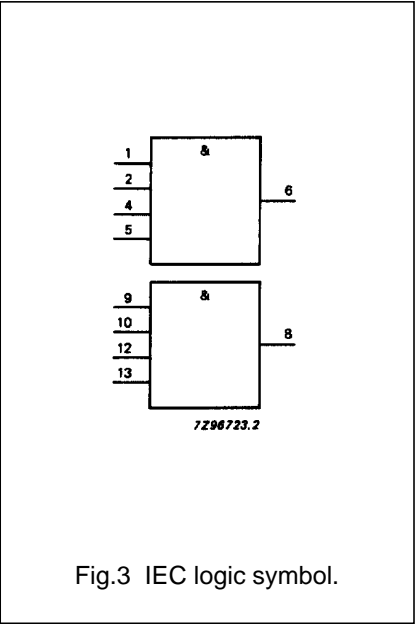
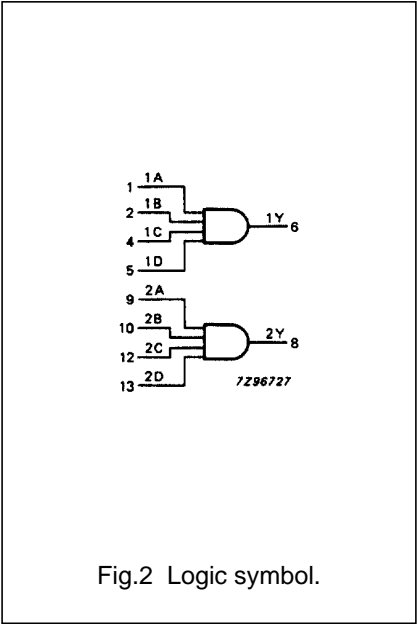
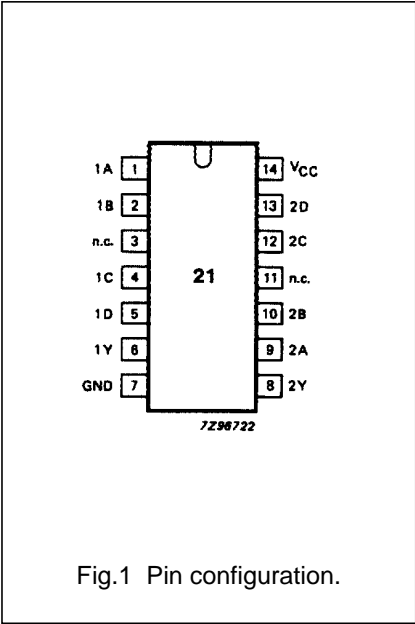
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Dual 4-input AND gate

74HC/HCT21

PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---------|-----------------|-------------------------|
| 1, 9 | 1A, 2A | data inputs |
| 2, 10 | 1B, 2B | data inputs |
| 3, 11 | n.c. | not connected |
| 4, 12 | 1C, 2C | data inputs |
| 5, 13 | 1D, 2D | data inputs |
| 6, 8 | 1Y, 2Y | data outputs |
| 7 | GND | ground (0 V) |
| 14 | V _{CC} | positive supply voltage |



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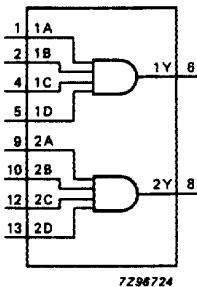


Fig.4 Functional diagram.

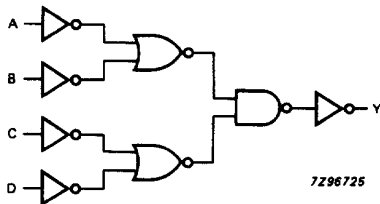


Fig.5 Logic diagram (one gate).

FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|----|----|----|--------|
| nA | nB | nC | nD | nY |
| L | X | X | X | L |
| X | L | X | X | L |
| X | X | L | X | L |
| X | X | X | L | L |
| H | H | H | H | H |

Notes

- 1. H = HIGH voltage level
L = LOW voltage level
X = don't care

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|---|-----------------------|------|------|-----------|------|------------|------|------|------------------------|-----------|
| | | 74HC | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | −40 to+85 | | −40 to+125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay nA, nB, nC, nD to nY | | 33 | 110 | | 140 | | 165 | ns | 2.0 | Fig.6 |
| | | | 12 | 22 | | 28 | | 33 | | 4.5 | |
| | | | 10 | 19 | | 24 | | 28 | | 6.0 | |
| t _{THL} / t _{TLH} | output transition time | | 19 | 75 | | 95 | | 110 | ns | 2.0 | Fig.6 |
| | | | 7 | 15 | | 19 | | 22 | | 4.5 | |
| | | | 6 | 13 | | 16 | | 19 | | 6.0 | |

Dual 4-input AND gate

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

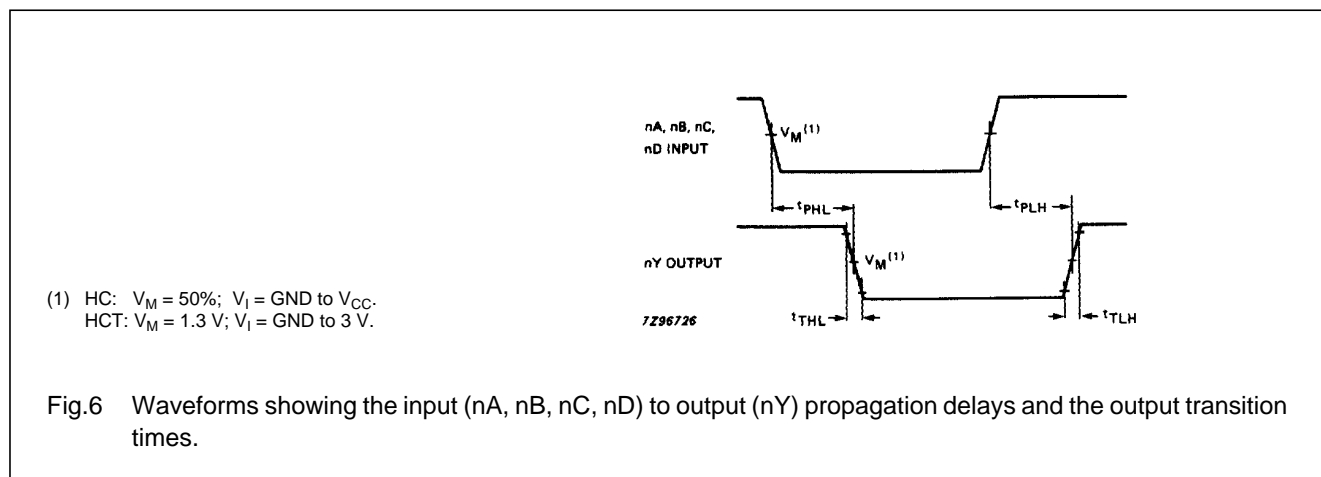
| INPUT | UNIT LOAD COEFFICIENT |
|---------|-----------------------|
| nA, nB, | 1.50 |
| nC, nD | 1.50 |

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|--|-----------------------|------|------|-----------|------|------------|------|------|------------------------|-----------|
| | | 74HCT | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | −40 to+85 | | −40 to+125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay nA, nB nC, nD to nY | | 15 | 27 | | 34 | | 41 | ns | 4.5 | Fig.6 |
| t _{THL} / t _{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.6 |

AC WAVEFORMS



PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.