



# CYPRESS

## PRELIMINARY

## CY7C199B

### 32K x 8 Static RAM

#### Features

- High speed
  - 10 ns
- Fast  $t_{DOE}$
- CMOS for optimum speed/power
- Low active power
  - 495 mW (max, 10 ns “L” version)
- Low standby power
  - 0.275 mW (max, “L” version)
- 2V data retention (“L” version only)
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

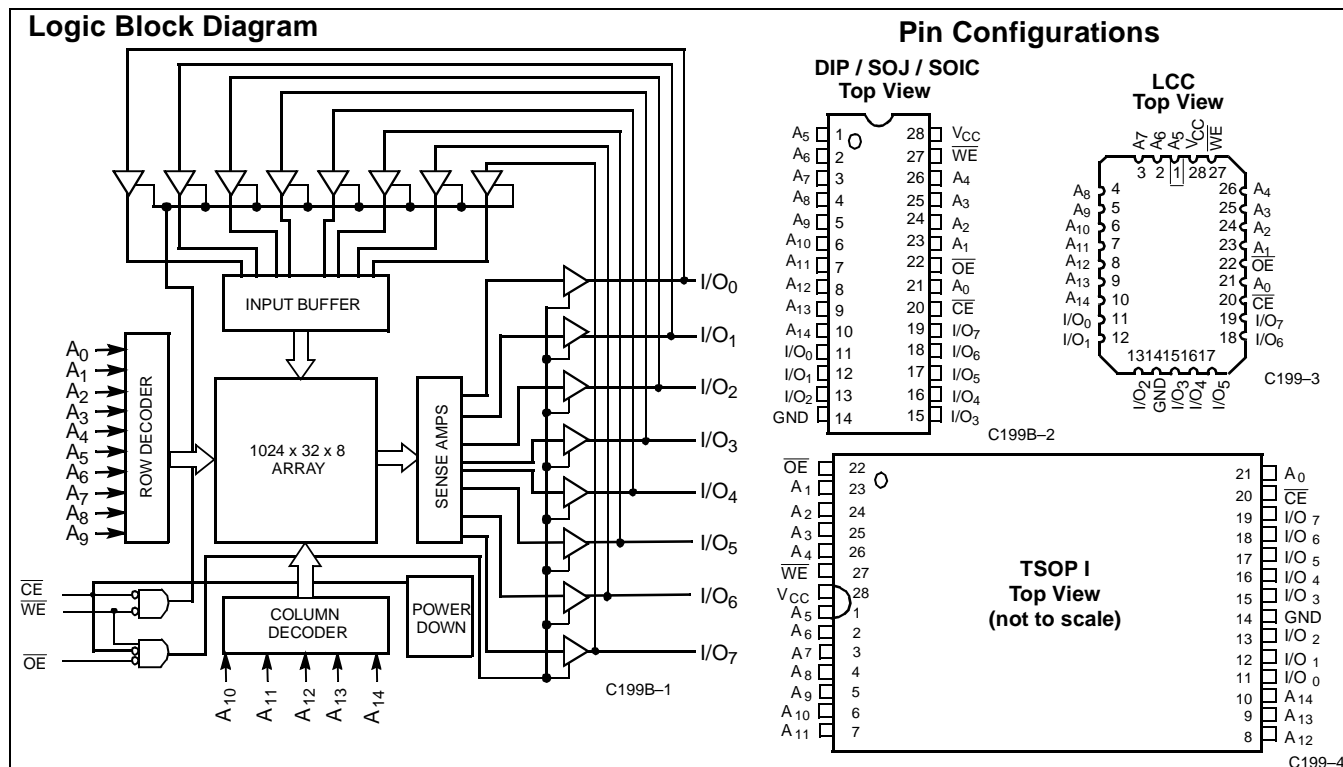
#### Functional Description

The CY7C199B is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion

is provided by an active LOW Chip Enable ( $\overline{CE}$ ) and active LOW Output Enable ( $\overline{OE}$ ) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199B is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW Write Enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{14}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ( $\overline{WE}$ ) is HIGH. A die coat is used to improve alpha immunity.



#### Selection Guide

	199B-8	199B-10	199B-12	199B-15	199B-20	199B-25	199B-35	199B-45
Maximum Access Time (ns)	8	10	12	15	20	25	35	45
Maximum Operating Current (mA)	120	110	160	155	150	150	140	140
Maximum CMOS Standby Current (mA)	0.5	0.5	10	10	10	10	10	10
	0.05	0.05	0.05	0.05	0.05	0.05	0.05	

Shaded area contains advance information.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range<sup>[3]</sup>

Parameter	Description	Test Conditions	7C199B-8		7C199B-10		7C199B-12		7C199B-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
$V_{IL}$	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	-5	+5	-5	+5	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	Com'l	120		110		160		155	mA
			L			85		85		100	mA
			Mil							180	mA
$I_{SB1}$	Automatic CE Power-Down Current— TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	Com'l	5		5		30		30	mA
			L			5		5		5	mA
$I_{SB2}$	Automatic CE Power-Down Current— CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = 0$	Com'l	0.5		0.5		10		10	mA
			L	0.05		0.05		0.05		0.05	mA
			Mil							15	mA

Shaded area contains advance information.

**Notes:**

- $V_{IL}(\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- $T_A$  is the case temperature.
- See the last page of this specification for Group A subgroup testing information.

**Electrical Characteristics** Over the Operating Range<sup>[3]</sup> (continued)

Parameter	Description	Test Conditions	7C199B-20		7C199B-25		7C199B-35		7C199B-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l	150		150		140		140	mA
			L	90		80		70		70	mA
			Mil	170		150		150		150	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com'l	30		30		25		25	mA
			L	5		5		5		5	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l	10		10		10		10	mA
			L	0.05		0.05		0.05		0.05	μA
			Mil	15		15		15		15	mA

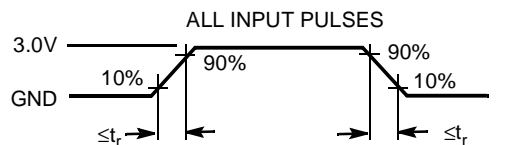
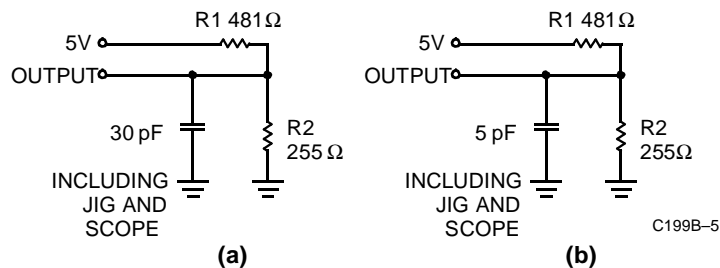
**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Note:**

4. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

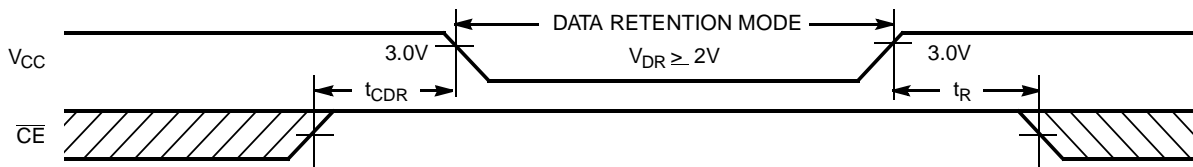
167  $\Omega$

OUTPUT  $\rightarrow$  1.73V

## Data Retention Characteristics Over the Operating Range (L version only)

Parameter	Description		Conditions <sup>[5]</sup>	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention			2.0		V
I <sub>CCDR</sub>	Data Retention Current	Com'I	V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V			μA
		Com'I L			10	μA
t <sub>CDR</sub> <sup>[4]</sup>	Chip Deselect to Data Retention Time			0		ns
t <sub>R</sub>	Operation Recovery Time			200		μs

## Data Retention Waveform



### Note:

5. No input may exceed  $V_{CC} + 0.5V$ .

**Switching Characteristics** Over the Operating Range<sup>[3, 6]</sup>

Parameter	Description	7C199B-8		7C199B-10		7C199B-12		7C199B-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t <sub>RC</sub>	Read Cycle Time	8		10		12		15		ns
t <sub>AA</sub>	Address to Data Valid		8		10		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		4.5		5		5		7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[7]</sup>	0		0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup>		5		5		5		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup>		4		5		5		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		8		10		12		15	ns
WRITE CYCLE <sup>[9, 10]</sup>										
t <sub>WC</sub>	Write Cycle Time	8		10		12		15		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	7		7		9		10		ns
t <sub>AW</sub>	Address Set-Up to Write End	7		7		9		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	7		7		8		9		ns
t <sub>SD</sub>	Data Set-Up to Write End	5		5		8		9		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[8]</sup>		5		6		7		7	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		3		ns

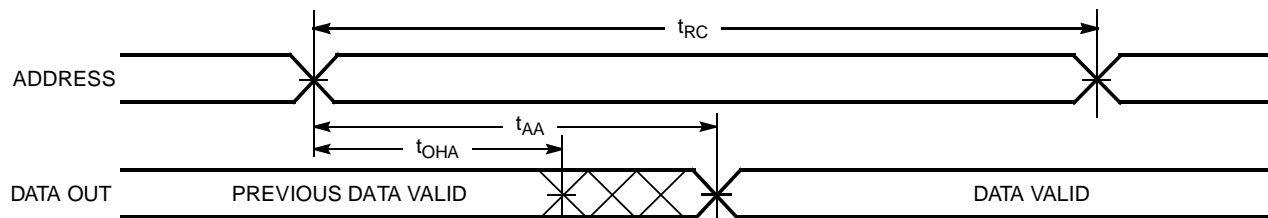
Shaded area contains advance information.

**Notes:**

6. Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
7. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
8.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Characteristics** Over the Operating Range<sup>[3,6]</sup> (continued)

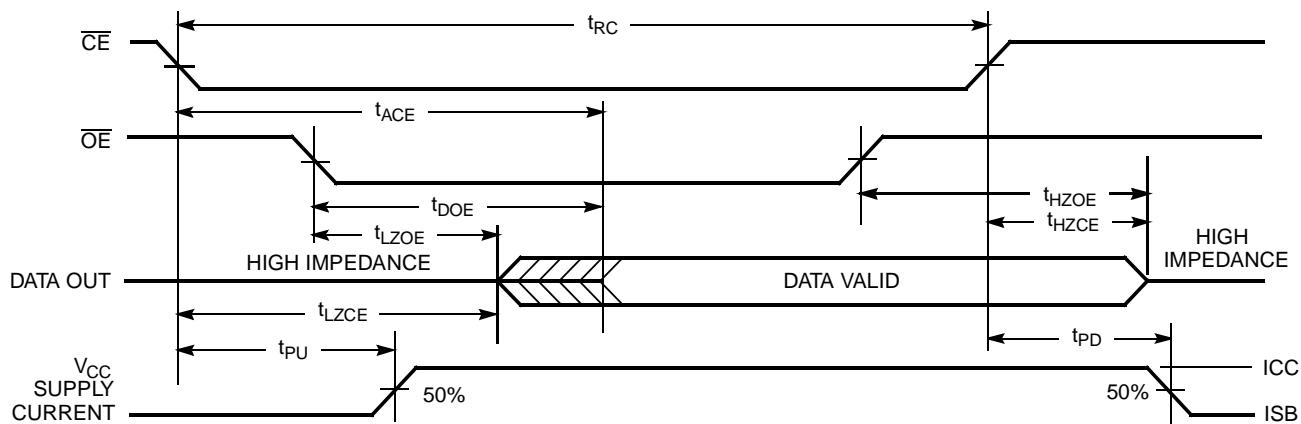
Parameter	Description	7C199B-20		7C199B-25		7C199B-35		7C199B-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t <sub>RC</sub>	Read Cycle Time	20		25		35		45		ns
t <sub>AA</sub>	Address to Data Valid		20		25		35		45	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		20		25		35		45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		9		10		16		16	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[7]</sup>	0		0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup>		9		11		15		15	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup>		9		11		15		15	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		20		20		20		25	ns
WRITE CYCLE <sup>[9,10]</sup>										
t <sub>WC</sub>	Write Cycle Time	20		25		35		45		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	15		18		22		22		ns
t <sub>AW</sub>	Address Set-Up to Write End	15		20		30		40		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	15		18		22		22		ns
t <sub>SD</sub>	Data Set-Up to Write End	10		10		15		15		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[8]</sup>		10		11		15		15	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		3		ns

**Switching Waveforms**
**Read Cycle No. 1**<sup>[11, 12]</sup>


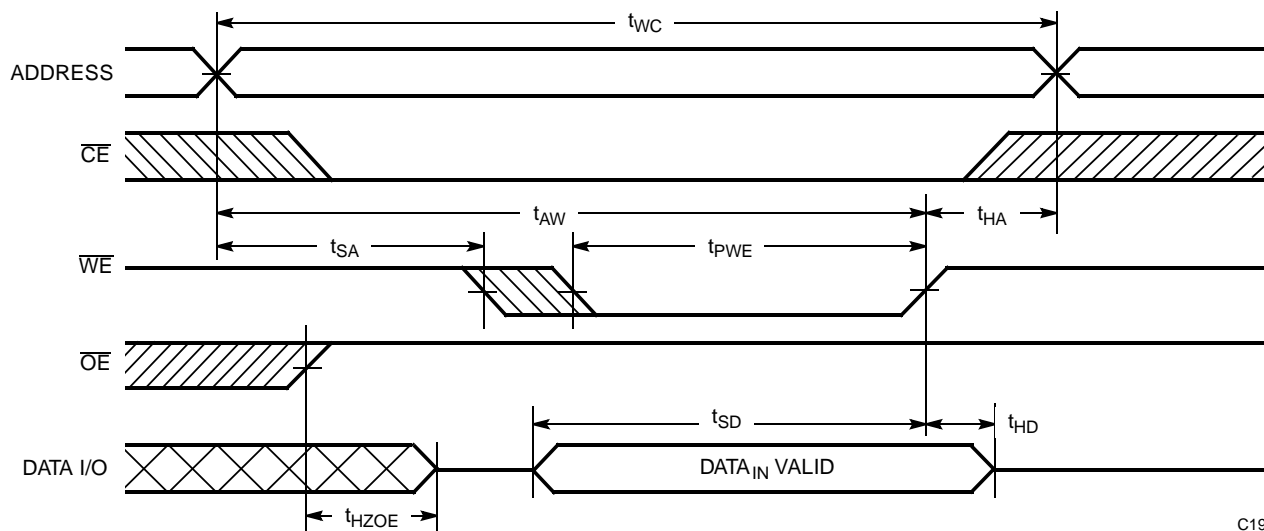
C199B-8

**Notes:**

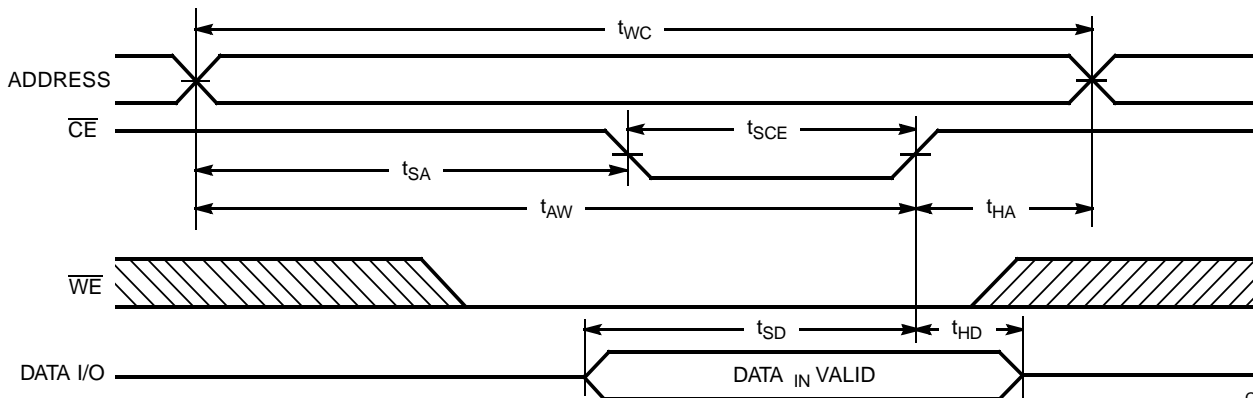
11. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
12.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms (continued)**
**Read Cycle No. 2** [12, 13]


C199B-9

**Write Cycle No. 1 (WE Controlled)** [9, 14, 15]


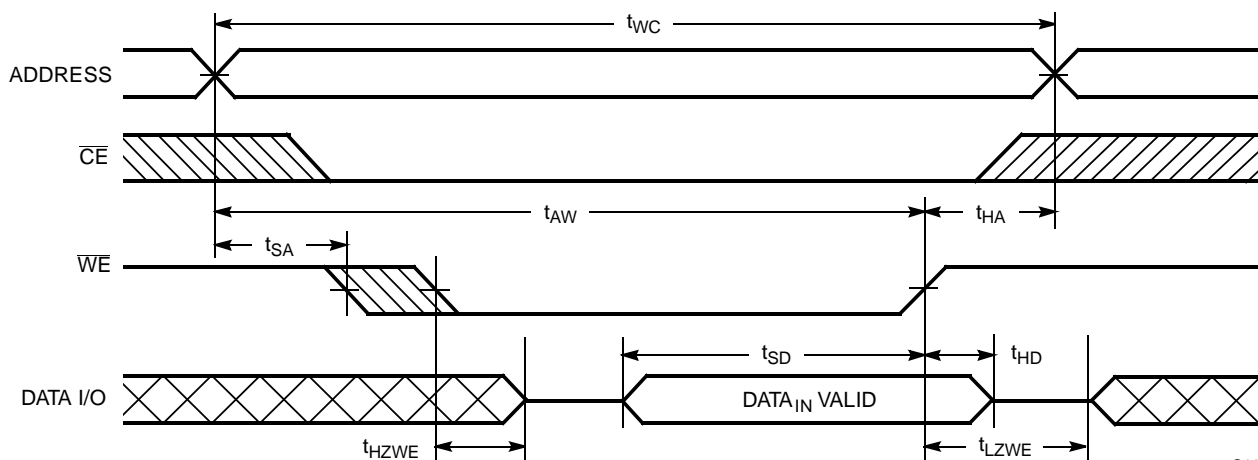
C199B-10

**Write Cycle No. 2 (CE Controlled)** [9, 14, 15]


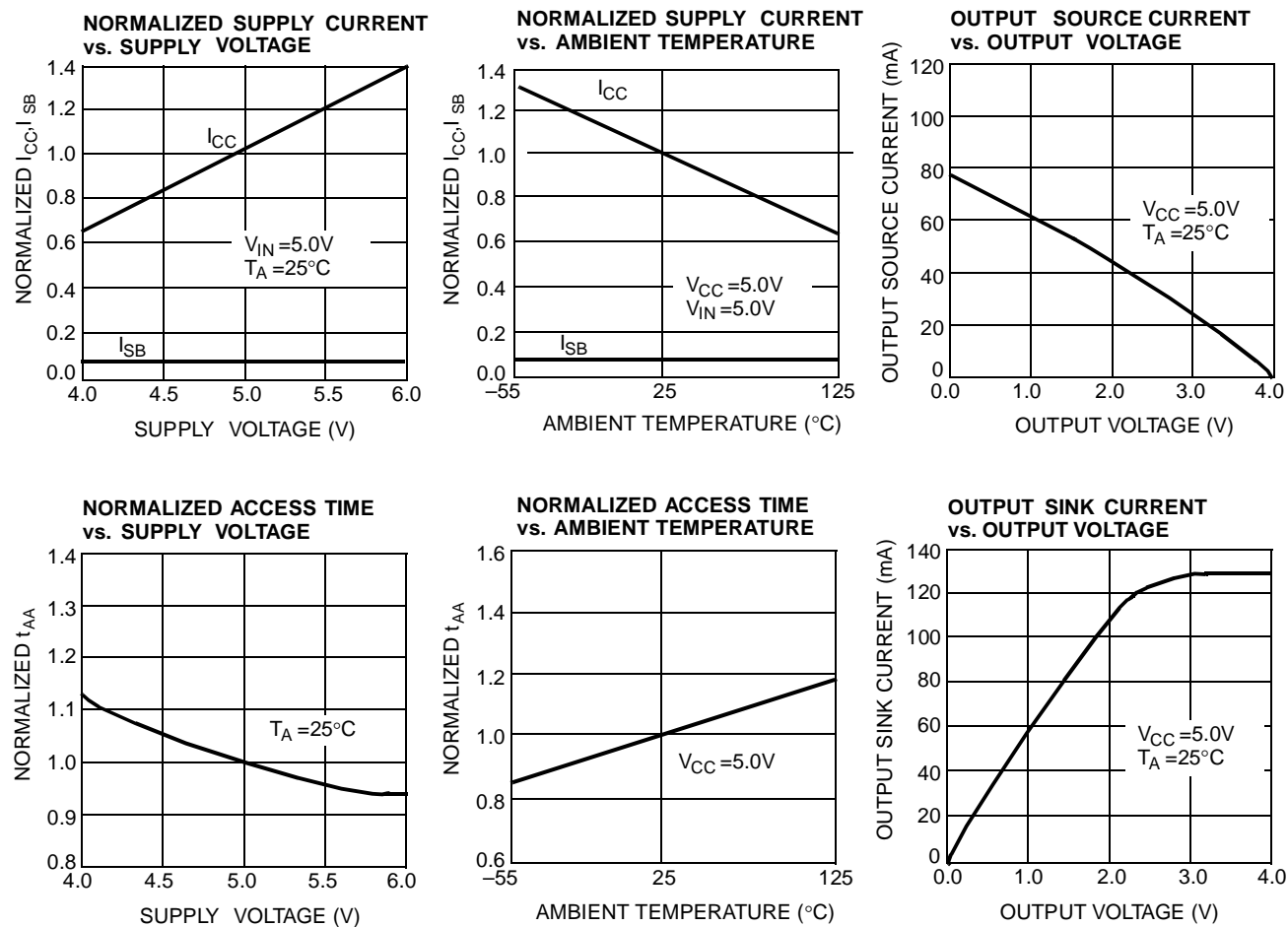
C199B-11

**Notes:**

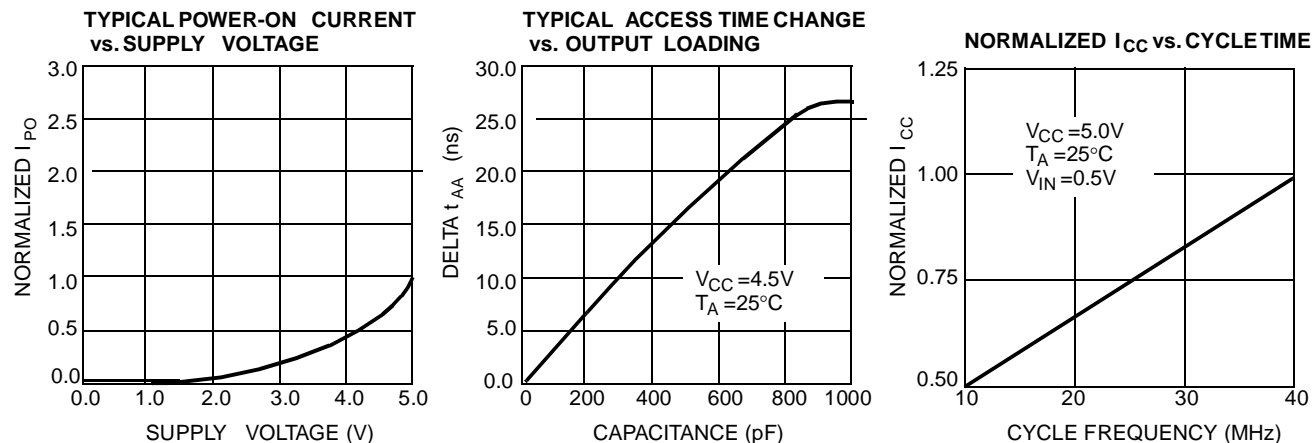
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
14. Data I/O is high impedance if  $OE = V_{IH}$ .
15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 3 (WE Controlled  $\overline{OE}$  LOW)**<sup>[10, 15]</sup>


C199B-12

**Typical DC and AC Characteristics**




**Typical DC and AC Characteristics (continued)**

**Truth Table**

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C199B-8VC	V21	28-Lead Molded SOJ	Commercial
	CY7C199B-8ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199BL-8VC	V21	28-Lead Molded SOJ	
	CY7C199BL-8ZC	Z28	28-Lead Thin Small Outline Package	
10	CY7C199B-10VC	V21	28-Lead Molded SOJ	Commercial
	CY7C199B-10ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199BL-10VC	V21	28-Lead Molded SOJ	
	CY7C199BL-10ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199B-10VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199B-10ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199BL-10VI	V21	28-Lead Molded SOJ	
	CY7C199BL-10ZI	Z28	28-Lead Thin Small Outline Package	
12	CY7C199B-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199B-12VC	V21	28-Lead Molded SOJ	
	CY7C199B-12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199BL-12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199BL-12VC	V21	28-Lead Molded SOJ	
	CY7C199BL-12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199B-12VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199B-12ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199BL-12VI	V21	28-Lead Molded SOJ	
	CY7C199BL-12ZI	Z28	28-Lead Thin Small Outline Package	

Shaded area contains advance information. Contact your Cypress sales representative for availability

**Ordering Information** (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C199B-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199B-15VC	V21	28-Lead Molded SOJ	
	CY7C199B-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199BL-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199BL-15VC	V21	28-Lead Molded SOJ	
	CY7C199BL-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199B-15VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199B-15ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199B-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199B-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199BL-15DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199BL-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C199B-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199B-20VC	V21	28-Lead Molded SOJ	
	CY7C199B-20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199BL-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199BL-20VC	V21	28-Lead Molded SOJ	
	CY7C199BL-20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199B-20VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199B-20ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199B-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199B-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199BL-20DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199BL-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C199B-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199B-25SC	S21	28-Lead Molded SOIC	
	CY7C199B-25VC	V21	28-Lead Molded SOJ	
	CY7C199B-25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199BL-25ZI	Z28	28-Lead Thin Small Outline Package	Industrial
	CY7C199B-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199B-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C199B-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199B-35SC	S21	28-Lead Molded SOIC	
	CY7C199B-35VC	V21	28-Lead Molded SOJ	
	CY7C199B-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199B-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199B-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C199B-45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199B-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advance information. Contact your Cypress sales representative for availability

**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**
**DC Characteristics**

Parameter	Subgroups
$V_{OH}$	1, 2, 3
$V_{OL}$	1, 2, 3
$V_{IH}$	1, 2, 3
$V_{IL}$ Max.	1, 2, 3
$I_{IX}$	1, 2, 3
$I_{OZ}$	1, 2, 3
$I_{CC}$	1, 2, 3
$I_{SB1}$	1, 2, 3
$I_{SB2}$	1, 2, 3

**Switching Characteristics**

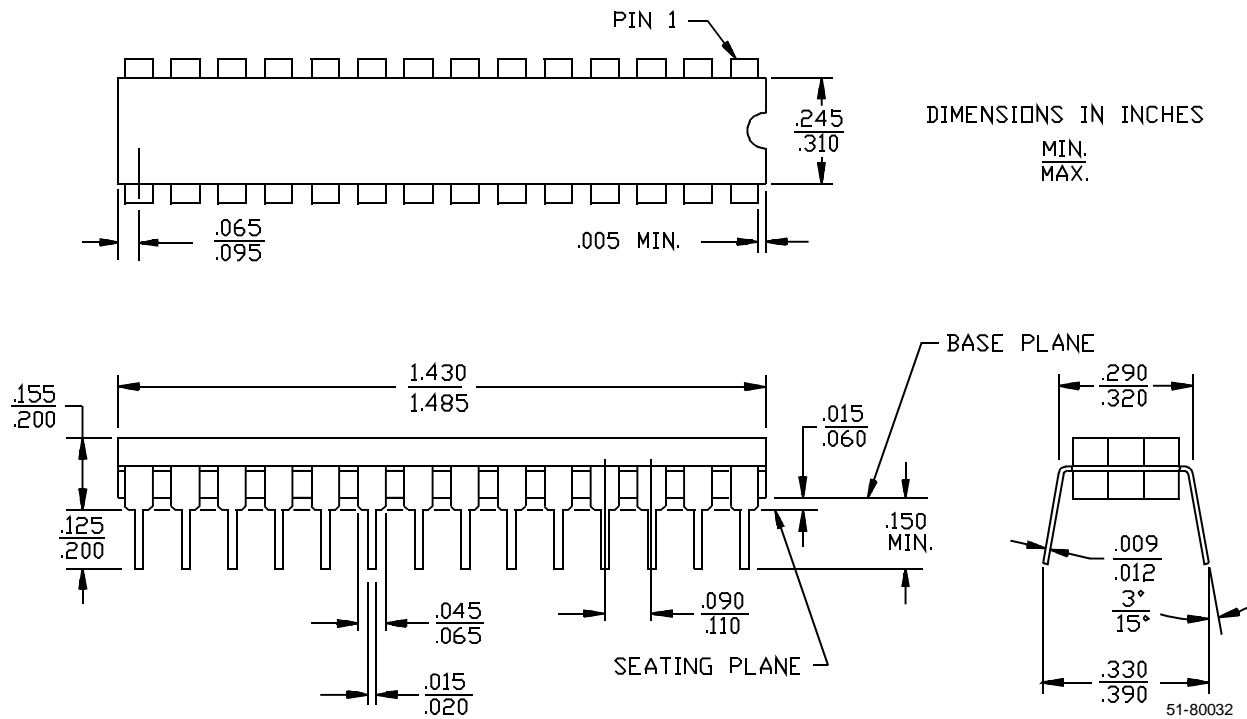
Parameter	Subgroups
<b>READ CYCLE</b>	
$t_{RC}$	7, 8, 9, 10, 11
$t_{AA}$	7, 8, 9, 10, 11
$t_{OHA}$	7, 8, 9, 10, 11
$t_{ACE}$	7, 8, 9, 10, 11
$t_{DOE}$	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
$t_{WC}$	7, 8, 9, 10, 11
$t_{AA}$	7, 8, 9, 10, 11
$t_{AW}$	7, 8, 9, 10, 11
$t_{HA}$	7, 8, 9, 10, 11
$t_{SA}$	7, 8, 9, 10, 11
$t_{PWE}$	7, 8, 9, 10, 11
$t_{SD}$	7, 8, 9, 10, 11
$t_{HD}$	7, 8, 9, 10, 11

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## Package Diagrams

### 28-Lead (300-Mil) CerDIP D22

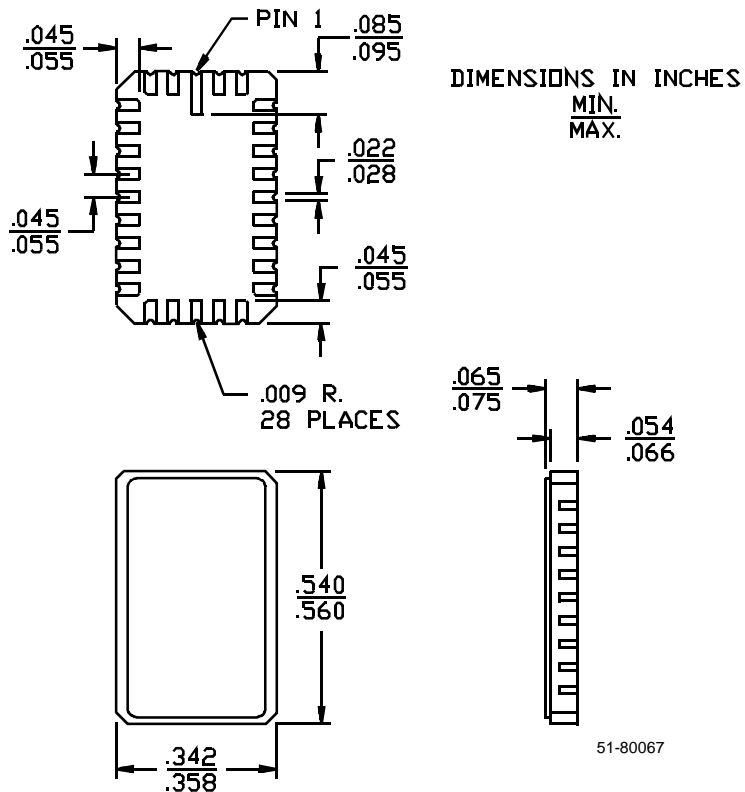
MIL-STD-1835 D-15 Config. A



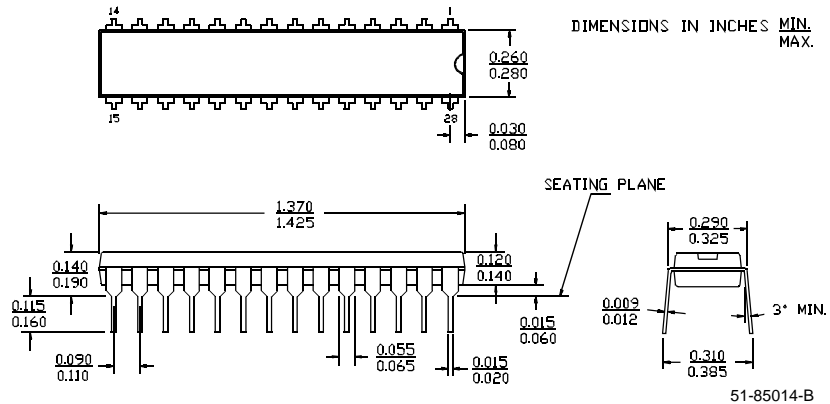
**Package Diagrams (continued)**

**28-Pin Rectangular Leadless Chip Carrier L54**

MIL-STD-183C-11A

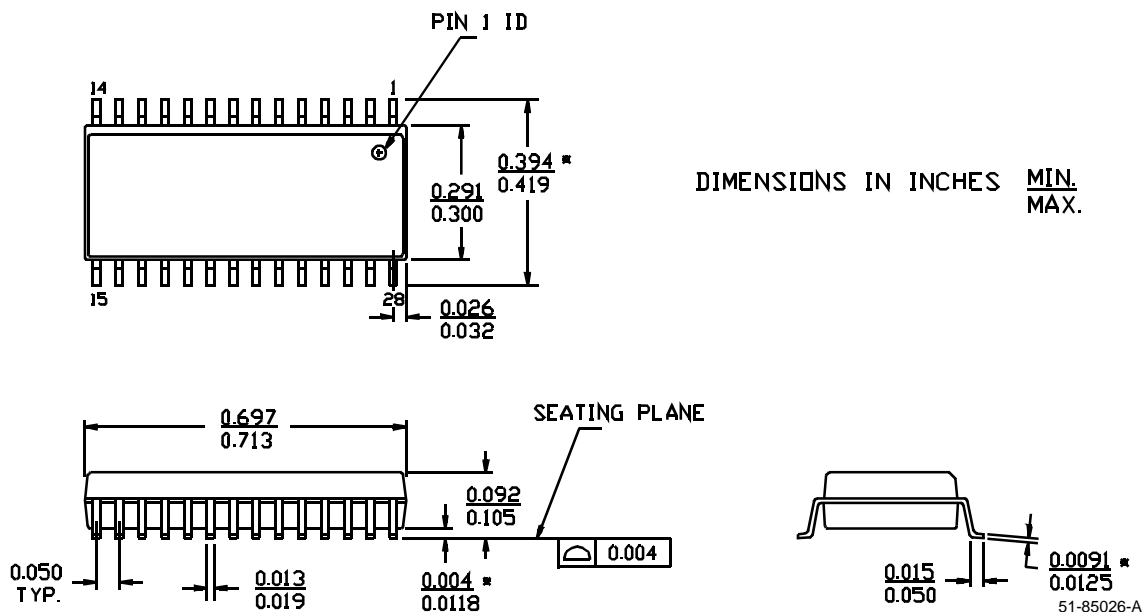


**28-Lead (300-Mil) Molded DIP P21**

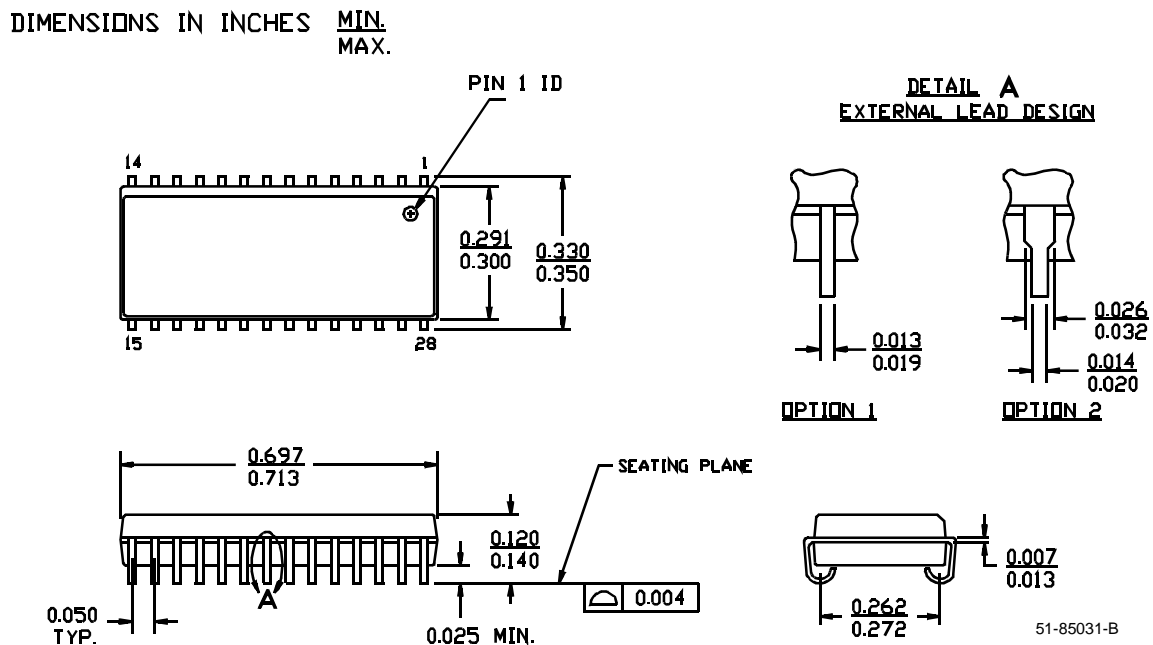


**Package Diagrams** (continued)

**28-Lead (300-Mil) Molded SOIC S21**



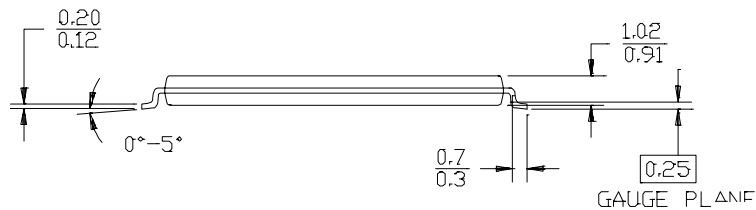
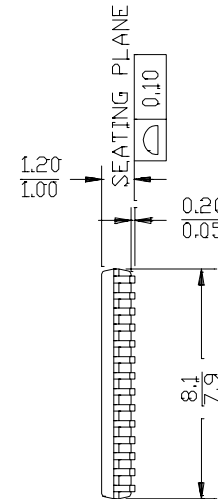
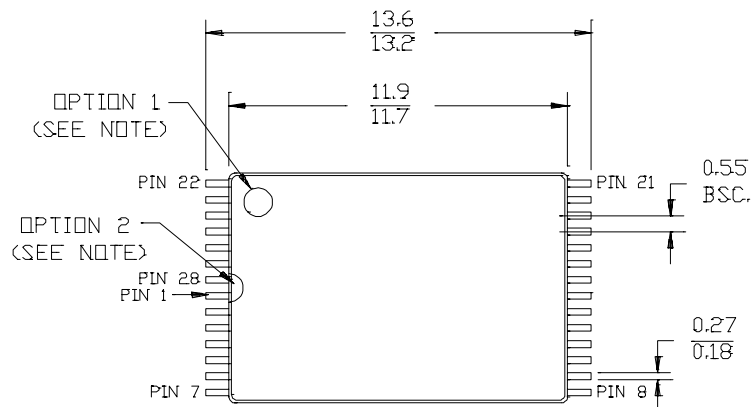
**28-Lead (300-Mil) Molded SOJ V21**



**Package Diagrams (continued)**

**28-Lead Thin Small Outline Package Z28**

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER  
AS SHOWN IN OPTION 1 OR OPTION 2



DIMENSION IN MM  
MAX.  
MIN.

51-85071-F