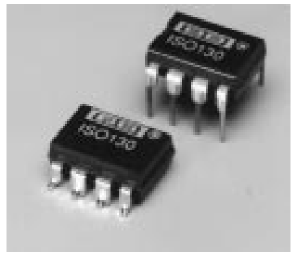
BURR - BROWN®

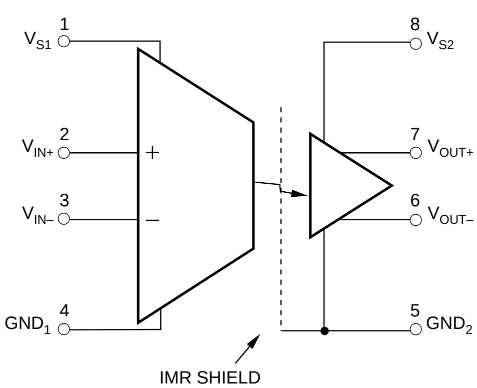


ISO130

High IMR, Low Cost ISOLATION AMPLIFIER

FEATURES

- **HIGH ISOLATION-MODE REJECTION: 10kV/μs (min)**
- **LARGE SIGNAL BANDWIDTH: 85kHz (typ)**
- **DIFFERENTIAL INPUT/DIFFERENTIAL OUTPUT**
- **VOLTAGE OFFSET DRIFT vs TEMPERATURE: 4.6μV/°C (typ)**
- **OFFSET VOLTAGE 1.8mV (max)**
- **INPUT REFERRED NOISE: 300μVrms (typ)**
- **NONLINEARITY: 0.25% (max)**
- **SINGLE SUPPLY OPERATION**
- **SIGMA-DELTA A/D CONVERTER TECHNOLOGY**
- **WORLDWIDE SAFETY APPROVAL: UL1577 (File No. E162573), VDE0884 (File No. 85511), CSA22.2 (File No. 88324)**
- **AVAILABLE IN 8-PIN PLASTIC DIP and 8-PIN GULL-WING PLASTIC SURFACE MOUNT**



APPLICATIONS

- **MOTOR AND SCR CONTROL**
- **MOTOR PHASE CURRENT SENSING**
- **INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs**
- **GENERAL PURPOSE ANALOG SIGNAL ISOLATION**
- **POWER MONITORING**
- **GROUND LOOP ELIMINATION**

DESCRIPTION

The ISO130 is a high isolation-mode rejection, isolation amplifier suited for motor control applications. Its versatile design provides the precision and stability needed to accurately monitor motor currents in high-noise motor control environments. The ISO130 can also be used for general analog signal isolation applications requiring stability and linearity under severe noise conditions.

The signal is transmitted digitally across the isolation barrier optically, using a high-speed AlGaAs LED. The remainder of the ISO130 is fabricated on 1μm CMOS IC process. A sigma-delta analog-to-digital converter, chopper stabilized amplifiers and differential input and output topologies make the isolation amplifier suitable for a variety of applications.

The ISO130 is easy to use. No external components are required for operation. The key specifications are 10kV/μs isolation-mode rejection, 85kHz large signal bandwidth, and 4.6μV/°C V_{OS} drift. A single power supply ranging from +4.5V to +5.5V makes this amplifier ideal for low power isolation applications.

The ISO130 is available in 8-pin plastic DIP and 8-pin plastic gull-wing surface mount packages.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1234B Printed in U.S.A. June, 1995

SPECIFICATIONS

ISOLATION SPECIFICATIONS – VDE0884 INSULATION CHARACTERISTICS

At V_{IN}–, V_{IN}– = 0V, T_A = 25°C, V_{S1}, V_{S2} = 5.0V unless otherwise noted.

		ISO130P/ISO130PB ISO130U/ISO130UB	
PARAMETER	**CONDITIONS**	**CHARACTERISTIC**	**UNITS**
ISOLATION CHARACTERISTICS			
Installation Classification	As Per VDE0109/12.83		
Table I			
Rated Mains Voltage ≤ 300Vrms		I-IV	
Rated Mains Voltage ≤ 600Vrms		I-III	
Climatic Classification		40/85/21	
Pollution Degree(1)	As Per VDE0109/12.83	2	
Maximum Working Insulation Voltage (V_{IORM})		600	Vrms
Side A to Side B Test Voltage, Method b (V_{PR})(9)			
Partial Discharge < 5pC	V_{PR} = 1.6 x V_{IORM}, t_P = 1s	960	Vrms
Side A to Side B Test Voltage, Method a (V_{PR})(9)	Type and Sample Test		
Partial Discharge < 5pC	V_{PR} = 1.2 x V_{IORM}, t_P = 60s	720	Vrms
Highest Allowable Overvoltage (V_{TR})(9)	Transient Overvoltage, t_{TR} = 10s	6000	V_{PEAK}
Safety-Limiting Values			
Case Temperature (T_{SI})		175	°C
Input Power ($P_{SI\ (INPUT)}$)		80	mW
Output Power ($P_{SI\ (OUTPUT)}$)		250	mW
INSULATION RELATED SPECIFICATIONS			
Min. External Air Gap (clearance)		> 7	mm
Min. External Tracking Path (creepage)		8	mm
Internal Isolation Gap (clearance)		0.5	mm
Tracking Resistance (CTI)		175	V
Isolation Group	per VDE0109	III a	
Insulation Resistance	25°C, V_{ISO} = 500V	≥ 10^{11}	Ω

SPECIFICATIONS

ISOLATION SPECIFICATIONS

At V_{IN}+, V_{IN}– = 0V, T_A = 25°C, V_{S1}, V_{S2} = 5.0V, unless otherwise noted.

		ISO130P, ISO130PB ISO130U, ISO130UP			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
ISOLATION					
Input-Output Surge Withstand Voltage(8, 9),	t = 1_{MIN}, RH ≤ 50%				
(In accordance with UL1577)		3750			Vrms
Barrier Impedance(9)					
Resistance	V_{ISO} = 500VDC		10^{13}		Ω
Capacitance	f = 1MHz		0.7		pF
Isolation Mode Voltage Errors					
Rising Edge Transient Immunity	V_{IM} = 1kV, ∂ V_{OUT} < 50mV	10	25		kV/µs
Falling Edge Transient Immunity	V_{IM} = 1kV, ∂ V_{OUT} < 50mV	10	15		kV/µs
Isolation Mode Rejection Ratio(2)			> 140		dB

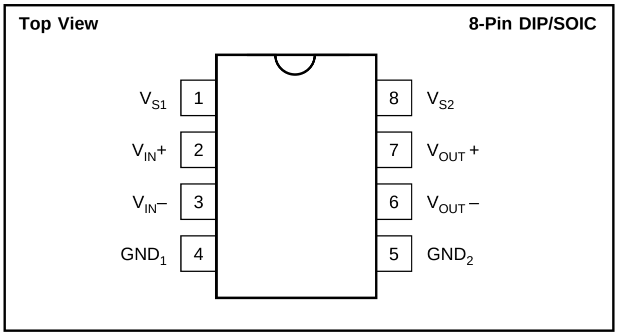
SPECIFICATIONS

At V_{IN}+, V_{IN}– = 0V, T_A = 25°C, V_{S1}, V_{S2} = 5.0V unless otherwise noted.

PARAMETER	CONDITIONS	ISO130P/ISO130PB ISO130U/ISO130UB			UNITS
		MIN	TYP	MAX	
INPUT					
Initial Offset Voltage		–1.8	–0.9	0.0	mV
vs Temperature			4.6		µV/°C
vs V_{S1}			30		µV/V
vs V_{S2}			–40		µV/V
Power Supply Rejection; V_{S1} and V_{S2} Together	1MHz Square Wave, 5ns Rise/Fall Time		5		mV/V
Noise	0.1Hz to 100kHz		300		µVrms
Input Voltage Range		–200		200	mV
Maximum Input Voltage Range before Output Clipping			±300		mV
Initial Input Bias Current(3)			–670		nA
vs Temperature			3		nA/°C
Input Resistance(3)			530		kΩ
vs Temperature			0.38		%/°C
Common-Mode Rejection Ratio(4)			72		dB
GAIN(5)					
Initial Gain					
ISO130P/ISO130U	–200mV < V_{IN}+ < 200mV	7.61	8.00	8.40	V/V
ISO130PB/ISO130UB	–200mV < V_{IN}+ < 200mV	7.85	7.93	8.01	V/V
Gain vs Temperature			10		ppm/°C
Gain vs V_{S1}			2.1		ppm/mV
Gain vs V_{S2}			–0.6		ppm/mV
Gain Nonlinearity					
for –200mV < V_{IN}+ < 200mV			0.2	0.35	%
for –100mV < V_{IN}+ < 100mV			0.1	0.25	%
vs Temperature(6)	–200mV < V_{IN}+ < 200mV		–0.001		% pts/°C
vs V_{S1}(6)	–200mV < V_{IN}+ < 200mV		–0.005		% pts/V
vs V_{S2} (6)	–200mV < V_{IN}+ < 200mV		–0.007		% pts/V
OUTPUT					
Voltage Range					
High	V_{IN}+ = +500mV		3.61		V
Low	V_{IN}+ = –500mV		1.18		V
Common-Mode Voltage	–40°C < T_A < 85°C, 4.5V < V_{S1} < 5.5V	2.2	2.39	2.6	V
Current Drive(7)			1		mA
Short-Circuit Current	V_{OUT} = 0V or V_{OUT} = V_{S2}		9.3		mA
Output Resistance			11		Ω
vs Temperature			0.6		%/°C
FREQUENCY RESPONSE					
Bandwidth					
–3dB	–40°C to 85°C	50	85		kHz
–45°			35		kHz
Rise/Fall Time (10% - 90%)	–40°C to 85°C		4.3	6.6	µs
Propagation Delay					
to 10%	–40°C to 85°C		2.0	3.3	µs
to 50%	–40°C to 85°C		3.4	5.6	µs
to 90%	–40°C to 85°C		6.3	9.9	µs
POWER SUPPLIES					
Rated Voltage			5.0		V
Voltage Range		4.5		5.5	V
Quiescent Current					
V_{S1}	V_{IN}+ = 200mV, –40°C < T_A < 85°C, 4.5V < V_{S1} < 5.5V		10.7	15.5	mA
V_{S2}	–40°C < T_A < 85°C, 4.5V < V_{S1} < 5.5V		11.6	15.5	mA
TEMPERATURE RANGE					
Specification		–40		85	°C
Operating		–40		100	°C
Storage		–55		125	°C
θ_{C-A}			86		°C/W

NOTES: (1) This part may also be used in Pollution Degree 3 environments where the rated mains voltage is 300Vrms (per DIN VDE0109/12.83). (2) IMRR = 20 log ($\partial V_{IN}/\partial V_{ISO}$). (3) Time averaged value. (4) V_{IN}+ = V_{IN}– = V_{CM}. CMRR = 20 log ($\partial V_{CM}/\partial V_{OS}$). (5) The slope of the best-fit line of (V_{OUT+} – V_{OUT-}) vs (V_{IN+} –V_{IN-}). (6) Change in nonlinearity vs temperature or supply voltage expressed in number of percentage points per °C or volt. (7) For best offset voltage performance. (8) For devices with minimum V_{ISO} specified at 3750Vrms, each isolation amplifier is proof-tested by applying an insulation test voltage ≥ 4500Vrms for 1 second (leakage current < 5µA). This specification does not guarantee continuous operation. (9) Pins 1-4 are shorted together and pins 5-8 are shorted together for this test.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltages: V_{S1}, V_{S2} .... 0V to 5.5V
Steady-State Input Voltage .... –2V to V_{S1} + 0.5V
2 Second Transient Input Voltage .... –6.0V
Output Voltages: $V_{OUT}+$, $V_{OUT}–$ .... –0.5V to V_{S2} + 0.5V
Lead Temperature Solder (1.6mm below seating plane, 10s) .... 260°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO130P	8-Pin Plastic DIP	006-3
ISO130PB	8-Pin Plastic DIP	006-3
ISO130U	8-Pin Gull-Wing Plastic Surface Mount	006-2
ISO130UB	8-Pin Gull-Wing Plastic Surface Mount	006-2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

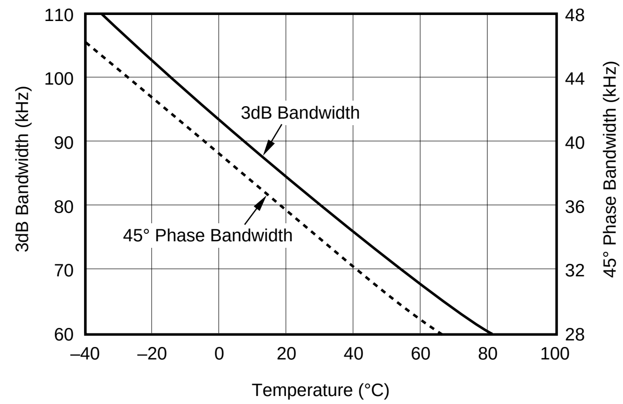
ORDERING INFORMATION

MODEL	PACKAGE	GAIN ERROR (MAX)
ISO130P	8-Pin Plastic DIP	±5% (mean value = 8.00)
ISO130PB	8-Pin Plastic DIP	±1% (mean value = 7.93)
ISO130U	8-Pin Gull-Wing Plastic Surface Mount	±5% (mean value = 8.00)
ISO130UB	8-Pin Gull-Wing Plastic Surface Mount	±1% (mean value = 7.93)

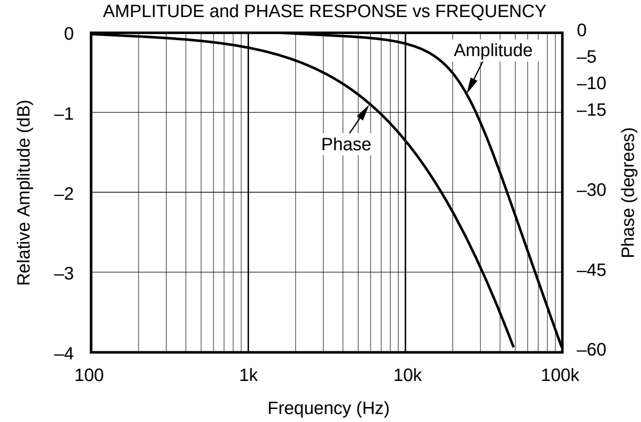
TYPICAL PERFORMANCE CURVES

At T_A = 25°C, V_{S1}, V_{S2} = 5.0V_{DC}, V_{IN}+, V_{IN}– = 0V unless otherwise noted.

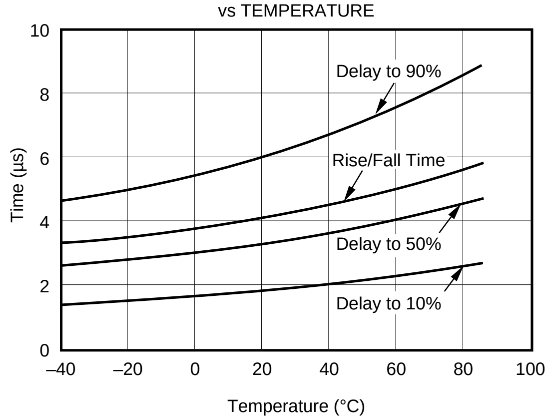
BANDWIDTH vs TEMPERATURE



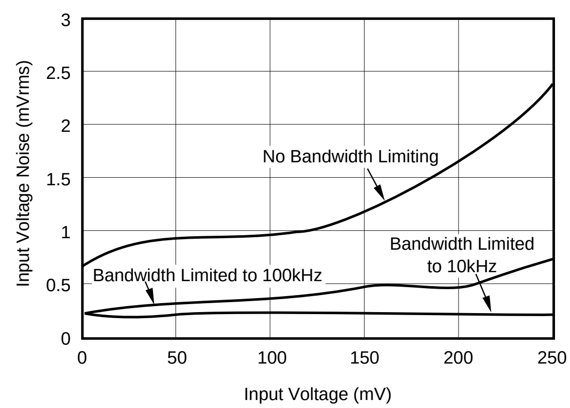
AMPLITUDE and PHASE RESPONSE vs FREQUENCY



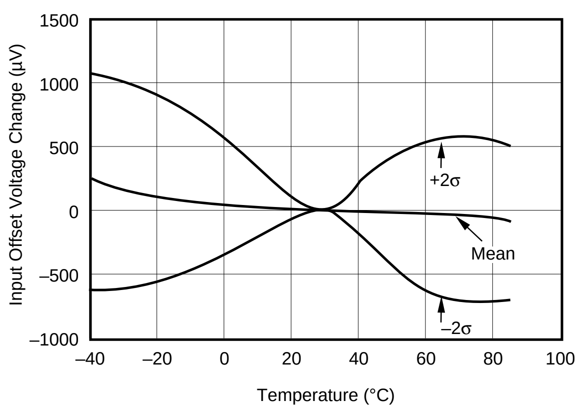
PROPAGATION DELAYS and RISE/FALL TIME vs TEMPERATURE



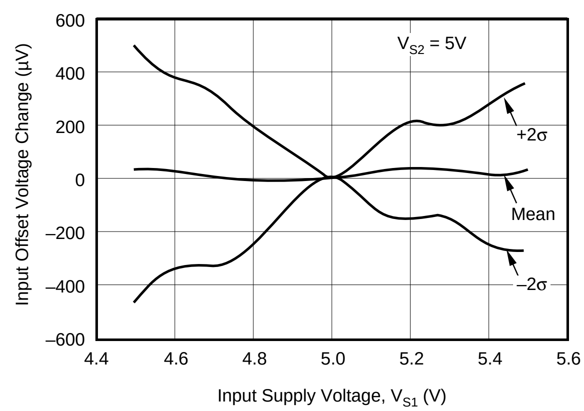
INPUT VOLTAGE NOISE vs INPUT VOLTAGE



INPUT OFFSET VOLTAGE CHANGE vs TEMPERATURE



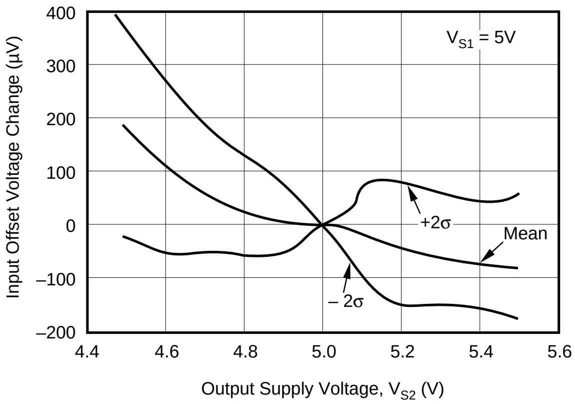
INPUT OFFSET VOLTAGE CHANGE vs INPUT SUPPLY VOLTAGE



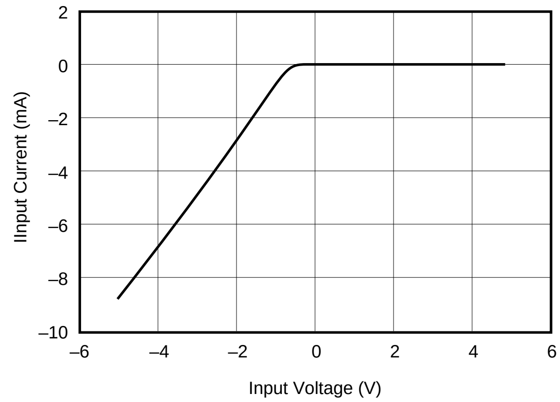
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = 25°C$, V_{S1}, $V_{S2} = 5.0V_{DC}$, $V_{IN}+$, $V_{IN}- = 0V$ unless otherwise noted.

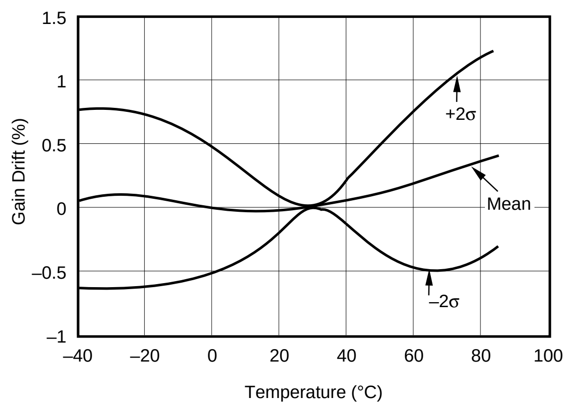
INPUT OFFSET VOLTAGE CHANGE vs OUTPUT SUPPLY VOLTAGE



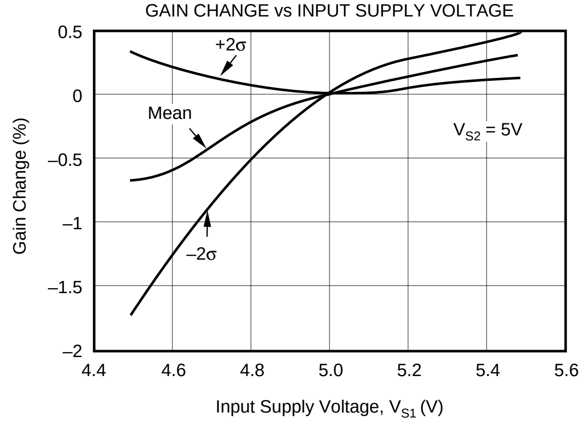
INPUT CURRENT vs INPUT VOLTAGE



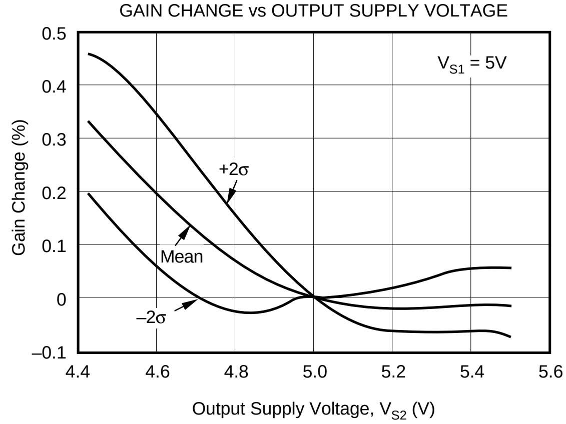
GAIN DRIFT vs TEMPERATURE



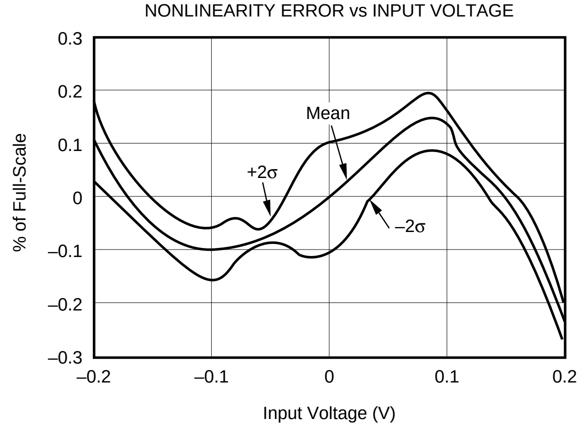
GAIN CHANGE vs INPUT SUPPLY VOLTAGE



GAIN CHANGE vs OUTPUT SUPPLY VOLTAGE



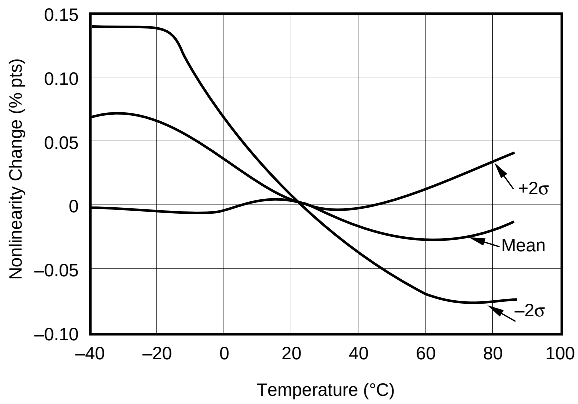
NONLINEARITY ERROR vs INPUT VOLTAGE



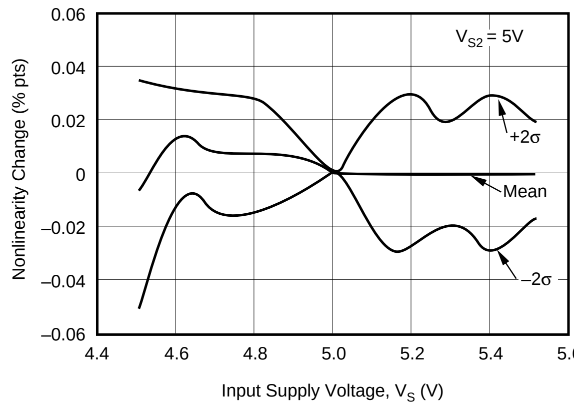
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = 25°C, V_{S1}, V_{S2} = 5.0V_{DC}, V_{IN}+, V_{IN}– = 0V unless otherwise noted.

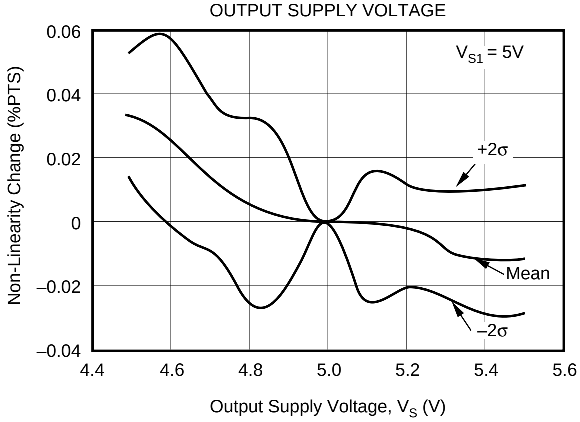
NONLINEARITY CHANGE vs TEMPERATURE



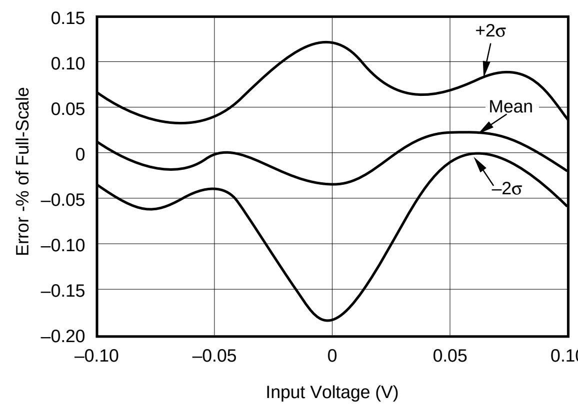
NONLINEARITY CHANGE vs INPUT SUPPLY VOLTAGE



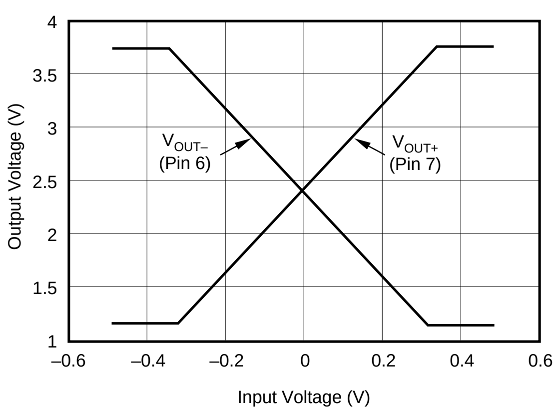
NONLINEARITY CHANGE vs OUTPUT SUPPLY VOLTAGE



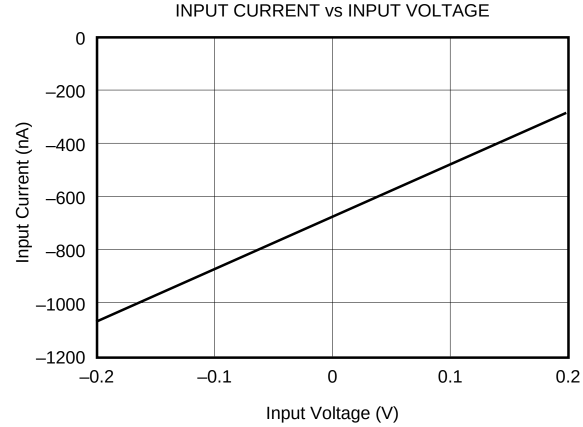
NONLINEARITY ERROR vs INPUT VOLTAGE



OUTPUT VOLTAGE vs INPUT VOLTAGE



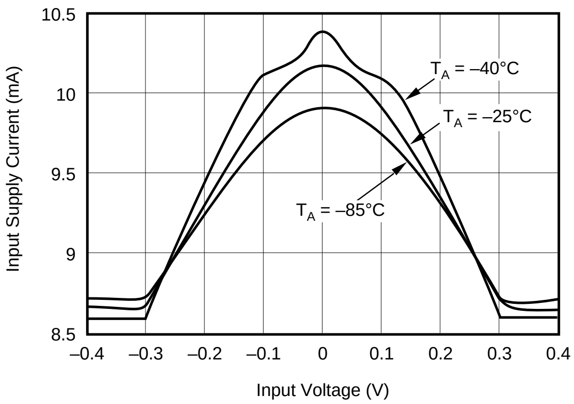
INPUT CURRENT vs INPUT VOLTAGE



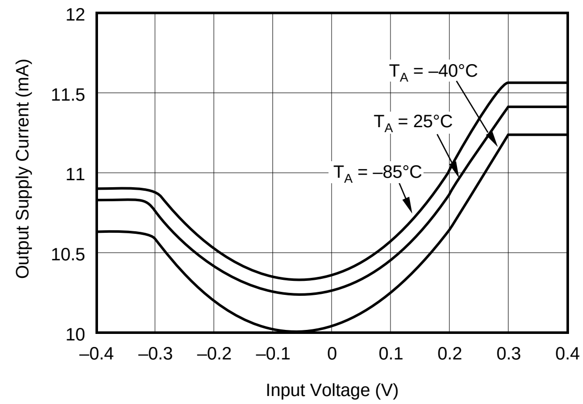
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = 25°C, V_{S1}, V_{S2} = 5.0V_{DC}, V_{IN}+, V_{IN}– = 0V unless otherwise noted.

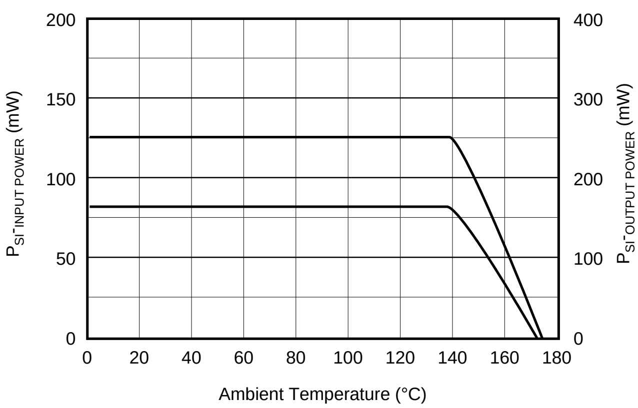
INPUT SUPPLY CURRENT vs INPUT VOLTAGE



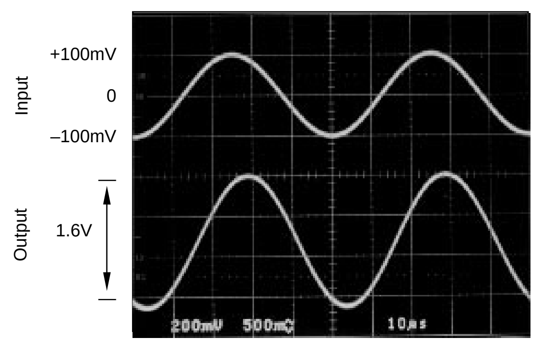
OUTPUT SUPPLY CURRENT vs INPUT VOLTAGE



DEPENDENCE OF SAFETY-LIMITING PARAMETERS ON AMBIENT TEMPERATURE

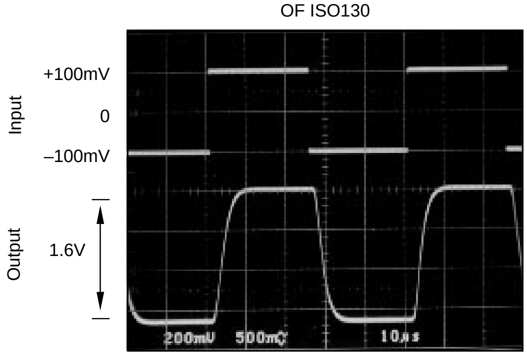


LARGE SIGNAL SINUSOIDAL RESPONSE OF ISO130



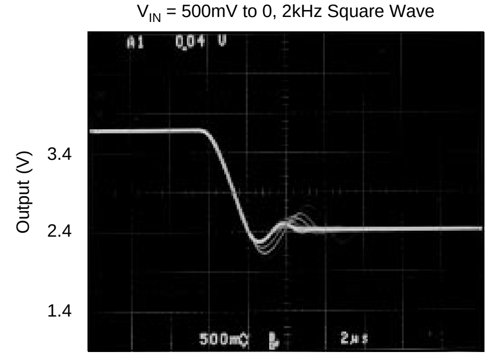
10µs/div

LARGE SIGNAL SQUARE WAVE RESPONSE OF ISO130



10µs/div

OVERLOAD RECOVERY OF ISO130
V_{IN} = 500mV to 0, 2kHz Square Wave



2µs/div

THEORY OF OPERATION

The ISO130 isolation amplifier (Figure 1) uses an input and output section galvanically isolated by a high speed optical barrier built into the plastic package. The input signal is converted to a time averaged serial bit stream by use of a sigma-delta analog-to-digital converter and then optically transmitted digitally across the isolation barrier. The output section receives the digital signal and converts it to an analog voltage, which is then filtered to produce the final output signal.

Internal amplifiers are chopper-stabilized to help maintain device accuracy over time and temperature. The encoder circuit eliminates the effects of pulse-width distortion of the optically transmitted data by generating one pulse for every edge of the converter data to be transmitted. This coding scheme reduces the effects of the non-ideal characteristics of the LED, such as non-linearity and drift over time and temperature.

ISOLATION AND INSULATION SPECIFICATIONS

The performance of the isolation barrier of the ISO130 is specified with three specifications, two of which require high voltage testing. In accordance with UL1577, the barrier integrity of each isolation amplifier is proof-tested by applying an insulation test voltage greater than or equal to 4500Vrms for one second. This is to guarantee the isolation amplifier will survive a 3750V transient voltage. The barrier leakage current test limit is 5µA. Pins 1-4 are shorted together and pins 5-8 are shorted together during the test.

This test is followed by the partial discharge isolation voltage test as specified in the German VDE0884. This method requires the measurement of small current pulses (<5pico Colomb) while applying 960Vrms across every ISO130 isolation barrier. This guarantees 600Vrms continuous isolation (V_{ISO}) voltage. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 x 600Vrms) protection without damage to the ISO130.

This test method represents “state of the art” for nondestructive high voltage reliability testing. It is based on the effects of nonuniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01 to 0.1µs current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the “inception voltage”. Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the “extinction voltage”.

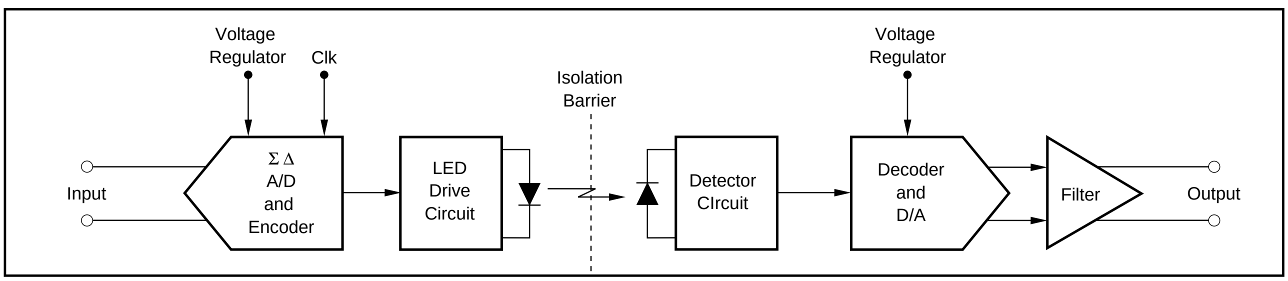


FIGURE 1. Block Diagram of ISO130 Isolation Amplifier.

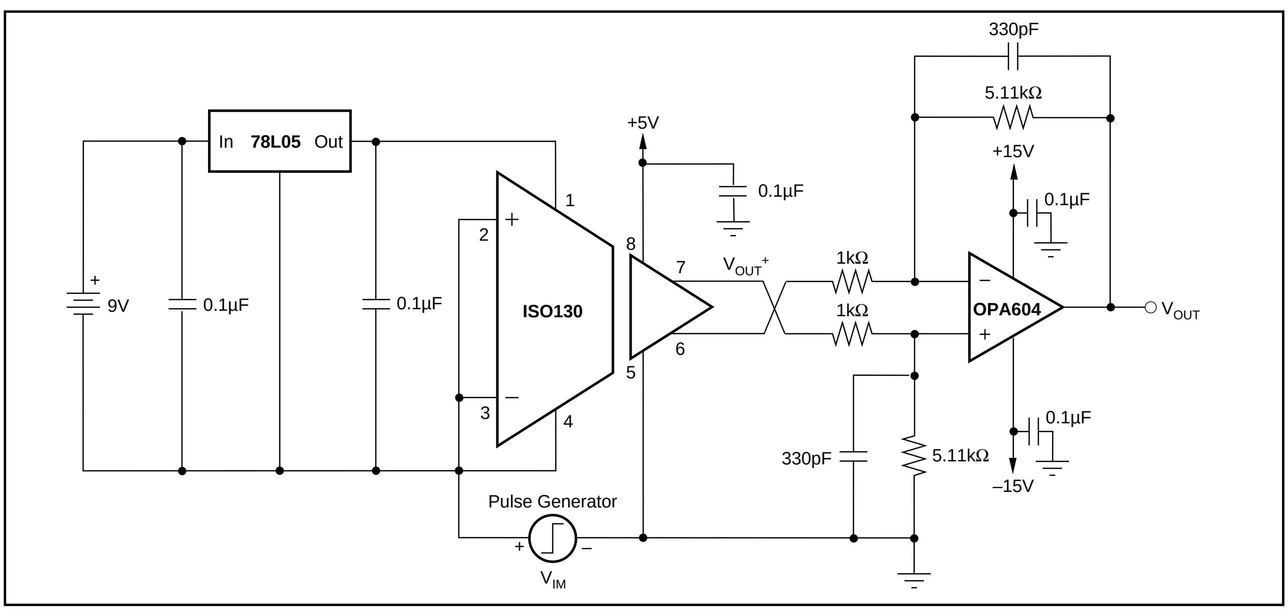


FIGURE 2. Isolation Mode Rejection and Transient Immunity Test Circuit.

Both tests are 100% production tests. The partial discharge testing of the ISO130 is performed after the UL1577 test criterion giving more confidence in the barrier reliability.

The third guaranteed isolation specification for the ISO130 is Transient Immunity (TI), which specifies the minimum rate of rise or fall of an isolation mode noise signal at which small output perturbations begin to occur. An isolation mode signal is defined as a signal appearing between the isolated grounds, GND_1 and GND_2. Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds. Under certain circumstances this voltage across the isolation barrier can induce errors at the output of the isolation amplifier. Figure 2 shows the Transient Immunity Test Circuit for the ISO130. In this test circuit a pulse generator is placed between the isolated grounds (GND_1 and GND_2). The inputs of the ISO130 are both tied to GND_1. A difference amplifier is used to gain the output signal of the ISO130. A Transient Immunity failure is determined when the output of the ISO130 changes by more than 50mV as illustrated in Figure 3.

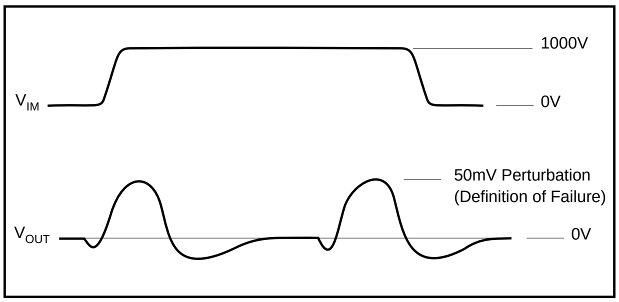


FIGURE 3. Typical Transient Immunity Failure Waveform.

Finally, Isolation Mode Rejection Ratio (typically >140dB for the ISO130) is defined as the ratio of differential signal gain to the isolation mode gain at 60Hz. The magnitude of the 60Hz voltage across the isolation barrier during this test is not so large as to cause Transient Immunity errors. The Isolation Mode Rejection Ratio should not be confused with the Common Mode Rejection Ratio. The Common Mode Rejection Ratio defines the relationship of differential signal gain (signal applied differentially between pins 2 and 3) to the common mode gain (input pins tied together and the signal applied to both inputs at the same time).

APPLICATIONS INFORMATION

APPLICATION CIRCUITS

Figure 4 illustrates a typical application for the ISO130. In this motor control circuit, the current that is sent to the motor is sensed by the resistor, R_{SENSE}. The voltage drop across this resistor is gained up by the ISO130 and then transmitted across the isolation barrier. A difference amplifier, A_2, is used to change the differential output signal of the ISO130 to a single ended signal. This voltage information is then sent to the control circuitry of the motor. The ISO130 is particularly well suited for this application because of its superior Transient Immunity (10kV/µs, max) and its excellent immunity to RF noise.

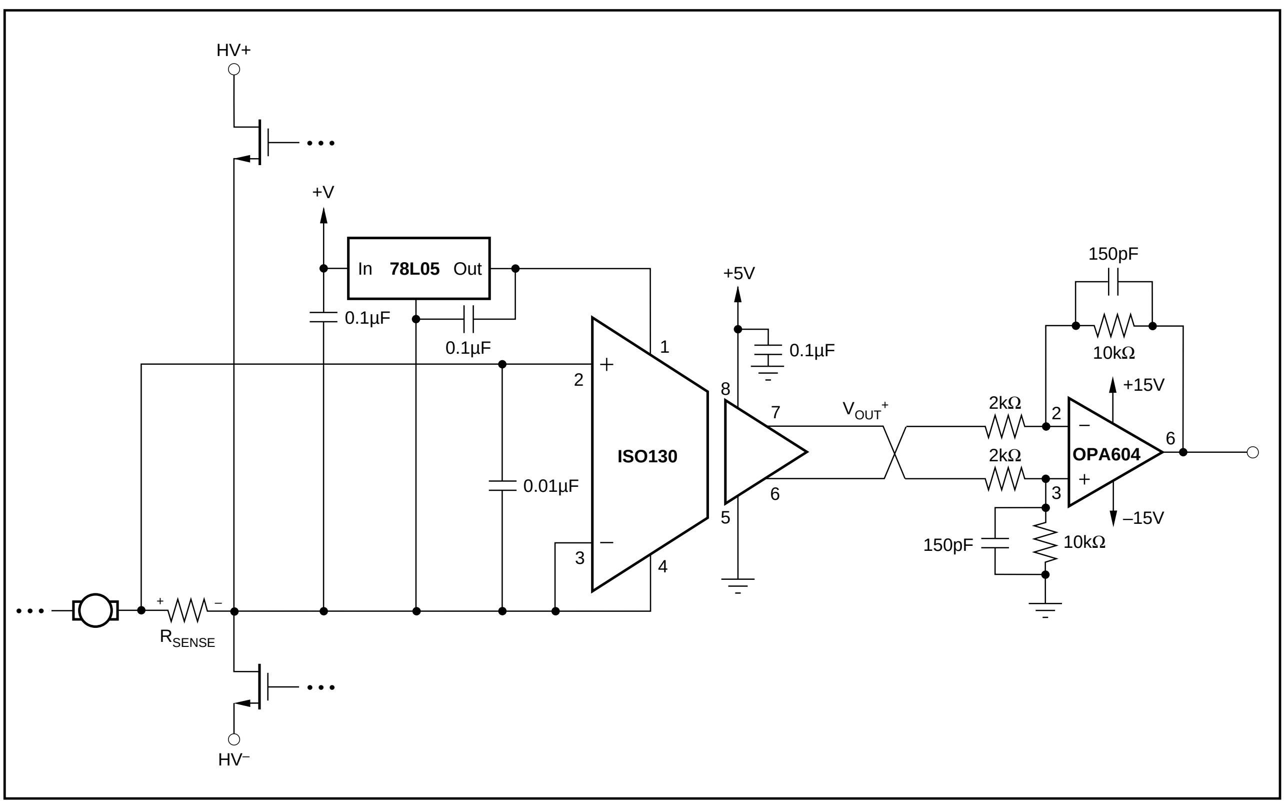


FIGURE 4. ISO130 Used to Monitor Motor Current.

The current-sensing resistor should have a relatively low value of resistance (to minimize power dissipation), a fairly low inductance (to accurately reflect high-frequency signal components), and a reasonably tight tolerance (to maintain overall circuit accuracy).

LAYOUT SUGGESTIONS

1. Bypass capacitors should be located as close as possible to the input and output power supply pins.
2. In some applications, offset voltage can be reduced by placing a 0.01µF capacitor from pin 2 and/or pin 3 to GND_1. This noise can be caused by the combination of long input leads and the switched-capacitor nature of the input circuit. This capacitor(s) should be placed as close to the isolation amplifier as possible.
3. The trace lengths at input should be kept short or a twisted wire pair should be used to minimize EMI and inductance effects. For optimum performance, the input signal should be as close to the input pins a possible.
4. A maximum distance between the input and output sides of the isolation amplifier should be maintained in the layout in order to minimize stray capacitance. This practice will help obtain optimal Isolation Mode performance. Ground planes should not pass below the device on the PCB.
5. Care should be taken in selecting isolated power supplies or regulators. The ISO130 can be affected by changes in the power supply voltages. Carefully regulated power supplies are recommended.
6. For improved nonlinearity and nonlinearity temperature drift performance, pin 3 should be tied to GND_1 and the input voltage range of pin 2 should be less than 100mV.