DESCRIPTION

The Hyundai HY5DV651622 is a 67,108,864-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the point to point applications which require high bandwidth. HY5DV651622 is organized as 4 banks of 1,048,576x16.

HY5DV651622 offers fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the clock(falling edges of the $\overline{CLK}$), Data(DQ), Data strobes(LDQS/UDQS) and Write data masks(LDM/UDM) inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

Mode Register Set options include the length of pipeline ($\overline{CAS}$ latency of 2 / 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 2 / 4 / 8), and the burst count sequence(sequential or interleave). Because data rate is doubled through reading and writing at both rising and falling edges of the clock, 2X higher data bandwidth can be achieved than that of traditional (single data rate) Synchronous DRAM.

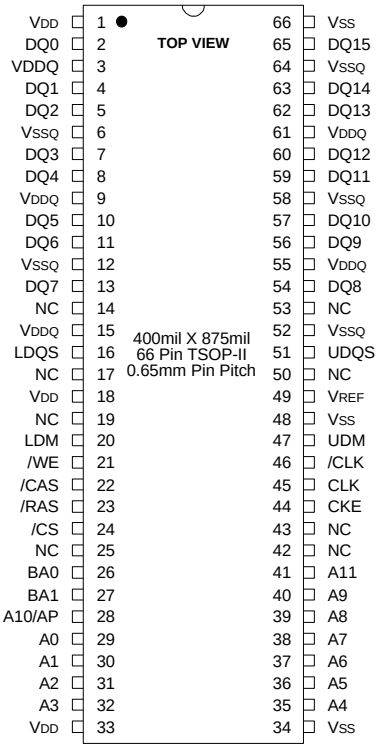
FEATURES

- 3.3V for V_{DD} and 2.5V for V_{DDQ} power supplies
- All inputs and outputs are compatible with SSTL_2 interface
- JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
- Fully differential clock operations(CLK & $\overline{CLK}$)
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Data(DQ), Data strobes(LDQS/UDQS) and Write masks(LDM/UDM) latched on both rising and falling edges of the clock
- Data outputs on LDQS/UDQS edges when read (edged DQ)
- Data inputs on LDQS/UDQS centers when write (centered DQ)
- Data strobes synchronized with output data for read and input data for write
- Delay Locked Loop(DLL) installed with DLL reset mode
- Write mask byte controls by LDM and UDM
- Programmable $\overline{CAS}$ Latency 2.0 / 3.0
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Internal 4 bank operations with single pulsed $\overline{RAS}$
- Auto refresh and self refresh supported
- 4096 refresh cycles / 64ms

ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Organization	Interface	Package
HY5DV651622T-G55	V_{DD}=3.3V V_{DDQ}=2.5V	183MHz	4Banks x 1Mbit x 16	SSTL_2	400mil 66pin TSOP II
HY5DV651622T-G6		166MHz			
HY5DV651622T-G7		143MHz			

PIN CONFIGURATION

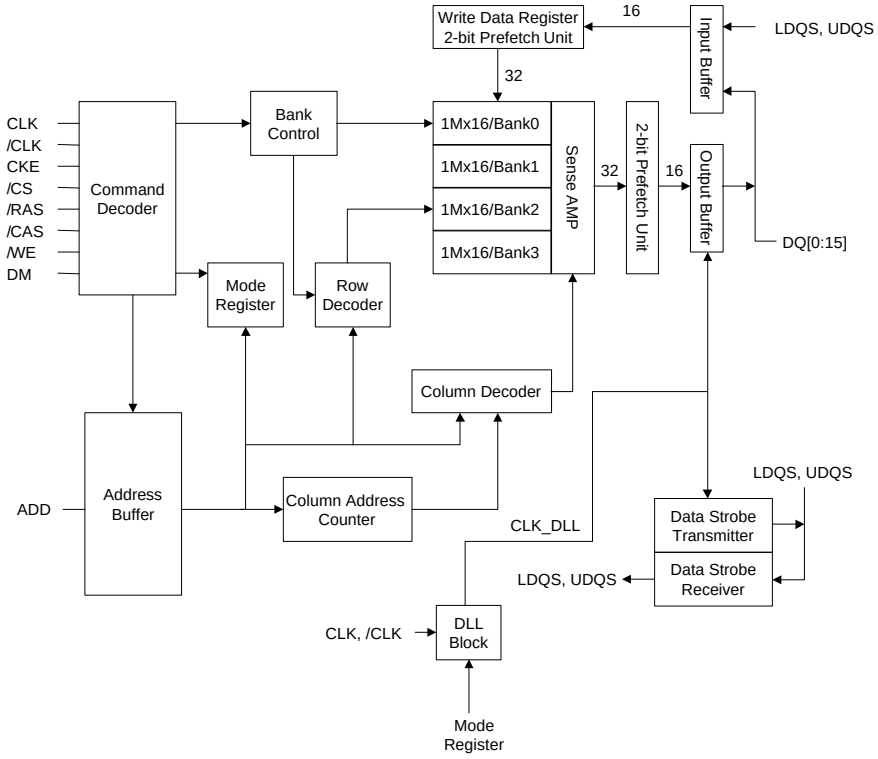


PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK, $\overline{CLK}$	Differential Clock Input	The system clock input. All of the inputs are latched on the rising edges of the clock except DQi, LDQS/UDQS and LDM/UDM that are sampled on the both.
CKE	Clock Enable	Controls internal clock signal. When deactivated, the DDR SDRAM will be one of the states among power down or self refresh.
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK/ $\overline{CLK}$, CKE, LDQS/UDQS and LDM/UDM.
BA0, BA1	Bank Select Address	Selects bank to be activated during either $\overline{RAS}$ or $\overline{CAS}$ activity. Selects bank to be read/written during either $\overline{RAS}$ or $\overline{CAS}$ activity.
A0 ~ A11	Address	Row Address : A0 ~ A11, Column Address : A0 ~ A7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the command being issued. Refer function truth table for details.
LDM, UDM	Write Mask	Masks input data in write mode.
LDQS, UDQS	Data Input/Output Strobe	Active on the both edges for Data Input and Output.
DQ0 ~ DQ15	Data Input/Output	Bidirectional data input / output pin.
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers for Noise immunity.
VREF	Reference Voltage	Reference voltage for inputs for SSTL interface.
NC	No Connection	No connection.

FUNCTIONAL BLOCK DIAGRAM

4banks x 1Mbit x 16 I/O Double data rate Synchronous DRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	×C
Storage Temperature	TSTG	-55 ~ 125	×C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD relative to VSS	VDD	-1.0 ~ 4.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature Þ Time	TSOLDER	260 Þ 10	×C Þ Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITIONS (TA=0 to 70×C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD	3.15	3.3	3.6	V	
Power Supply Voltage	VDDQ	2.3	2.5	2.7	V	1
Input High Voltage	VIH	VREF + 0.18	-	VDDQ + 0.3	V	
Input Low Voltage	VIL	-0.3	-	VREF - 0.18	V	2
Termination Voltage	VTT	VREF - 0.04	VREF	VREF + 0.04	V	
Reference Voltage	VREF	1.15	1.25	1.35	V	3

Note :
1. VDDQ must not exceed the level of V DD.
2. VIL (min) is acceptable -1.5V AC pulse width with £5ns of duration.
3. The value of VREF is approximately equal to 0.5V DDQ.

AC OPERATING TEST CONDITIONS (TA=0 to 70×C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.35	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.35	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V

AC OPERATING TEST CONDITIONS (TA=0 to 70×C, Voltage referenced to VSS = 0V) *- continued*

Parameter	Value	Unit
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	W
Series Resistor (RS)	25	W
Output Load Capacitance for Access Time Measurement (C L)	30	pF

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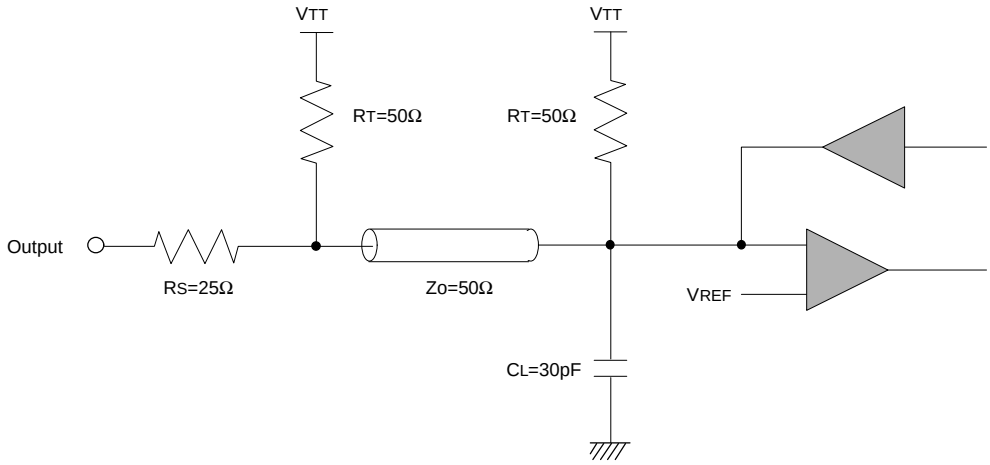
CAPACITANCE (TA=25×C, f=1MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	A0 ~ A11, BA0 ~ BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CIN	2.5	3.5	pF
Clock Capacitance	CLK, $\overline{CLK}$	CCLK	2.5	3.5	pF
Data Input / Output Capacitance	DQ0 ~ DQ15, LDQS, UDQS, LDM, UDM	CIO	4.0	5.5	pF

OUTPUT LOAD CIRCUIT



DC CHARACTERISTICS I (TA=0 to 70×C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	ILI	-5	5	mA	1
Output Leakage Current	ILO	-5	5	mA	2
Output High Voltage	VOH	VTT + 0.76	-	V	IOH = -15.2mA
Output Low Voltage	VOL	-	VTT - 0.76	V	IOL = +15.2mA

Note :
1.VIN = 0 to 3.6V, All other pins are not tested under V IN =0V
2.DOUT is disabled, VOUT=0 to 2.7V

DC CHARACTERISTICS II (TA=0 to 70×C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Test Condition		Speed			Unit	Note
				G55	G6	G7		
Operating Current	IDD1	Burst length=2, One bank active tRC Š tRC(min), IOL=0mA		160	150	140	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE £ VIL(max), tCK = min		20			mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE Š VIH(min), $\overline{CS}$ Š VIH(min), tCK = min Input signals are changed one time during 2clks		40			mA	
Active Standby Current in Power Down Mode	IDD3P	CKE £ VIL(max), tCK = min		25			mA	
Active Standby Current in Non Power Down Mode	IDD3N	CKE Š VIH(min), $\overline{CS}$ Š VIH(min), tCK = min Input signals are changed one time during 2clks		50			mA	
Burst Mode Operating Current	IDD4	tCK Š tCK(min), IOL=0mA All banks active	CL=3.0	280	260	240	mA	1
			CL=2.0	220	210	200		
Auto Refresh Current	IDD5	tRC Š tRFC(min), All banks active		210	200	190	mA	1,2
Self Refresh Current	IDD6	CKE £ 0.2V		2			mA	

Note :
1. IDD1, IDD4 and IDD5 depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of tRFC (Auto Refresh Row Cycle Time) is shown at AC CHARACTERISTICS.

AC CHARACTERISTICS

Parameter		Symbol	-G55		-G6		-G7		Unit	Note
			Min	Max	Min	Max	Min	Max		
Row Cycle Time		tRC	55	-	60	-	62	-	ns	
Auto Refresh Row Cycle Time		tRFC	66	-	72	-	77	-	ns	
Row Active Time		tRAS	38.5	120K	42	120K	42	120K	ns	
Row Address to Column Address Delay		tRCD	16.5	-	18	-	20	-	ns	
Row Prechage Time		tRP	16.5	-	18	-	20	-	ns	
Row Active to Row Active Delay		tRRD	2	-	2	-	2	-	CLK	
Column Address to Column Address Delay		tCCD	1	-	1	-	1	-	CLK	
Write Recovery Time		tWR	2	-	2	-	2	-	CLK	
Last Data-In to Read Command delay		tDRL	1	-	1	-	1	-	CLK	
Auto Precharge Write Recovery + Precharge Time		tDAL	27.5	-	30	-	34	-	ns	
System Clock Cycle Time	CL = 3.0	tCK	5.5	12	6	15	7	15	ns	
	CL = 2.0		-	-	-	-	-	-	ns	
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	CLK	
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	CLK	
DQS-Out edge to Clock edge skew		tDQSCK	-0.4	0.1	-0.4	0.1	-0.4	0.1	CLK	
Data-Out edge to Clock edge skew		tAC	-0.4	0.1	-0.4	0.1	-0.4	0.1	CLK	
DQS-Out edge to Data-Out edge skew		tDQSQ	-0.4	0.4	-0.4	0.4	-0.5	0.5	ns	
Data/DQS-Out Valid Window		tDV	0.35	-	0.35	-	0.35	-	CLK	
DQS-Out Preamble Time		tRPRE	0.8	1.1	0.8	1.1	0.8	1.1	CLK	
DQS-Out Postamble Time		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
CLK to first rising edge of DQS-In		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	CLK	
DQS-In Preamble Setup Time		tWPRES	0	-	0	-	0	-	CLK	
DQS-In Preamble Hold Time		tWPREH	0.25	-	0.25	-	0.25	-	CLK	
DQS-In Last falling edge to Hi-Z Delay		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
DQS-In High Level Width		tDSH	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
DQS-In Low Level Width		tDSL	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Input Setup Time to CLK (ADDR & Control)		tIS	1.1	-	1.1	-	1.1	-	ns	1
Input Hold Time to CLK (ADDR & Control)		tIH	1.1	-	1.1	-	1.1	-	ns	1
Data-In Setup Time to DQS-In (DQ & DM)		tDS	0.5	-	0.5	-	0.5	-	ns	2
Data-In Hold Time to DQS-In (DQ & DM)		tDH	0.5	-	0.5	-	0.5	-	ns	2
DQS-In Pulse Width		tDIPW	1.6	-	1.6	-	1.7	-	ns	
Mode register Set Cycle Time		tMRD	2	-	2	-	2	-	CLK	
Power Down Exit Time		tPDEX	10	-	10	-	10	-	ns	
Exit Self Refresh to Non-Read Command		tXSNR	66	-	72	-	75	-	ns	
Exit Self Refresh to Read command		tXSRD	200	-	200	-	200	-	CLK	3
Average Periodic Refresh Interval		tREFI	-	15.6	-	15.6	-	15.6	us	

Note :

1. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
2. Data letched at both rising and falling edges of Data Strobes(LDQS/UDQS) : DQ, LDM/UDM.
3. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.

SIMPLIFIED COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	A10/AP	BA	Note
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3,6
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4,6
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode (Clock Suspend)	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Dont Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

1. LDM/UDM states are "Dont Care". Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A_0~A_{11} and BA_0~BA_1 used for Mode Registering duing Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+t_{RP}).
4. If a Write with Autoprecharge command is detected by memory compoment in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+1+t_{DPL}+t_{RP}). Last Data-In to Prechage delay(t_{DPL}) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If A_{10}/AP is "High" when Row Precharge command being issued, BA_0/BA_1 are ignored and all banks are selected to be precharged.
6. The speed grade with G code will not be guaranteed the Read and Write with Autoprecharge function.

WRITE MASK TRUTH TABLE

Function	CKEn-1	CKEn	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	LDM	UDM	ADDR	A10/ AP	BA	Note
Data Write	H	X	X	L	L	X			1,2
Data-In Mask	H	X	X	H	H	X			1,2
Lower Byte Write / Upper Byte-In Mask	H	X	X	L	H	X			1,2
Upper Byte Write / Lower Byte-In Mask	H	X	X	H	L	X			1,2

(H=Logic High Level, L=Logic Low Level, X=Dont Care)

Note :

1. Write Mask command masks burst write data with reference to LDQS/UDQS(Data Strobes) and it is not related with read data.
2. In case of x16 data I/O, LDM and UDM control lower byte(DQ0~7) and Upper byte(DQ8~15) respectively.

PACKAGE INFORMATION

400mil 66pin Thin Small Outline Package