DALLAS SEMICONDUCTOR

DS1612
Lithium Battery Monitor

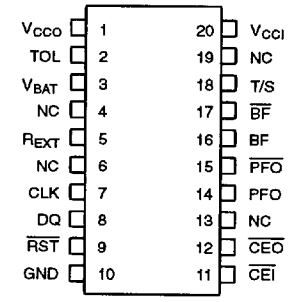
FEATURES

- Programmable battery monitor tracks voltage of a lithium cell and provides advanced warning of an impending battery failure
- Measurement technique 1 monitors $-\Delta V/\Delta T$, with programmable voltage delta and programmable time interval for test
- Measurement technique 2 monitors voltage while powering a test load. Triggered via test strobe input or programmable timer
- Both active high and active low battery fail indicators provided
- Voltage trip point settings are nonvolatile in the absence of V_{CC}
- Voltage trip points are set and read through a 3–wire interface (CLK, DQ, $\overline{RST}$)
- Converts CMOS RAM into nonvolatile memory
- Unconditionally write protects when V_{CC} is out of tolerance
- Power fail signals can be used to interrupt processor on power failure
- Automatically switches to battery backup supply when power fail occurs
- Optional 5% or 10% power fail detection
- Optional industrial temperature range of –40°C to +85°C.

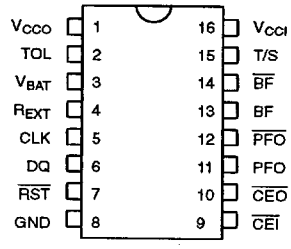
DESCRIPTION

The DS1612 Lithium Battery Monitor performs three vital backup power supply monitoring functions. The first function is to continuously monitor the decay in a lithium cell's no load voltage over time. As a lithium cell approaches the end of its life, its voltage decay begins to accelerate. Early in this acceleration process, the DS1612 can predict using $-\Delta V/\Delta T$ monitoring techniques that the lithium battery is close to its end of life and activate battery fail signals so that the backup lithium supply may be replaced before it fails.

PIN ASSIGNMENT



20–PIN TSSOP



16–PIN DIP, SOIC

PIN DESCRIPTION

V_{BAT}	–	Backup Battery Input
V_{CCI}	–	+5V Supply
BF, $\overline{BF}$	–	Battery Fail Outputs
CLK	–	Serial Port Clock Input
DQ	–	Serial Port Data Input
$\overline{RST}$	–	Serial Port Reset Input
V_{CCO}	–	RAM Supply
PFO, $\overline{PFO}$	–	Power Fail Outputs
T/S	–	Test Strobe Input
NC	–	No Connect
TOL	–	V_{CC} Tolerance Select
R_{EXT}*	–	External Resistance (Optional)
GND	–	Ground
$\overline{CEI}$	–	Chip Enable Input
$\overline{CEO}$	–	Chip Enable Output

*Either this pin or an external resistor must be grounded.

The second monitoring function which the DS1612 supplies is monitoring the absolute voltage of a backup lithium supply under unloaded and loaded conditions. While the open circuit voltage of a backup lithium source may remain relatively constant over time, the cell's ability to effectively back a constant load will gradually degrade. The DS1612 can be used to periodically test the battery voltage as it powers a known test load and indicate, through its battery fail outputs, if the battery voltage drops too far to support an actual system load.

The third function performed by the DS1612 is monitoring the incoming power supply for an out–of–tolerance condition and converting SRAM into nonvolatile memory. When such a condition is detected, chip enable is inhibited to accomplish write protection and the backup lithium supply is switched in to supply the SRAM with uninterrupted power.

TABLE 1

BATTERY TEST	T/S STATUS	L/$\overline{U}$ BIT	TIME–OUT REGISTER
$-\Delta V/\Delta T$	not transitioning	X	X
Unloaded Absolute Trip Point (External)	rising edge	0	X
Unloaded Absolute Trip Point (Internal)	not transitioning	0	1–255
Loaded Absolute Trip Point (External)	rising edge	1	X
Loaded Absolute Trip Point (Internal)	not transitioning	1	1–255

$-\Delta V/\Delta T$ MEASUREMENT

This battery measurement mode is active when the ΔT register contains a nonzero value and no absolute voltage measurement is in progress. At the start of $-\Delta V/\Delta T$ measurement, the value in the ΔT register is loaded into a an auto-decrementing timer. When this timer reaches zero, it is re-initialized and another voltage sample is taken. For any new sample taken, if the voltage difference between the new sample and the previous sample is greater than or equal to the voltage indicated in the $-\Delta V$ register, the BF and $\overline{BF}$ outputs are asserted to indicate impending battery failure. These outputs can only be reset by asserting the $\overline{RBF}$ bit in the Command Word (see below) or by replacing the battery connected to V_{BAT}.

ABSOLUTE VOLTAGE MEASUREMENT

An absolute voltage measurement (AVM) can be triggered manually on the rising edge of the Test Strobe pin (T/S)_ or automatically by loading a timeout duration into the Load Timeout register. If automatic measurement is active, a measurement can still be initiated by the T/S pin at any time without affecting the automatic measurements or the timeout duration between them.

On the rising edge of T/S or the expiration of a timeout period, the DS1612 connects V_{BAT} to (1) a 750 ohm test load, (2) a 750 ohm test load in series with an external load, or (3) no load. This loading is maintained for a period of one second, during which BF and $\overline{BF}$ are connected to the AVM circuitry instead of the $-\Delta V/\Delta T$ circuitry. During this one second period, if V_{BAT} falls below the trip point stored in the V_{TP} Register, BF and $\overline{BF}$ are asserted. After this period is over, BF and $\overline{BF}$ are reconnected to the $-\Delta V/\Delta T$ circuitry regardless of the status of T/S. If BF and $\overline{BF}$ were asserted by the absolute voltage measurement, they will not be reset until the $\overline{RBF}$ bit in the Command Word is asserted or the battery is replaced. Another AVM cannot occur until the next rising edge of the T/S pin or the expiration of the next timeout period.

To perform the absolute voltage measurement using a load, the Loaded/Unloaded (L/$\overline{U}$) bit in the V_{TP} register must be set (see Register Structure below). With the L/$\overline{U}$ bit set and R_{EXT} pin grounded, the internal 750 ohm resistor serves as the load during this measurement. With the L/$\overline{U}$ bit set and R_{EXT} connected through an external resistor R to ground, the load during this test will be 750

+ R ohms. To perform the absolute voltage measurment with no load, the L/$\overline{U}$ bit must be cleared.

NOTE:
R_{EXT} must be grounded or connected through an external resistor to ground.

USING BOTH MEASUREMENT TECHNIQUES

The $-\Delta V/\Delta T$ and AVM techniques can be active simultaneously on the DS1612 with no worries about relative timing. In the event that T/S is asserted at the end of a ΔT period (which is when $-\Delta V/\Delta T$ measurements are taken), the DS1612 performs the $-\Delta V/\Delta T$ measurement first and immediately proceeds to the AVM measurement. Likewise, in the event that the ΔT register and the Load Timeout register contain the same durations and call for their measurements at the same periodic instants in time, the DS1612 always schedules the $-\Delta V/\Delta T$ measurement first and immediately proceeds to the AVM measurement.

READ AND WRITE ACCESS

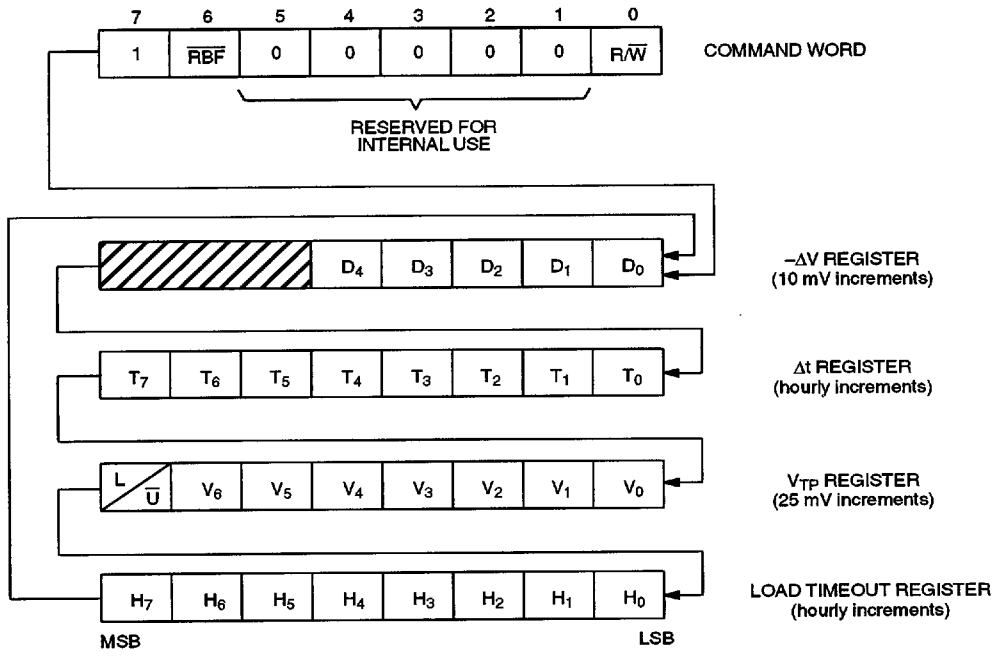
Communication with the DS1612 occurs over a 3–wire serial interface consisting of a bi-directional data line (DQ), a clock strobe (CLK) and an active-low reset signal ($\overline{RST}$). Data transfers begin by deasserting $\overline{RST}$. Then an 8-bit protocol called the Command Word is strobed into the device LSB first, with each bit set up to be strobed in on the rising edge of CLK. Following the Control Word, data can be written into or read from the device. For writes, data is again set up to be strobed in on the rising edge of CLK. For reads, the DS1612 will produce valid data a short time after the falling edge of CLK; this data should be latched by the external system on the rising edge of CLK. Assertion of $\overline{RST}$ will terminate the current transfer and put DQ into a high-impedance state.

THE COMMAND WORD

Bit 7 of the Command Word is reserved must be logic 1. Bit 6 ($\overline{RBF}$) is active-low; when it is asserted, the BF and $\overline{BF}$ outputs are reset. Please note that the deassertion of these two outputs does not actually take place until after the $\overline{RST}$ pin is deasserted to end the current transfer. Bits 5, 4, 3, 2, and 1 are reserved and must be logic 0. Bit 0 (R/$\overline{W}$) controls whether subsequent CLK cycles will strobe data into the DS1612 registers (logic 0) or read data out of the registers (logic 1).

Read and write operations both start with bit 0 of the $-\Delta V$ register, continue through bit 7 of the load timeout register and wrap around continuously until $\overline{RST}$ is asserted. Following a write, $\overline{RST}$ must be asserted for t_{CEH} to ensure completion of the cycle. If the only desired operation is to assert the $\overline{RBF}$ bit, $\overline{RST}$ can be asserted after $\overline{RBF}$ has beed strobed in.

COMMAND WORD AND REGISTER STRUCTURE



REGISTER STRUCTURE

The –ΔV register is a bytewide register storing a 5–bit value which specifies the voltage drop at which successive V_{BAT} samples will trigger the BF and $\overline{BF}$ outputs during –ΔV/ΔT testing. The three most significant bits of this register are reserved for internal use. During read transfers they are shifted out as logic 0. During write transfers, these bits will be ignored. The voltage drop value is stored in increments of 10 mV, with values of 00000–11111 corresponding to 10–320 mV.

The ΔT register is a bytewide register, storing an 8–bit value which specifies the time interval between successive battery voltage samples during –ΔV/ΔT testing. This time value is stored in hourly increments, from 1–255 hours. A value of 0 in the ΔT register disables the –ΔV/ΔT measurement system.

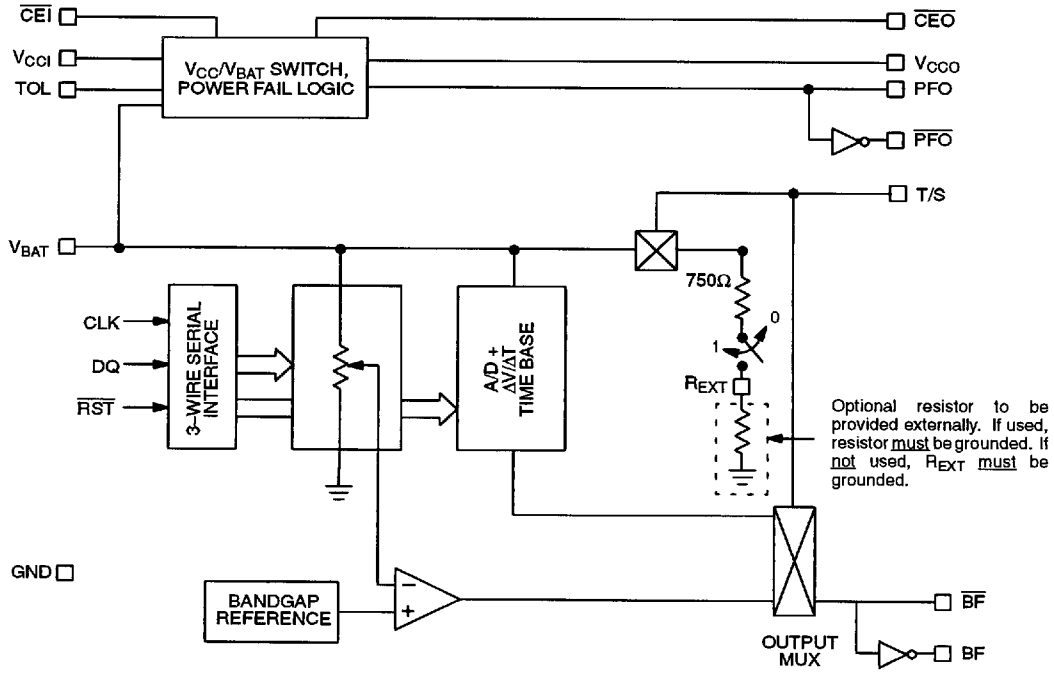
The V_{TP} register is a bytewide register, storing a 7–bit value which specifies the battery voltage at which the monitor will activate the BF and $\overline{BF}$ output signals during an absolute trip point test. The MSB of the V_{TP} register (L/$\overline{U}$) determines whether a loaded or unloaded absolute trip point test will be performed. A logic 0 specifies an unloaded test while a logic 1 specifies a loaded test is to be conducted. The V_{TP} register records in 25 mV increments and starts at 2.0 volts. The desired trip point is computed as 2.0V + (25 mV *V_{TP}). For example, a value of 0010100 indicates an unloaded test will be performed and compared against a 2.5 trip point, 2.0V + (25 mV * 20).

The time–out register is a bytewide register, storing an 8–bit value which specifies the time interval between successive battery voltage samples during an absolute trip point test. This time value is stored in hourly increments, from 1–255 hours. A value of 0 in the time–out register disables the periodic test function. A disabled periodic test function does not affect the T/S input, that is, T/S may still be asserted to perform an absolute trip point test at any time on demand, regardless of the status of the periodic test. This register is set to 0 when shipped from the factory.

POWER SUPPLY MONITORING AND NV RAM CONTROL

The DS1612 performs the circuit functions required to battery backup a RAM. First, a switch is provided to direct power from the battery or the incoming power supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.2 volts. The second function is power fail detection and write protection. The incoming supply (V_{CCI}) is constantly monitored. When the supply goes out of tolerance a precision comparator detects power failure and inhibits the chip enable output ($\overline{CEO}$). This is accomplished by holding the chip enable output ($\overline{CEO}$) to within 0.2 volts of V_{CCO} when V_{CCI} is out of tolerance. If $\overline{CEI}$ is low at the time that power fail detection occurs, the $\overline{CEO}$ signal is kept low until $\overline{CEI}$ is brought high again. However, $\overline{CEO}$ is forced high after 1.5 µs regardless of the state of $\overline{CEI}$. The delay of write protection until the current memory cycle is complete prevents corrupted data. Power fail detection occurs in the range of 4.75 to 4.5 volts with the tolerance pin (TOL) grounded. If the tolerance pin is connected to V_{CCO}, then the power fail detection occurs in the range of 4.5 to 4.25 volts. The $\overline{PFO}$ and PFO signals are driven active and remain active until V_{CCI} returns to nominal conditions. During nominal supply conditions $\overline{CEO}$ will follow $\overline{CEI}$ with a maximum propagation delay of 5ns.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage TOL=GND	V_{CCI}	4.75	5.0	5.5	V	1
Supply Voltage TOL=V_{CCO}	V_{CCI}	4.5	5.0	5.5	V	1
Battery Supply Voltage	V_{BAT}	2.0	3.0	4.0	V	1
Logic 1 Input	V_{IH}	2.0		V_{CCI}+0.3	V	1
Logic 0 Input	V_{IL}	–0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI} = >V_{CCTP})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{CC1}		0.5	2.0	mA	2
Standby Current	I_{CC2}			150	µA	2, 6
Supply Voltage	V_{CCO}	V_{CCI}–0.2			V	1
Supply Current	I_{CCO1}			100	mA	3
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.75	V	1, 13
V_{CC} Trip Point (TOL=V_{CCO})	V_{CCTP}	4.25	4.37	4.50	V	1, 13
Output Current @ 2.4V	I_{OH}	–1.0			mA	7, 13
Output Current @ 0.4V	I_{OL}			4.0	mA	7, 13
$\overline{CEI}$ to $\overline{CEO}$ Impedance	Z_{CE}			30	Ω	4
Input Leakage	I_{IL}	–1.0		+1.0	µA	
Output Leakage	I_{LO}	–1.0		+1.0	µA	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI} < V_{BAT})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Current	I_{BAT}			100	nA	2
Battery Backup Current	I_{CCO2}			500	µA	5
Supply Voltage	V_{CCO}	V_{BAT}–0.2			V	
$\overline{CEO}$ Output	V_{OHL}	V_{BAT}–0.2			V	8

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CCI}= > V_{CCTP})

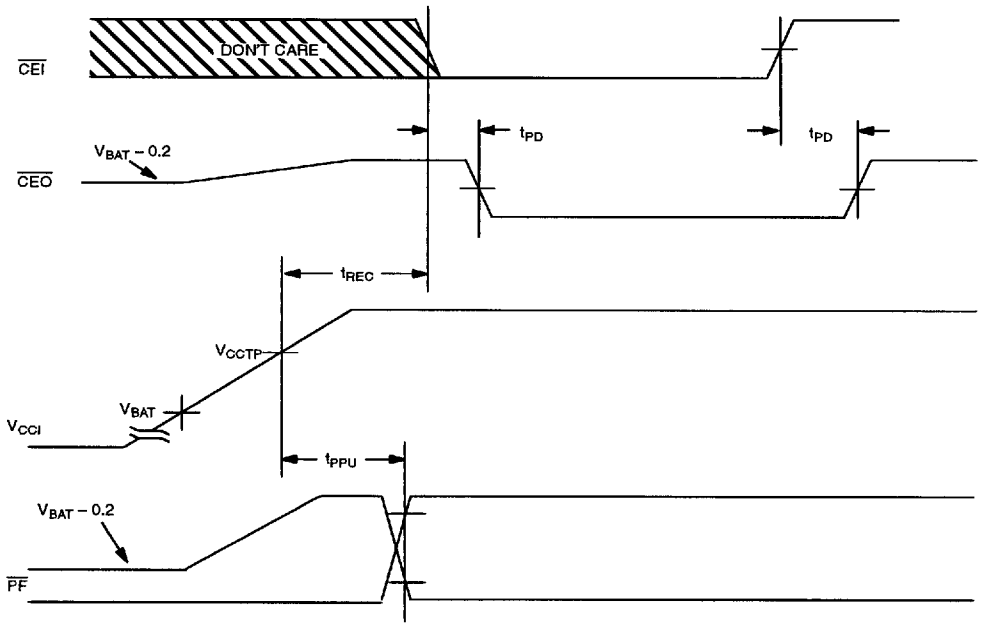
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CEI}$ to $\overline{CEO}$ Propagation Delay	t_{PD}			5	ns	7
V_{BAT} Detect to BF, $\overline{BF}$	t_{BF}			1	ms	

AC ELECTRICAL CHARACTERISTICS

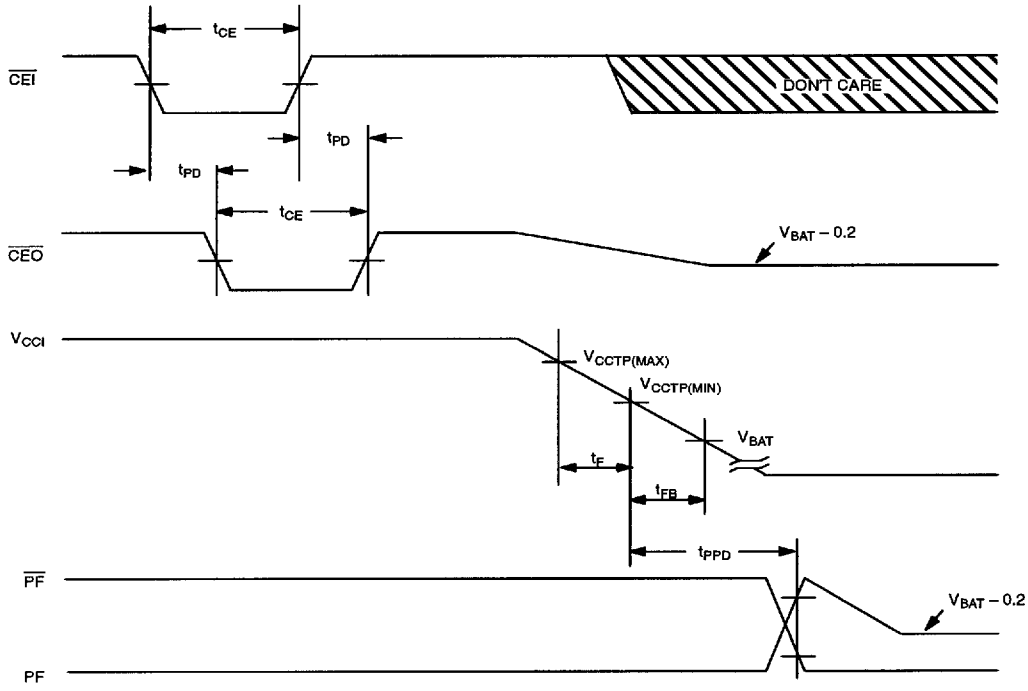
(0°C to 70°C; V_{CCI} < V_{CCTP})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	2		125	ms	12
V_{CC} Slew Rate	t_F	300			µs	
V_{CC} Slew Rate	t_{FB}	10			µs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	µs	14
V_{CC} Fail Detect to PF, $\overline{PF}$	t_{PPD}			200	µs	
V_{CC} Valid to PF, $\overline{PF}$	t_{PPU}			100	µs	

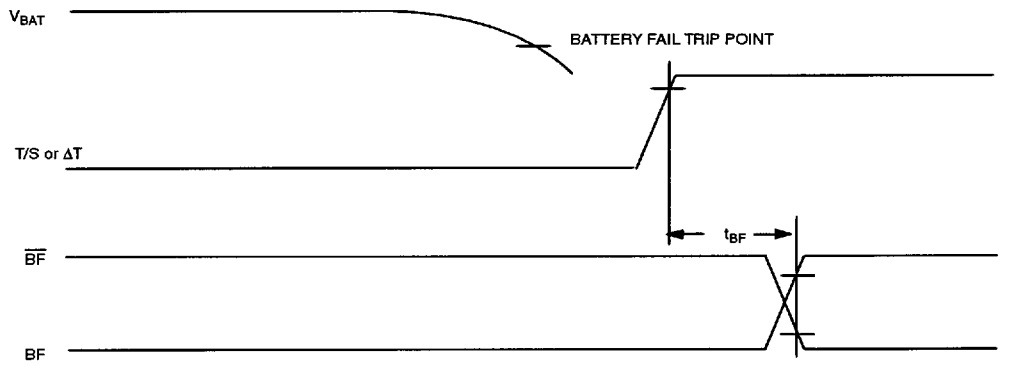
TIMING DIAGRAM: POWER UP



TIMING DIAGRAM: POWER DOWN



TIMING DIAGRAM: BATTERY FAIL DETECTION



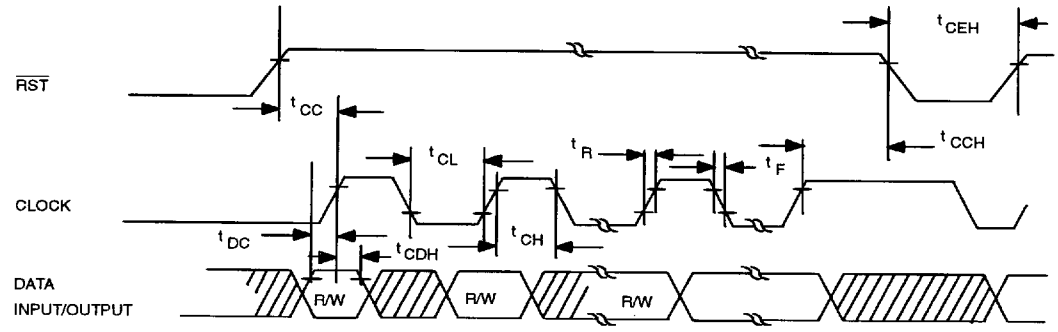
NOTE:
t_{BF} is measured from either the T/S pin being asserted or the the internal ΔT register expiring to the battery fail outputs (BF and $\overline{BF}$) going active.

3-WIRE SERIAL INTERFACE

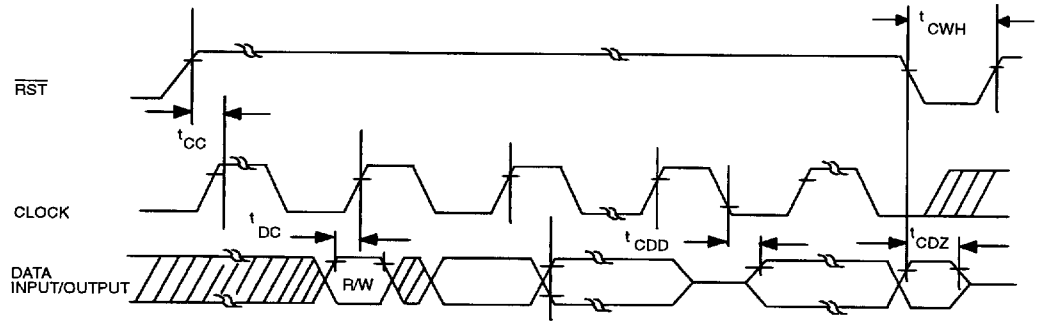
(0°C to +70°C; $V_{CCI} \geq V_{CCTP}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	9
CLK to Data Hold	t_{CDH}	40			ns	2
CLK to Data Delay	t_{CDD}			100	ns	9, 10, 11
CLK Low Time	t_{CL}	250			ns	9
CLK High Time	t_{CH}	250			ns	9
CLK Frequency	t_{CLK}	DC		2.0	MHz	9
CLK Rise & Fall	t_R, t_F			500	ns	9
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	9
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	9
$\overline{RST}$ Inactive Time	t_{CWH}	250			ns	9
RST to I/O High Z	t_{CDZ}			50	ns	9
$\overline{RST}$ Inactive Time	t_{CEH}	20			ms	9, 15

3-WIRE WRITE DATA TIMING DIAGRAM



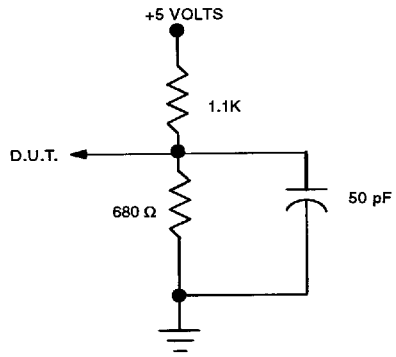
3-WIRE READ DATA TIMING DIAGRAM



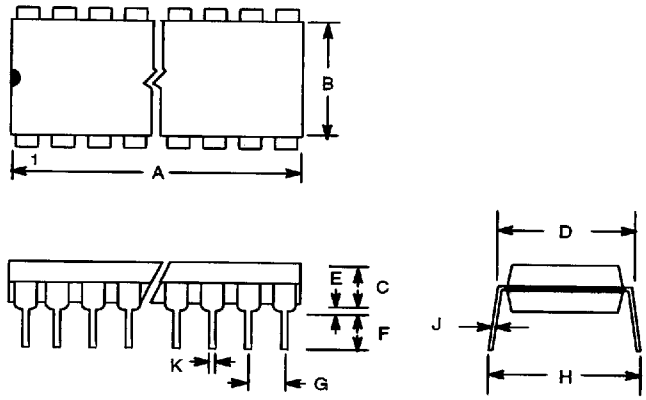
NOTES:

1. All voltages referenced to ground.
2. Measured with outputs open circuited.
3. I_{CCO1} is the maximum average load which the DS1612 can supply to the memories
4. Z_{CE} is an average input-to-output impedance as $\overline{CEI}$ is swept from ground to V_{CCI} and less than 4 mA is forced through Z_{CE}.
5. I_{CCO2} is the maximum average load current which the DS1612 can supply to the memories in the battery backup mode.
6. All inputs within 0.3V of ground or V_{CCI} and $\overline{CEI}$ within 0.3V of V_{CCI}.
7. Measured with a load as shown in Figure 1.
8. Chip Enable Output $\overline{CEO}$ can only sustain leakage current in the battery mode.
9. V_{IH}=2.0V or V_{IL}=0.8V with 10 ns minimum rise and fall time.
10. V_{OH}=2.4V and V_{OL}=0.4V.
11. Load capacitance = 50 pF.
12. $\overline{CEO}$ will be held high for a time equal to t_{REC} after V_{CCI} crosses V_{CCTP}.
13. $\overline{PF}$ and $\overline{BF}$ are open drain outputs.
14. t_{CE} maximum must be met to ensure data integrity on power down.
15. t_{CEH} must be met following a write to ensure data integrity.

OUTPUT LOAD Figure 1

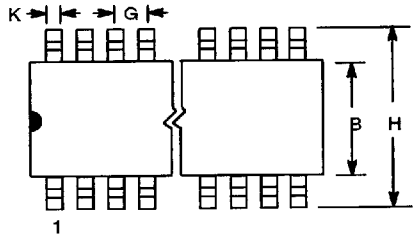


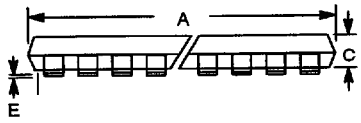
DS1612 16–PIN DIP (300 MIL)

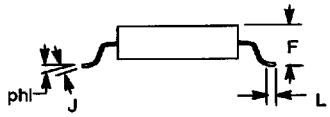


PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.740 18.80	0.780 19.81
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.29	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

DS1612 16–PIN SOIC (300 MIL)

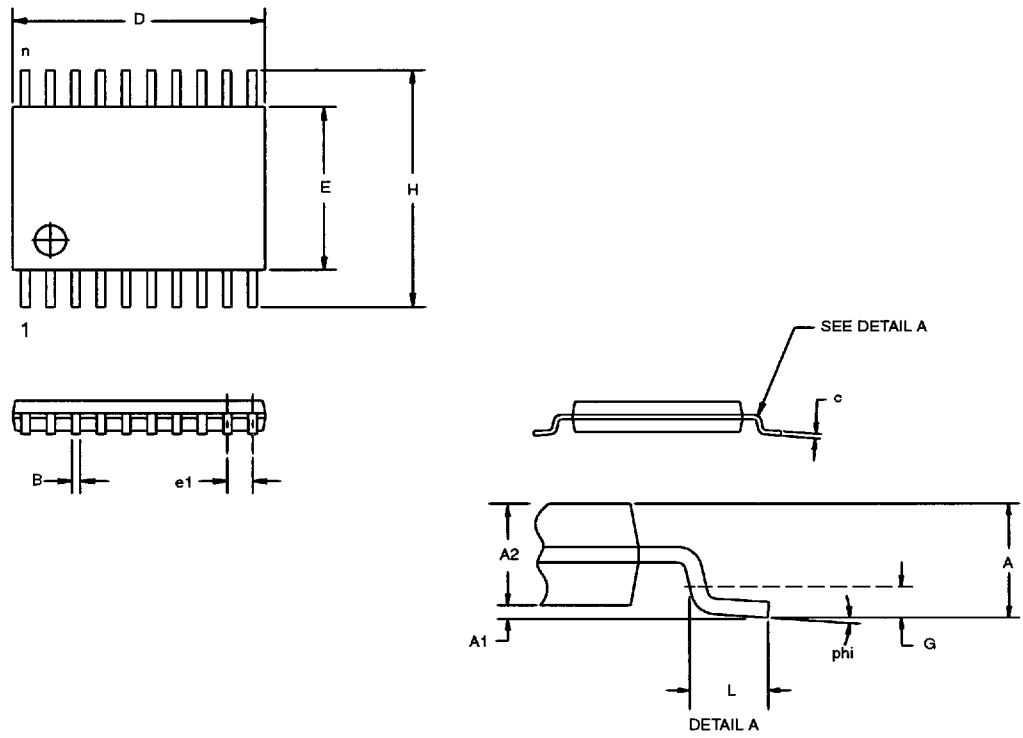






PKG	16-PIN	
DIM	MIN	MAX
A IN. MM	0.402 10.21	0.412 10.46
B IN. MM	0.290 7.37	0.300 7.65
C IN. MM	0.089 2.26	0.095 2.41
E IN. MM	0.004 0.102	0.012 0.30
F IN. MM	0.094 2.38	0.105 2.68
G IN. MM	.050 BSC 1.27 BSC	
H IN MM	0.398 10.11	0.416 10.57
J IN MM	0.009 0.229	0.013 0.33
K IN. MM	0.013 0.33	0.019 0.48
L IN MM	.016 .40	.040 1.02
PHI	0°	8°

DS1612 20-PIN TSSOP



DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°