93AA46A/B/C, 93LC46A/B/C, 93C46A/B/C

1K Microwire Compatible Serial EEPROM

Device Selection Table

Part Number	Vcc Range	ORG Pin	Word Size	Temp Ranges	Packages
93AA46A	1.8-5.5	No	8-bit	I	P, SN, ST, MS, OT
93AA46B	1.8-5-5	No	16-bit	I	P, SN, ST, MS, OT
93LC46A	2.5-5.5	No	8-bit	I, E	P, SN, ST, MS, OT
93LC46B	2.5-5.5	No	16-bit	I, E	P, SN, ST, MS, OT
93C46A	4.5-5.5	No	8-bit	I, E	P, SN, ST, MS, OT
93C46B	4.5-5.5	No	16-bit	I, E	P, SN, ST, MS, OT
93AA46C	1.8-5.5	Yes	8 or 16-bit	I	P, SN, ST, MS
93LC46C	2.5-5.5	Yes	8 or 16-bit	I, E	P, SN, ST, MS
93C46C	4.5-5.5	Yes	8 or 16-bit	I, E	P, SN, ST, MS

Features

- Low-power CMOS technology
- ORG pin to select word size for ‘46C version
- 128 x 8-bit organization ‘A’ ver. devices (no ORG)
- 64 x 16-bit organization ‘B’ ver. devices (no ORG)
- Self-timed ERASE/WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power-on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device Status signal (READY/$\overline{\text{BUSY}}$)
- Sequential READ function
- 1,000,000 E/W cycles
- Data retention > 200 years
- Temperature ranges supported
  - Industrial (I) -40°C to +85°C
  - Automotive (E) -40°C to +125°C

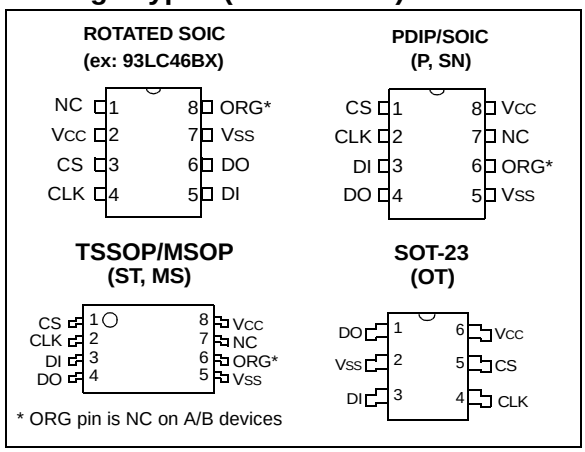
Pin Function Table

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
NC	No internal connection
ORG	Memory Configuration
Vcc	Power Supply

Description

The Microchip Technology Inc. 93XX46A/B/C devices are 1K bit low voltage serial Electrically Erasable PROMs (EEPROM). Word-selectable devices such as the 93AA46C, 93LC46C or 93C46C are dependent upon external logic levels driving the ORG pin to set word size. For dedicated 8-bit communication, the 93AA46A, 93LC46A or 93C46A devices are available, while the 93AA46B, 93LC46B and 93C46B devices provide dedicated 16-bit communication. Advanced CMOS technology makes these devices ideal for low power, nonvolatile memory applications. The entire 93XX Series is available in standard packages including 8-lead PDIP and SOIC, and advanced packaging including 8-lead MSOP, 6-lead SOT-23, and 8-lead TSSOP. Pb-free (Pure Matte Sn) finish is also available.

Package Types (not to scale)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....7.0V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			VCC = range by device (see Table on Page 1) Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C				
Param. No.	**Symbol**	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D1	VIH1 VIH2	High-level input voltage	2.0 0.7 VCC	— —	VCC +1 VCC +1	V V	VCC ≥ 2.7V VCC < 2.7V
D2	VIL1 VIL2	Low-level input voltage	-0.3 -0.3	— —	0.8 0.2 VCC	V V	VCC ≥ 2.7V VCC < 2.7V
D3	VOL1 VOL2	Low-level output voltage	— —	— —	0.4 0.2	V V	IOL = 2.1 mA, VCC = 4.5V IOL = 100 µA, VCC = 2.5V
D4	VOH1 VOH2	High-level output voltage	2.4 VCC - 0.2	— —	— —	V V	IOH = -400 µA, VCC = 4.5V IOH = -100 µA, VCC = 2.5V
D5	ILI	Input leakage current	—	—	±1	µA	VIN = VSS to VCC
D6	ILO	Output leakage current	—	—	±1	µA	VOUT = VSS to VCC
D7	CIN, COUT	Pin capacitance (all inputs/outputs)	—	—	7	pF	VIN/VOUT = 0V **(Note 1)** TA = 25°C, FCLK = 1 MHz
D8	ICC write	Write current	— —	— 500	2 —	mA µA	FCLK = 3 MHz, VCC = 5.5V FCLK = 2 MHz, VCC = 2.5V
D9	ICC read	Read current	— — —	— — 100	1 500 —	mA µA µA	FCLK = 3 MHz, VCC = 5.5V FCLK = 2 MHz, VCC = 3.0V FCLK = 2 MHz, VCC = 2.5V
D10	ICCS	Standby current	— —	— —	1 5	µA µA	I-Temp E-Temp CLK = CS = 0V ORG = DI = VSS or VCC **(Note 2) (NOTE 3)**
D11	VPOR	VCC voltage detect 93AA46A/B/C, 93LC46A/B/C 93C46A/B/C	— —	1.5V 3.8V	— —	V V	**(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: ORG pin not available on ‘A’ or ‘B’ versions.

3: READY/$\overline{\text{BUSY}}$ status must be cleared from DO, see **Section 3.4 "Data Out (DO)"**.

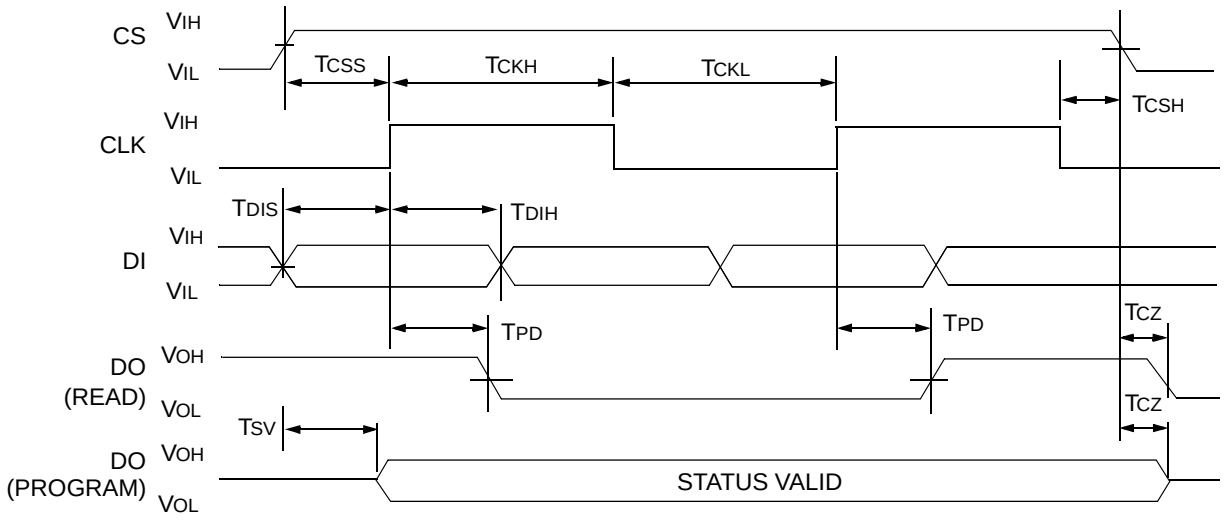
TABLE 1-2: AC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			V_{CC} = range by device (see Table on Page 1) Industrial (I): T_A = -40°C to +85°C Automotive (E): T_A = -40°C to +125°C			
Param. No.	**Symbol**	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
A1	F_{CLK}	Clock frequency	— — —	3 2 1	MHz MHz MHz	4.5V ≤ V_{CC} < 5.5V, 93XX46C only 2.5V ≤ V_{CC} < 5.5V 1.8V ≤ V_{CC} < 2.5V
A2	T_{CKH}	Clock high time	200 250 450	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V, 93XX46C only 2.5V ≤ V_{CC} < 5.5V 1.8V ≤ V_{CC} < 2.5V
A3	T_{CKL}	Clock low time	100 200 450	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V, 93XX46C only 2.5V ≤ V_{CC} < 5.5V 1.8V ≤ V_{CC} < 2.5V
A4	T_{CSS}	Chip Select setup time	50 100 250	— — —	ns ns ns	4.5V ≤ V_{CC} < 5.5V 2.5V ≤ V_{CC} < 4.5V 1.8V ≤ V_{CC} < 2.5V
A5	T_{CSH}	Chip Select hold time	0	—	ns	1.8V ≤ V_{CC} < 5.5V
A6	T_{CSL}	Chip Select low time	250	—	ns	1.8V ≤ V_{CC} < 5.5V
A7	T_{DIS}	Data input setup time	50 100 250	—	ns	4.5V ≤ V_{CC} < 5.5V, 93XX46C only 2.5V ≤ V_{CC} < 5.5V 1.8V ≤ V_{CC} < 2.5V
A8	T_{DIH}	Data input hold time	50 100 250	—	ns	4.5V ≤ V_{CC} < 5.5V, 93XX46C only 2.5V ≤ V_{CC} < 5.5V 1.8V ≤ V_{CC} < 2.5V
A9	T_{PD}	Data output delay time	— — —	200 250 400	ns	4.5V ≤ V_{CC} < 5.5V, C_L = 100 pF 2.5V ≤ V_{CC} < 4.5V, C_L = 100 pF 1.8V ≤ V_{CC} < 2.5V, C_L = 100 pF
A10	T_{CZ}	Data output disable time	— —	100 200	ns	4.5V ≤ V_{CC} < 5.5V, **(Note 1)** 1.8V ≤ V_{CC} < 4.5V, **(Note 1)**
A11	T_{SV}	Status valid time	—	200 300 500	ns	4.5V ≤ V_{CC} < 5.5V, C_L = 100 pF 2.5V ≤ V_{CC} < 4.5V, C_L = 100 pF 1.8V ≤ V_{CC} < 2.5V, C_L = 100 pF
A12	T_{WC}	Program cycle time	—	6	ms	Erase/Write mode (AA and LC versions)
A13	T_{WC}		—	2	ms	Erase/Write mode (93C versions)
A14	T_{EC}		—	6	ms	ERAL mode, 4.5V ≤ V_{CC} ≤ 5.5V
A15	T_{WL}		—	15	ms	WRAL mode, 4.5V ≤ V_{CC} ≤ 5.5V
A16	—	Endurance	1M	—	cycles	25°C, V_{CC} = 5.0V, **(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This application is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which may be obtained from www.microchip.com.

FIGURE 1-1: SYNCHRONOUS DATA TIMING



Note: TSV is relative to CS.

TABLE 1-3: INSTRUCTION SET FOR X 16 ORGANIZATION (93XX46B OR 93XX46C WITH ORG = 1)

Instruction	SB	Opcode	Address						Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	9
ERAL	1	00	1	0	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	9
EWDS	1	00	0	0	X	X	X	X	—	HIGH-Z	9
EWEN	1	00	1	1	X	X	X	X	—	HIGH-Z	9
READ	1	10	A5	A4	A3	A2	A1	A0	—	D15 - D0	25
WRITE	1	01	A5	A4	A3	A2	A1	A0	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25
WRAL	1	00	0	1	X	X	X	X	D15 - D0	(RDY/$\overline{\text{BSY}}$)	25

TABLE 1-4: INSTRUCTION SET FOR X 8 ORGANIZATION (93XX46A OR 93XX46C WITH ORG = 0)

Instruction	SB	Opcode	Address							Data In	Data Out	Req. CLK Cycles
ERASE	1	11	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	10
ERAL	1	00	1	0	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	10
EWDS	1	00	0	0	X	X	X	X	X	—	HIGH-Z	10
EWEN	1	00	1	1	X	X	X	X	X	—	HIGH-Z	10
READ	1	10	A6	A5	A4	A3	A2	A1	A0	—	D7 - D0	18
WRITE	1	01	A6	A5	A4	A3	A2	A1	A0	D7 - D0	(RDY/$\overline{\text{BSY}}$)	18
WRAL	1	00	0	1	X	X	X	X	X	D7 - D0	(RDY/$\overline{\text{BSY}}$)	18

2.0 FUNCTIONAL DESCRIPTION

When the ORG* pin is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/BUSY status during a programming operation. The READY/BUSY status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the HIGH-Z state on the falling edge of CS.

2.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK, and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a Start condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a “bus conflict” to occur during the “dummy zero” that precedes the READ operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

2.3 Data Protection

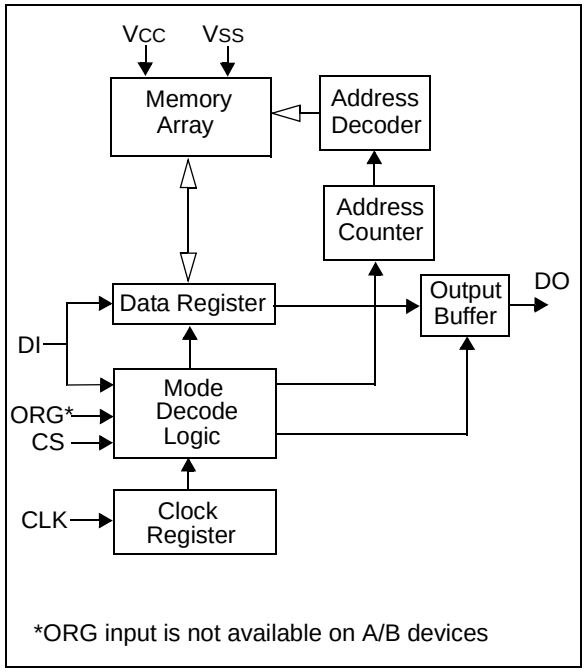
All modes of operation are inhibited when VCC is below a typical voltage of 1.5V for '93AA' and '93LC' devices or 3.8V for '93C' devices.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

Note: For added protection, an EWDS command should be performed after every write operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before the initial ERASE or WRITE instruction can be executed.

Block Diagram



2.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical ‘1’ state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle, except on ‘93C’ devices where the rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical ‘0’ indicates that programming is still in progress. DO at logical ‘1’ indicates that the register at the specified address has been erased and the device is ready for another instruction.

Note: Issuing a Start bit and then taking CS low will clear the READY/$\overline{\text{BUSY}}$ status from DO.

FIGURE 2-1: ERASE TIMING FOR 93AA AND 93LC DEVICES

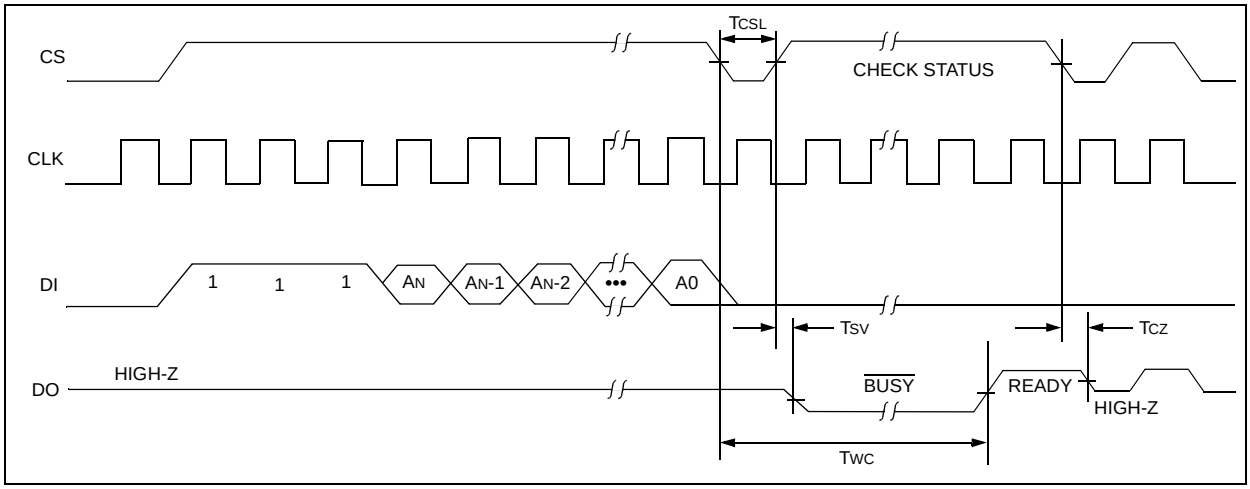
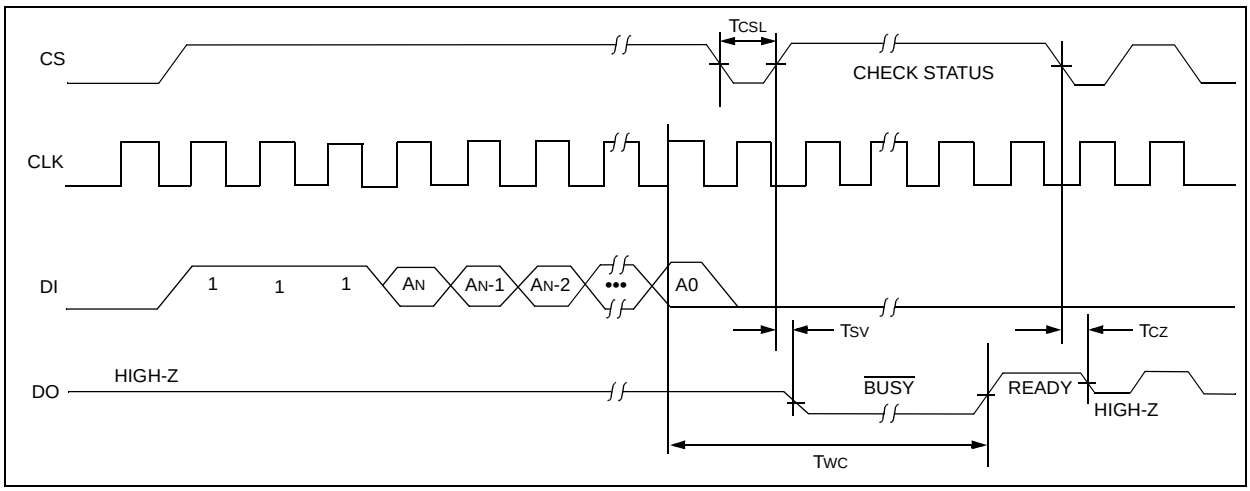


FIGURE 2-2: ERASE TIMING FOR 93C DEVICES



2.5 ERASE ALL (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical '1' state. The ERAL cycle is identical to the ERASE cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS, except on '93C' devices where the rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (T_{CSL}).

Note: Issuing a Start bit and then taking CS low will clear the READY/$\overline{\text{BUSY}}$ status from DO.

V_{CC} must be ≥ 4.5V for proper operation of ERAL.

FIGURE 2-3: ERAL TIMING FOR 93AA AND 93LC DEVICES

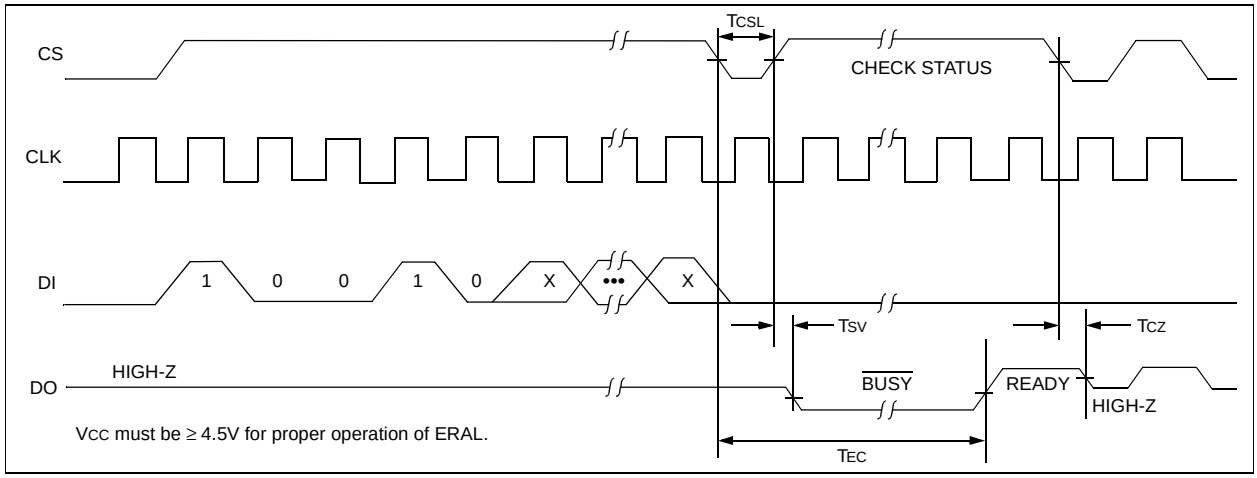
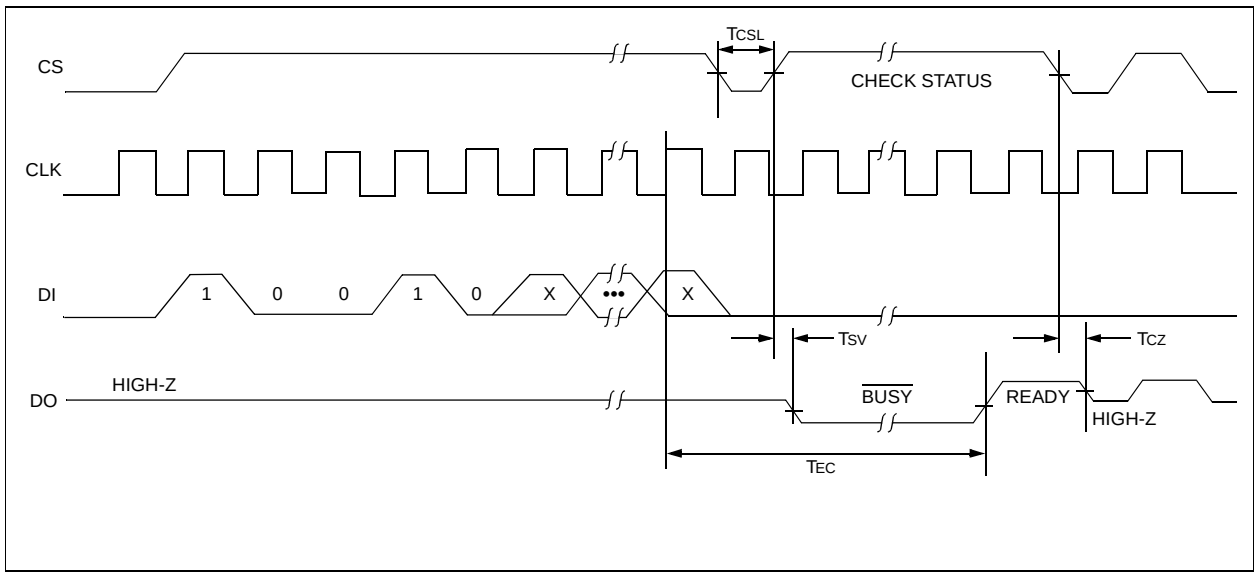


FIGURE 2-4: ERAL TIMING FOR 93C DEVICES



2.6 ERASE/WRITE DISABLE And ENABLE (EWDS/EWEN)

The 93XX46A/B/C powers up in the ERASE/WRITE Disable (EWDS) state. All Programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

FIGURE 2-5: EWDS TIMING

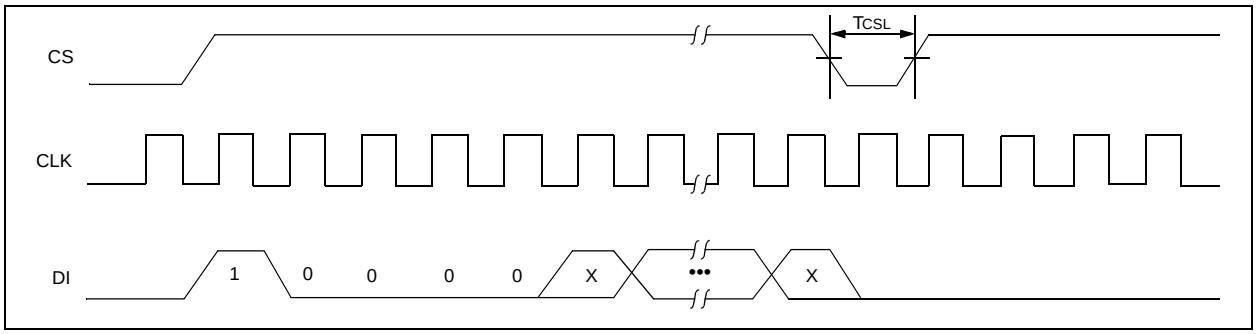
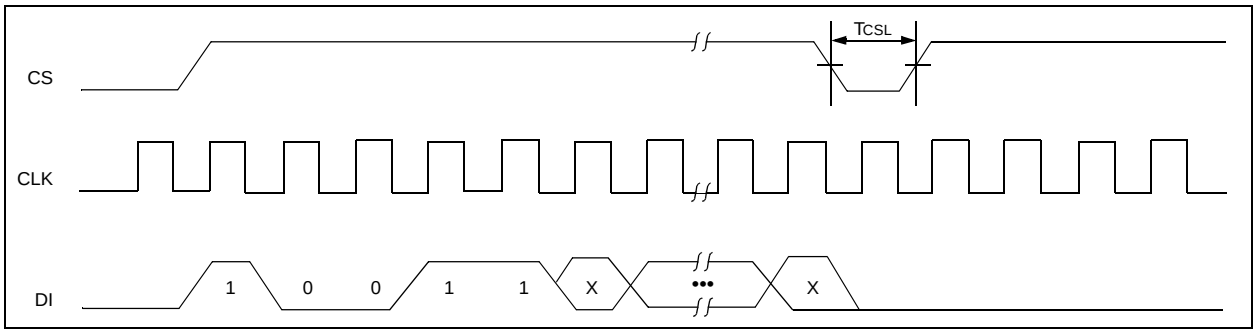


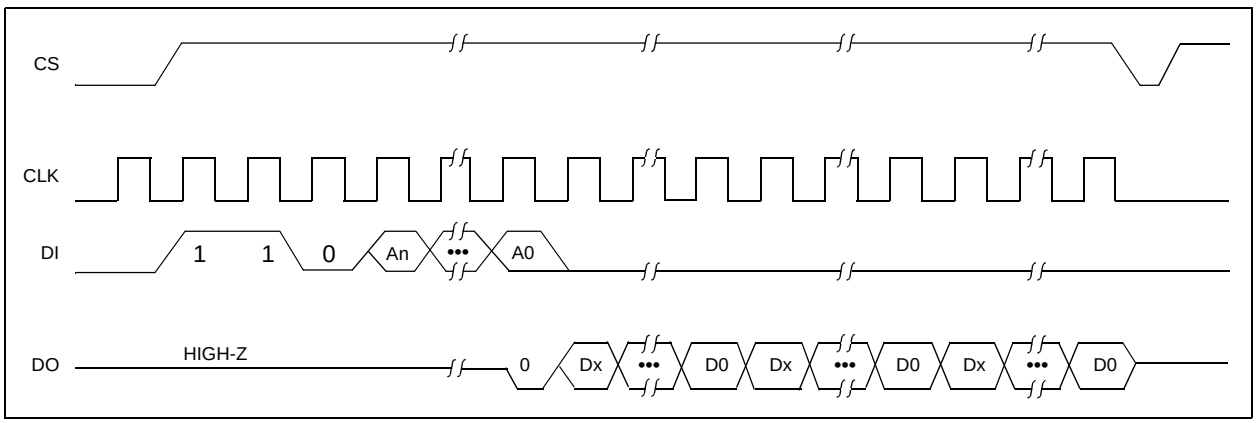
FIGURE 2-6: EWEN TIMING



2.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (If ORG pin is low or A-Version devices) or 16-bit (If ORG pin is high or B-version devices) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 2-7: READ TIMING



2.8 WRITE

The WRITE instruction is followed by 8 bits (If ORG is low or A-version devices) or 16 bits (If ORG pin is high or B-version devices) of data which are written into the specified address. For 93AA46A/B/C and 93LC46A/B/C devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93C46A/B/C devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

Note: Issuing a Start bit and then taking CS low will clear the READY/$\overline{\text{BUSY}}$ status from DO.

FIGURE 2-8: WRITE TIMING FOR 93AA AND 93LC DEVICES

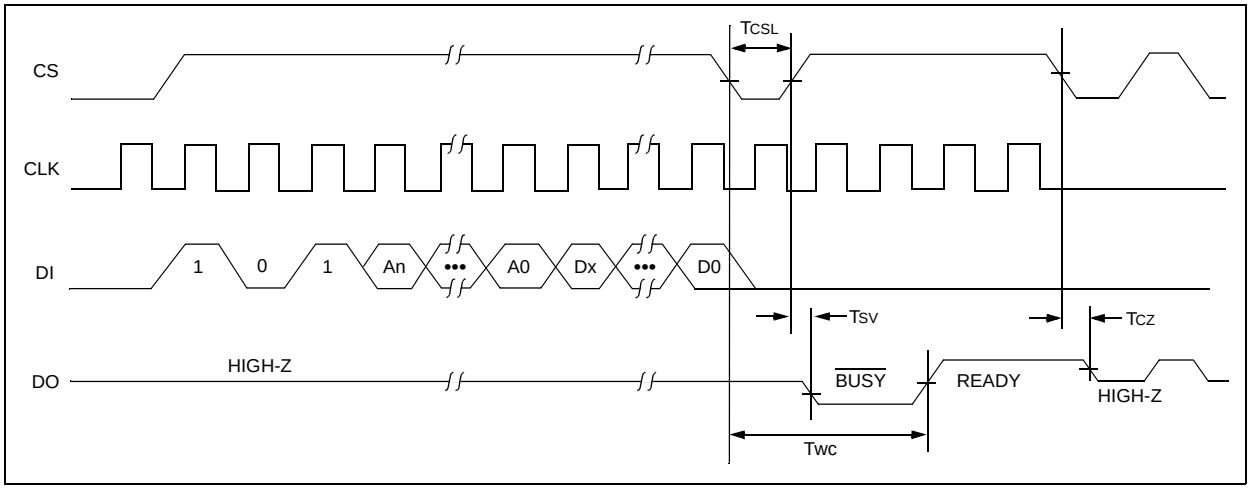
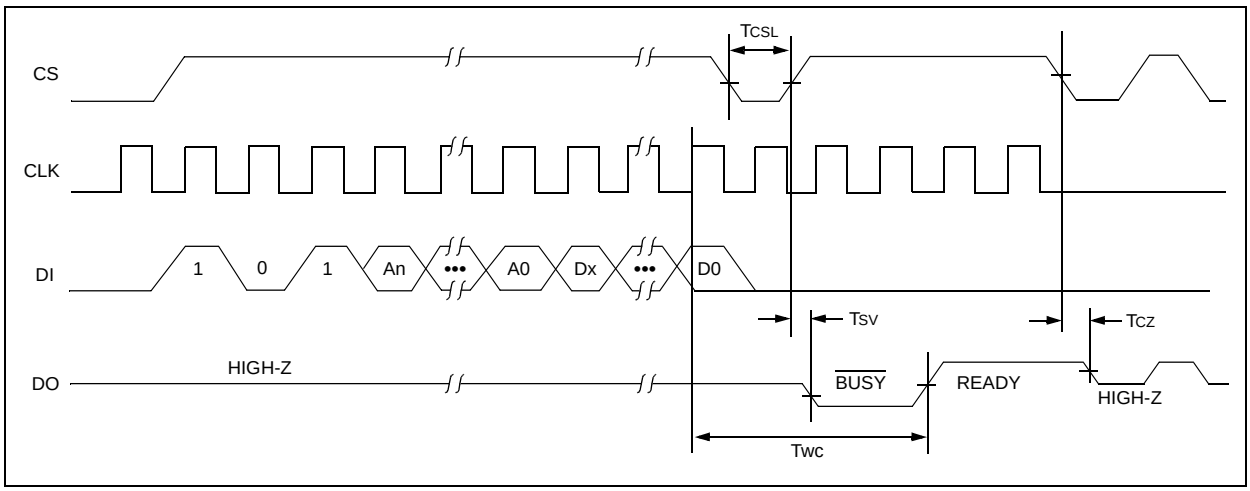


FIGURE 2-9: WRITE TIMING FOR 93C DEVICES



2.9 WRITE ALL (WRAL)

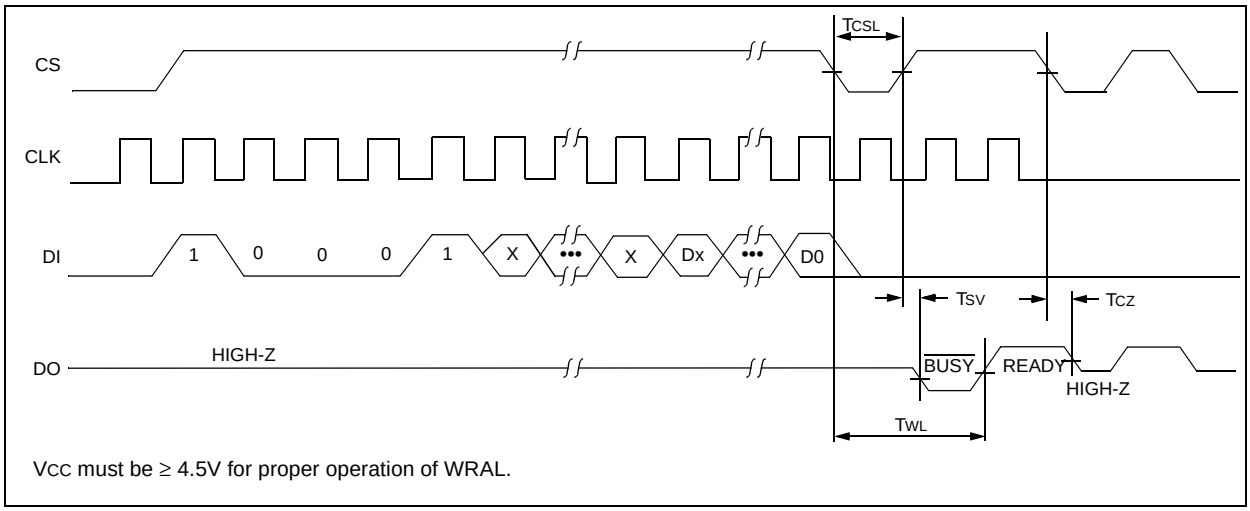
The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. For 93AA46A/B/C and 93LC46A/B/C devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93C46A/B/C devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}).

Note: Issuing a Start bit and then taking CS low will clear the READY/$\overline{\text{BUSY}}$ status from DO.

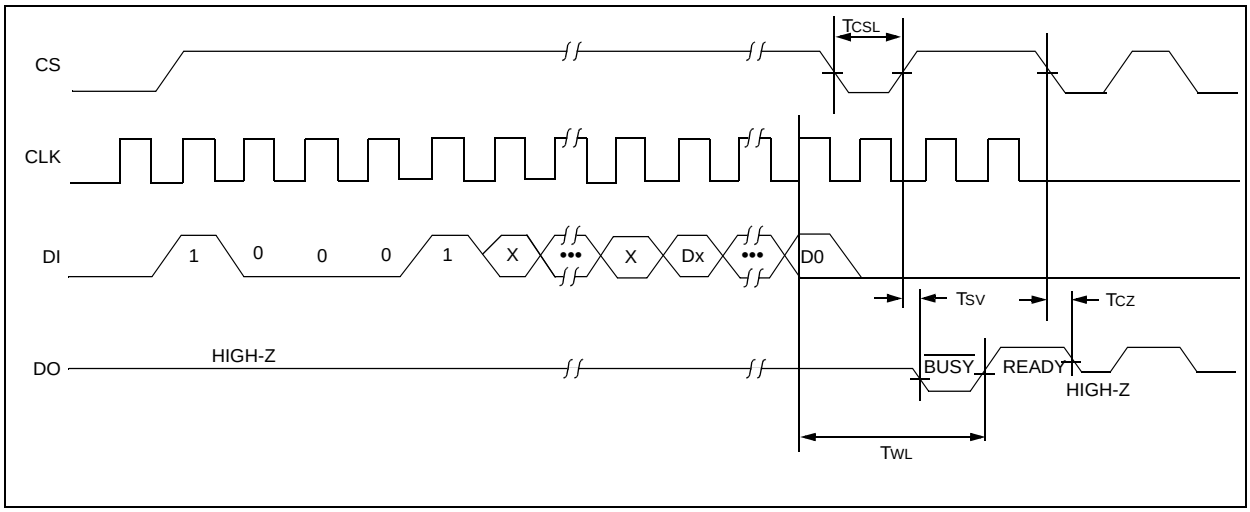
V_{CC} must be ≥ 4.5V for proper operation of WRAL.

FIGURE 2-10: WRAL TIMING FOR 93AA AND 93LC DEVICES



V_{CC} must be ≥ 4.5V for proper operation of WRAL.

FIGURE 2-11: WRAL TIMING FOR 93C DEVICES



3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN DESCRIPTIONS

Name	SOIC/PDIP/ MSOP/ TSSOP	SOT-23	Rotated SOIC	Function
CS	1	5	3	Chip Select
CLK	2	4	4	Serial Clock
DI	3	3	5	Data In
DO	4	1	6	Data Out
Vss	5	2	7	Ground
ORG/NC	6	N/A	8	Organization / 93XX46C No internal connection / 93XX46A/B
NC	7	N/A	1	No Internal Connection
VCC	8	6	2	Power Supply

3.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a “Don't Care” if CS is low (device deselected). If CS is high, but the Start condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed. CLK and DI then become don't care inputs waiting for a new Start condition to be detected.

3.3 Data In (DI)

Data In (DI) is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out (DO) is used in the READ mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum Chip Select low time (TCSL) and an ERASE or WRITE operation has been initiated.

The Status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

Note: Issuing a Start bit and then taking CS low will clear the READY/$\overline{\text{BUSY}}$ status from DO.

3.5 Organization (ORG)

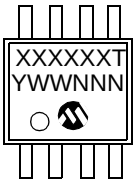
When the ORG pin is connected to VCC or Logic HI, the (x16) memory organization is selected. When the ORG pin is tied to VSS or Logic LO, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

93XX46A devices are always x8 organization and 93XX46B devices are always x16 organization.

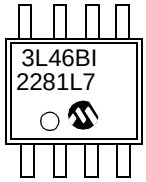
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

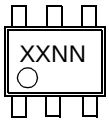
8-Lead MSOP (150 mil)



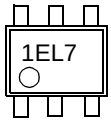
Example:



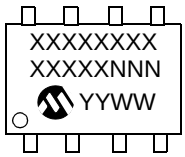
6-Lead SOT-23



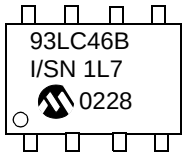
Example:



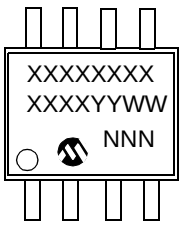
8-Lead PDIP



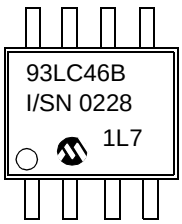
Example:



8-Lead SOIC

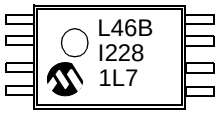


Example:



8-Lead TSSOP

Example:



MSOP 1st Line Marking Codes		
Device	std mark	Pb-free mark
93AA46A	3A46AT	GA46AT
93AA46B	3A46BT	GA46BT
93AA46C	3A46CT	GA46CT
93LC46A	3L46AT	GL46AT
93LC46B	3L46BT	GL46BT
93LC46C	3L46CT	GL46CT
93C46A	3C46AT	GC46AT
93C46B	3C46BT	GC46BT
93C46C	3C46CT	GC46CT
T = blank for commercial, “I” for Industrial, “E” for Extended.		

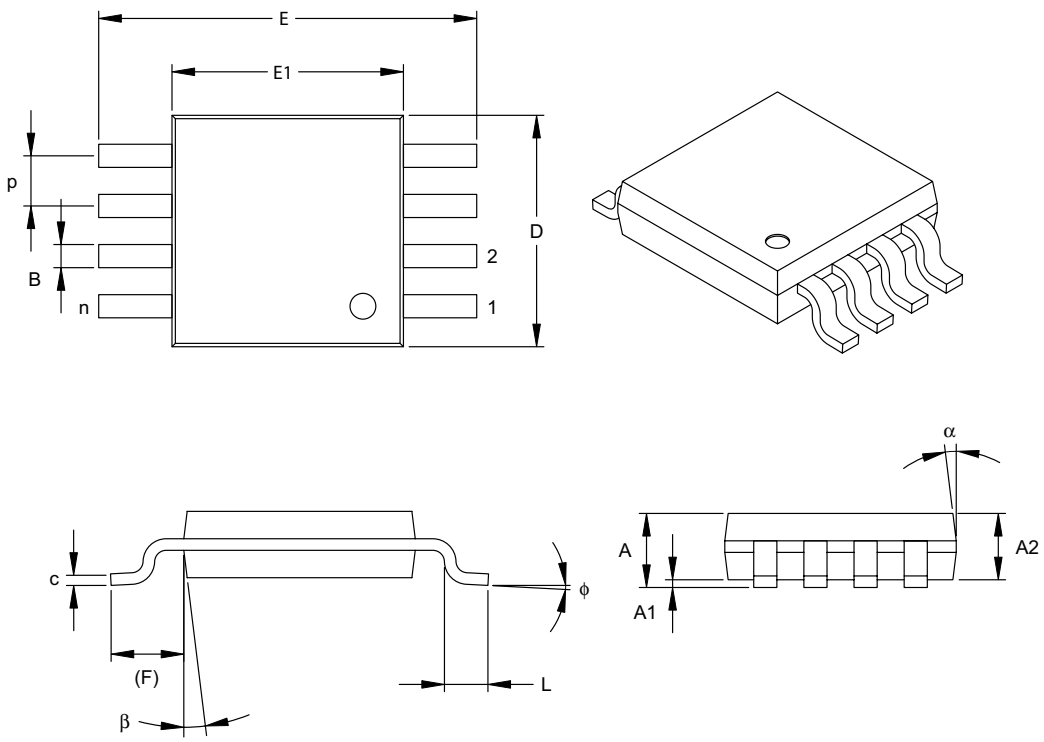
SOT23 Marking Codes		
Device	I-temp	E-temp
93AA46A	1BNN	–
93AA46B	1LNN	–
93LC46A	1ENN	1FNN
93LC46B	1PNN	1RNN
93C46A	1HNN	1JNN
93C46B	1TNN	1UNN
Pb-free topside mark is same; Pb-free noted only on carton label.		

TSSOP 1st Line Marking Codes		
Device	std mark	Pb-free mark
93AA46A	A46A	GAAA
93AA46B	A46B	GAAB
93AA46C	A46C	GAAC
93LC46A	L46A	GLAA
93LC46B	L46B	GLAB
93LC46C	L46C	GLAC
93C46A	C46A	GCAA
93C46B	C46B	GCAB
93C46C	C46C	GCAC
Temperature grade is marked on line 2.		

Legend:	XX...X	Part number
	T	Temperature
	Blank	Commercial
	I	Industrial
	E	Extended
	YY	Year code (last 2 digits of calendar year) except TSSOP and MSOP which use only the last 1 digit
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: Custom marking available.

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

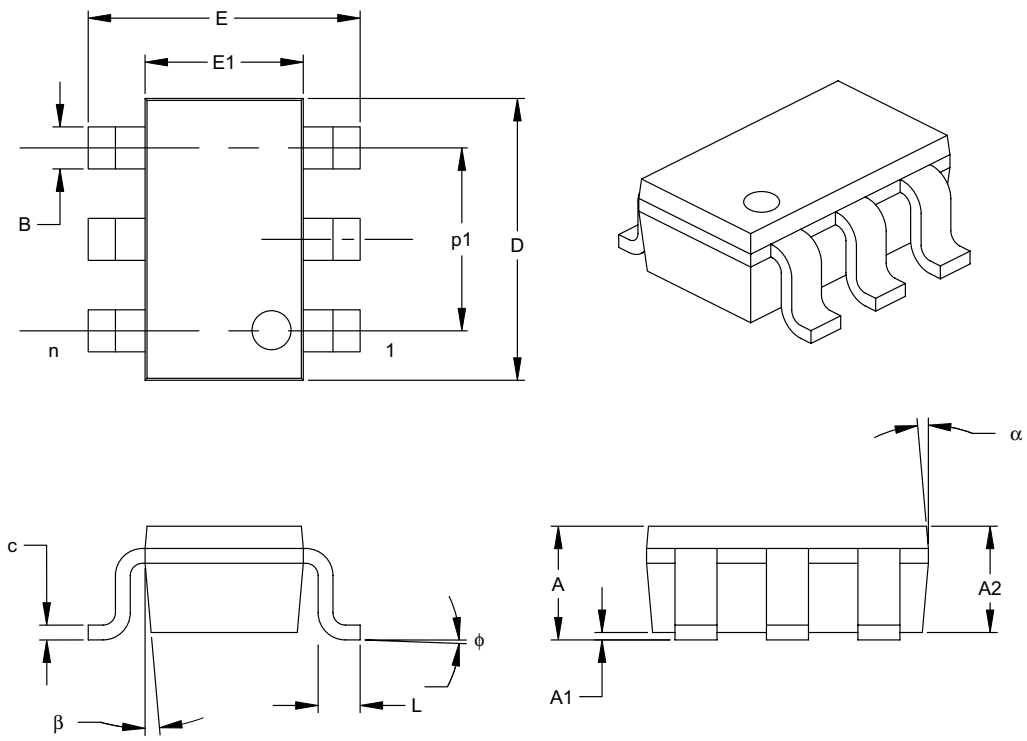
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

6-Lead Plastic Small Outline Transistor (OT) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		6			6	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

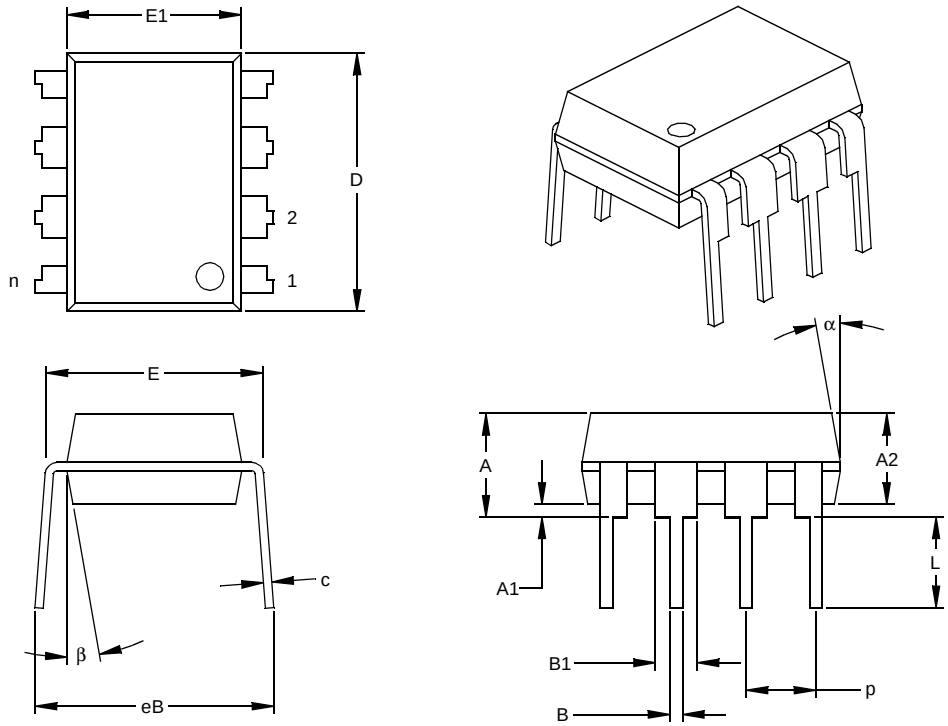
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (formerly EIAJ) equivalent: SC-74A

Drawing No. C04-120

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

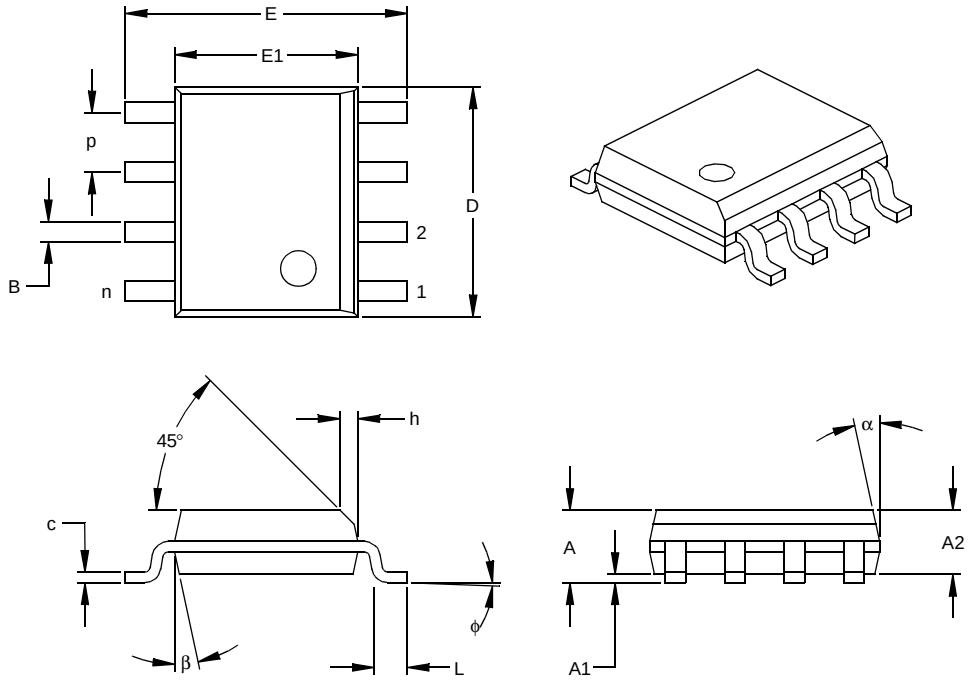


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

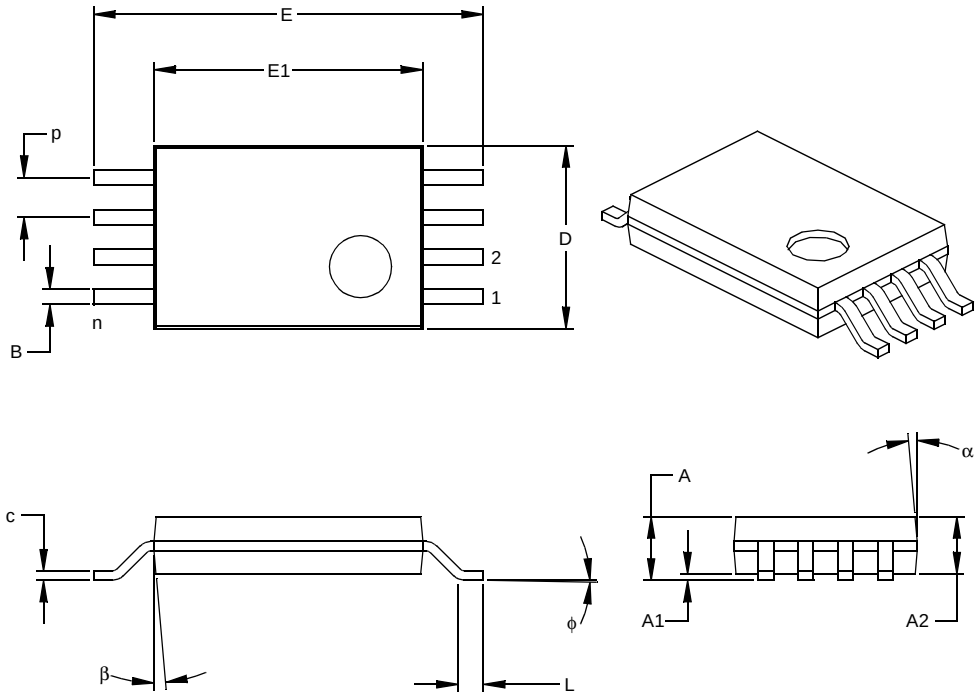


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

APPENDIX A: REVISION HISTORY

Revision D

Corrections to Section 1.0, Electrical Characteristics.
Section 4.1, 6-Lead SOT-23 package to OT.

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Questions:

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7. How would you improve this document?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	X	/XX	X
Device	Pinout	Tape & Reel	Temperature Range	Package	Lead Finish

Device	93AA46A:	1K 1.8V Microwire Serial EEPROM
	93AA46B:	1K 1.8V Microwire Serial EEPROM
	93AA46C:	1K 1.8V Microwire Serial EEPROM w/ORG
	93LC46A:	1K 2.5V Microwire Serial EEPROM
	93LC46B:	1K 2.5V Microwire Serial EEPROM
	93LC46C:	1K 2.5V Microwire Serial EEPROM w/ORG
	93C46A:	1K 5.0V Microwire Serial EEPROM
	93C46B:	1K 5.0V Microwire Serial EEPROM
	93C46C:	1K 5.0V Microwire Serial EEPROM w/ORG
Pinout:	Blank =	Standard pinout
	X =	Rotated pinout
Tape & Reel:	Blank =	Standard packaging
	T =	Tape & Reel
Temperature Range	I =	-40°C to +85°C
	E =	-40°C to +125°C
Package	MS =	Plastic MSOP (Micro Small outline, 8-lead)
	OT =	SOT-23, 6-lead (Tape & Reel only)
	P =	Plastic DIP (300 mil body), 8-lead
	SN =	Plastic SOIC (150 mil body), 8-lead
	ST =	TSSOP, 8-lead
Lead Finish:	Blank =	Standard 63% / 37% SnPb
	G =	Pure Matte Sn

Examples:

a) 93AA46C-I/MS: 1K, 128x8 or 64x16 Serial EEPROM, MSOP package, 1.8V

b) 93AA46B-I/MS: 1K, 64x16 Serial EEPROM, MSOP package, 1.8V

c) 93AA46AT-I/OT: 1K, 128x8 Serial EEPROM, SOT-23 package, tape and reel, 1.8V

d) 93AA46CT-I/MS: 1K, 128x8 or 16x16 Serial EEPROM, MSOP package, tape and reel, 1.8V

a) 93LC46A-I/MS: 1K, 128x8 Serial EEPROM, MSOP package, 2.5V

b) 93LC46BT-I/OT: 1K, 64x16 Serial EEPROM, SOT-23 package, tape and reel, 2.5V

c) 93LC46B-I/MS: 1K, 64x16 Serial EEPROM, MSOP package, 2.5V

d) 93LC46BXT-I/SNG: 1K, 64x16 Serial EEPROM, SOIC package, rotated pinout, Industrial temperature, Pb-free finish, 2.5V

a) 93C46B-I/MS: 1K, 64x16 Serial EEPROM, MSOP package, 5.0V

b) 93C46C-I/MS: 1K, 128x8 or 16x16 Serial EEPROM, MSOP package, 5.0V

c) 93C46AT-I/OT: 1K, 128x8 Serial EEPROM, SOT-23 package, tape and reel, 5.0V

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