

MITSUBISHI LSTTLs

M74LS273P

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

DESCRIPTION

The M74LS273P is a semiconductor integrated circuit containing 8 D-type positive edge-triggered flip-flop circuits with common direct reset and clock inputs.

FEATURES

- Positive edge-triggering
- High mounting density with 8 circuits contained
- Direct reset and clock inputs common to all 8 circuits
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

APPLICATION

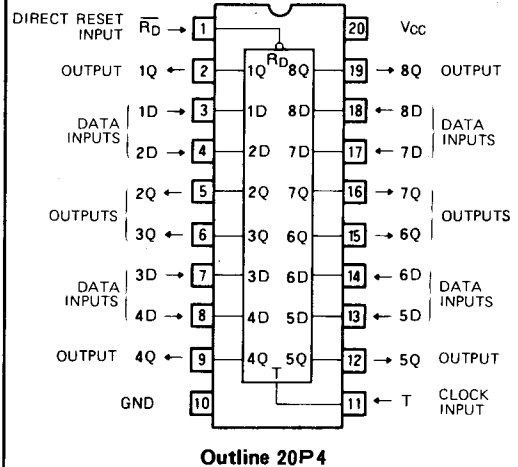
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 8 edge-triggered D-type flip-flop circuits and it is provided with direct reset $\overline{R_D}$ input and clock input T common to all 8 circuits. When T changes in each flip-flop from low to high, the data input signal D immediately before the change appears in output Q.

When $\overline{R_D}$ is set low, 1Q through 8Q are all set low irrespective of the status of the 1D through 8D and T signals. For use as a D-type flip-flop, $\overline{R_D}$ must be kept in high.

PIN CONFIGURATION (TOP VIEW)



FUNCTION TABLE (Note 1)

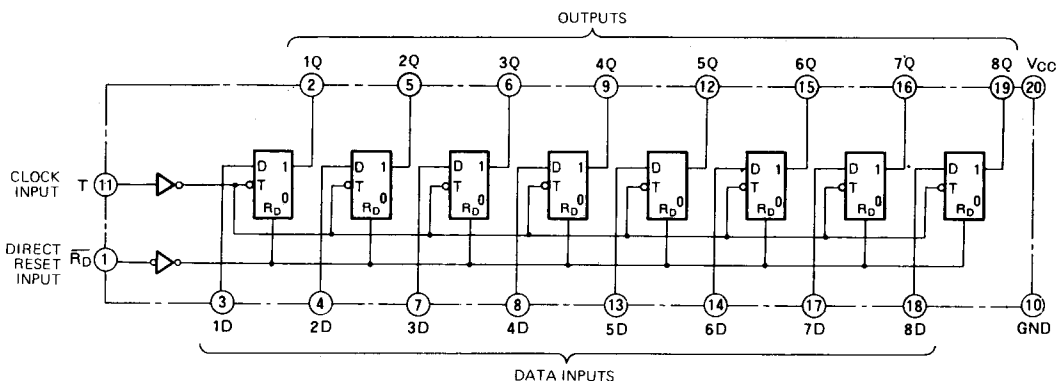
$\overline{R_D}$	T	D	Q
L	X	X	L
H	\uparrow	H	H
H	\uparrow	L	L
H	L	X	Q^0

Note 1 \uparrow : Transition from low to high (positive edge trigger)

Q^0 : Level of Q before the indicated steady-state input conditions were established.

X : Irrelevant

BLOCK DIAGRAM



OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage		-0.5 ~ +7	V
V _I	Input voltage		-0.5 ~ +15	V
V _O	Output voltage	High-level state	-0.5 ~ V _{CC}	V
T _{opr}	Operating free-air ambient temperature range		-20 ~ +75	°C
T _{stg}	Storage temperature range		-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V _{CC}	Supply voltage		4.75	5	5.25	V
I _{OH}	High-level output current	V _{OH} ≥ 2.7V	0		-400	μA
I _{OL}	Low-level output current	V _{OL} ≤ 0.4V	0		4	mA
		V _{OL} ≤ 0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{IC}	Input clamp voltage	V _{CC} = 4.75V, I _{IC} = -18mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = 4.75V, V _I = 0.8V V _I = 2V, I _{OH} = -400μA	2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = 4.75V, I _{OL} = 4mA		0.25	0.4	V
		V _I = 0.8V, V _I = 2V, I _{OL} = 8mA		0.35	0.5	V
I _{IH}	High-level input current	V _{CC} = 5.25V, V _I = 2.7V			20	μA
		V _{CC} = 5.25V, V _I = 10V			0.1	mA
I _{IL}	Low-level input current	V _{CC} = 5.25V, V _I = 0.4V			-0.4	mA
I _{OS}	Short-circuit output current (Note 2)	V _{CC} = 5.25V, V _O = 0V	-20		-100	mA
I _{CC}	Supply current	V _{CC} = 5.25V (Note 3)		17	27	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C

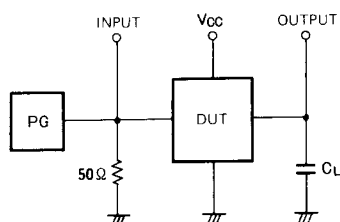
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured after 1D ~ 8D and \overline{R}_D are made 4.5V and T has been changed from 0V to 4.5V.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f _{max}	Maximum clock frequency		30	40		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from T to 1Q~8Q	C _L = 15pF (Note 4)		12	27	ns
t _{PHL}	High-to-low-level output propagation time, from \overline{R}_D to 1Q~8Q			13	27	ns
t _{PHL}	High-to-low-level output propagation time, from \overline{R}_D to 1Q~8Q			15	27	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:

PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_p = 3V_{p-p}, Z_o = 50Ω.

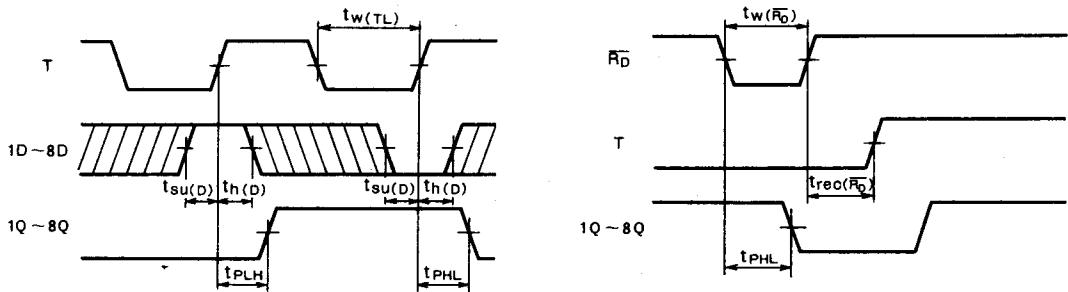
(2) C_L includes probe and jig capacitance.

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TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_w(TL)$	Clock input T low pulse width		20	7		ns
$t_w(R\bar{D})$	Direct reset pulse width		20	6		ns
$t_{su}(D)$	Setup time $1D \sim 8D$ to T		20	7		ns
$t_h(D)$	Hold time $1D \sim 8D$ to T		5	-3		ns
$t_{rec}(R\bar{D})$	Recovery time $R\bar{D}$ to T		25	8		ns

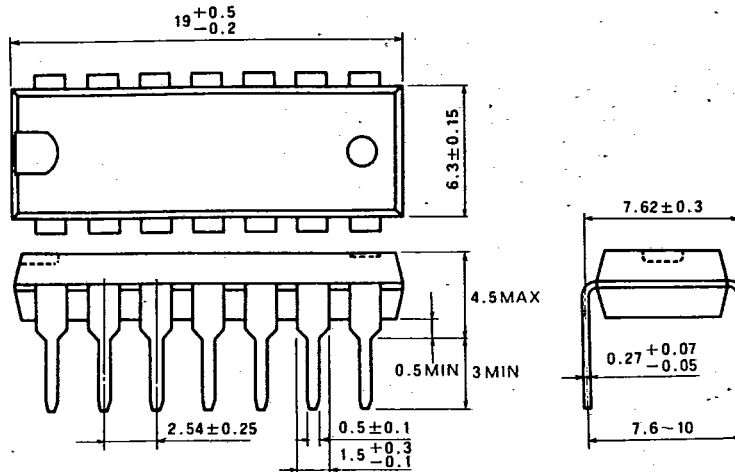
TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

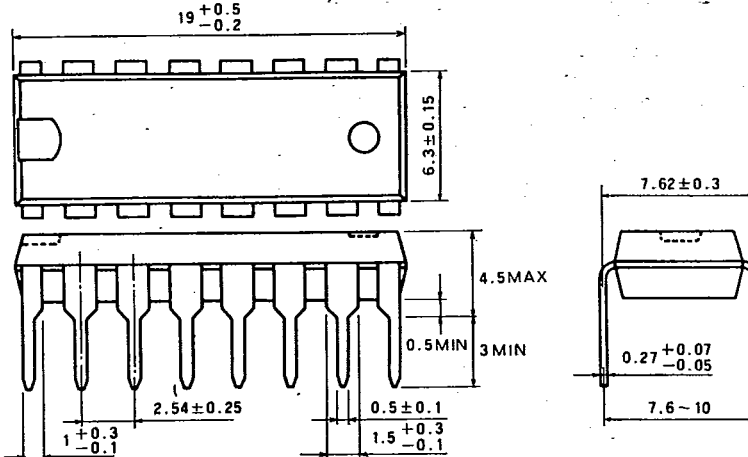
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

