

SIEMENS

Microcomputer Components

16-Bit CMOS Single-Chip Microcontroller

C167CR

Edition 06.95

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C167CR	
Revision History: Original Version: 06.95 (Advance Information)	
Previous Releases: Data Sheet C167 06.94	
Page	Subjects (changes compared to C167)
32	Register PICON added
37	V_{ILS} , V_{IHS} , HYS, I_{OV} added.
37	R_{RST} , I_{RWH} , I_{RWL} , I_{ALEL} , I_{ALEH} , I_{P6H} , test cond. I_{OZx} changed.
38	I_{P6L} , I_{CC} , I_{ID} changed.
39	I_{CC} , I_{ID} typical values added
40	ADC specification changed.
43...45	PLL description added.
45	External Clock Drive specification changed.
47	t_{14} , t_{15} , t_{16} , t_{17} , t_{22} , t_{39} , t_{46} changed.
47	t_{47} changed.
53	t_{14} , t_{15} , t_{16} , t_{17} , t_{20} , t_{21} , t_{22} changed.
54	t_{39} , t_{46} , t_{47} , t_{55} changed.
57, 58	t_{53} changed to t_{68} .
59	t_{36} changed.
63	t_{63} changed.

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C16x-Family of High-Performance CMOS 16-Bit Microcontrollers

C167CR

Advance Information

C167CR 16-Bit Microcontroller

- High Performance 16-bit CPU with 4-Stage Pipeline
- 100 ns Instruction Cycle Time at 20 MHz CPU Clock
- 500 ns Multiplication (16×16 bit), 1 μ s Division (32 / 16 bit)
- Enhanced Boolean Bit Manipulation Facilities
- Additional Instructions to Support HLL and Operating Systems
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- Clock Generation via on-chip PLL or via direct clock input
- Up to 16 MBytes Linear Address Space for Code and Data
- 2 KBytes On-Chip Internal RAM (IRAM)
- 2 KBytes On-Chip Extension RAM (XRAM)
- Programmable External Bus Characteristics for Different Address Ranges
- 8-Bit or 16-Bit External Data Bus
- Multiplexed or Demultiplexed External Address/Data Buses
- Five Programmable Chip-Select Signals
- Hold- and Hold-Acknowledge Bus Arbitration Support
- 1024 Bytes On-Chip Special Function Register Area
- Idle and Power Down Modes
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 50 ns
- 16-Channel 10-bit A/D Converter with 9.7 μ s Conversion Time
- Two 16-Channel Capture/Compare Units
- 4-Channel PWM Unit
- Two Multi-Functional General Purpose Timer Units with 5 Timers
- Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- On-Chip CAN Interface with 15 Message Objects (Full-CAN/Basic-CAN)
- Programmable Watchdog Timer
- Up to 111 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- Supported by a Wealth of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 144-Pin MQFP Package (EIAJ)

This document describes the **SAB-C167CR-LM**, the **SAF-C167CR-LM** and the **SAK-C167CR-LM**. For simplicity all versions are referred to by the term **C167CR** throughout this document.

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54	t_{39} , t_{46} , t_{47} , t_{55} changed.
57, 58	t_{53} changed to t_{68} .
59	t_{36} changed.
63	t_{63} changed.

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Introduction

The C167CR is a new derivative of the Siemens C16x Family of full featured single-chip CMOS microcontrollers. It combines high CPU performance (up to 10 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. It also provides on-chip high-speed RAM and clock generation via PLL.

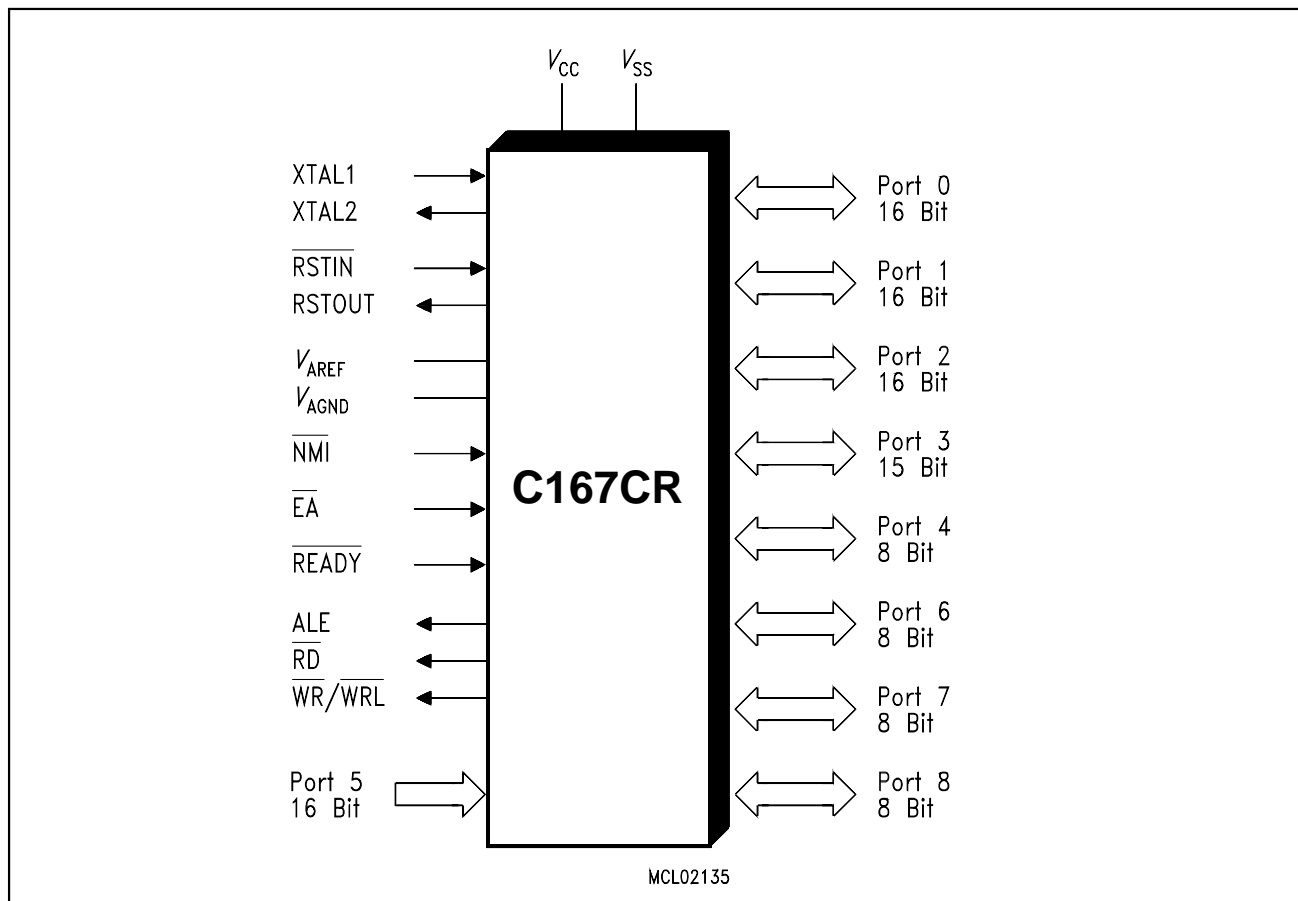


Figure 1
Logic Symbol

Ordering Information

Type	Ordering Code	Package	Function
SAB-C167CR-LM	Q67121-C942	P-MQFP-144-1	16-bit microcontroller with 2 × 2 KByte RAM Temperature range 0 to + 70 °C
SAF-C167CR-LM	Q67121-C946	P-MQFP-144-1	16-bit microcontroller with 2 × 2 KByte RAM Temperature range – 40 to + 85 °C
SAK-C167CR-LM	Q67121-C967	P-MQFP-144-1	16-bit microcontroller with 2 × 2 KByte RAM Temperature range – 40 to + 125 °C

Pin Configuration (top view)

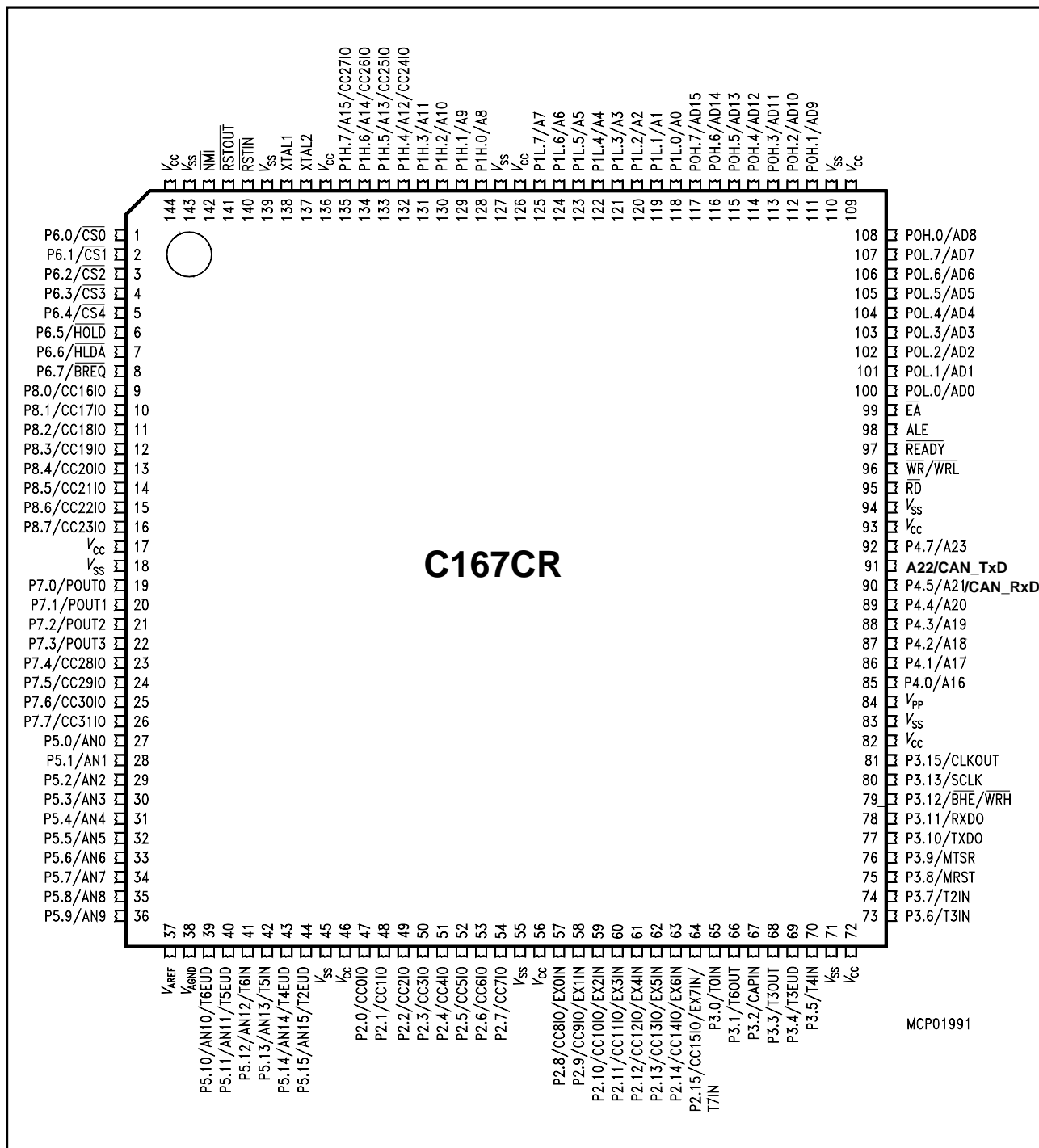


Figure 2

Pin Definitions and Functions

Symbol	Pin Number	Input (I) Output (O)	Function
P6.0 - P6.7	1 - 8	I/O	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The following Port 6 pins also serve for alternate functions:
	1	O	P6.0 $\overline{CS0}$ Chip Select 0 Output

	5	O	P6.4 $\overline{CS4}$ Chip Select 4 Output
	6	I	P6.5 \overline{HOLD} External Master Hold Request Input
	7	O	P6.6 \overline{HLDA} Hold Acknowledge Output
	8	O	P6.7 \overline{BREQ} Bus Request Output
P8.0 - P8.7	9 - 16	I/O	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special).
	9	I/O	The following Port 8 pins also serve for alternate functions:
	P8.0 CC16IO CAPCOM2: CC16 Cap.-In/Comp.Out
	16	I/O	...
P7.0 - P7.7	19 - 26	I/O	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special).
	19	O	The following Port 7 pins also serve for alternate functions:
	P7.0 POUT0 PWM Channel 0 Output
	22	O	...
	23	I/O	P7.3 POUT3 PWM Channel 3 Output
	P7.4 CC28IO CAPCOM2: CC28 Cap.-In/Comp.Out
	26	I/O	...
			P7.7 CC31IO CAPCOM2: CC31 Cap.-In/Comp.Out

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function
P5.0 - P5.15	27 - 36	I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as the (up to 16) analog input channels for the A/D converter, where P5.x equals ANx (Analog input channel x), or they serve as timer inputs: P5.10 T6EUD GPT2 Timer T6 Ext.Up/Down Ctrl.Input P5.11 T5EUD GPT2 Timer T5 Ext.Up/Down Ctrl.Input P5.12 T6IN GPT2 Timer T6 Count Input P5.13 T5IN GPT2 Timer T5 Count Input P5.14 T4EUD GPT1 Timer T4 Ext.Up/Down Ctrl.Input P5.15 T2EUD GPT1 Timer T2 Ext.Up/Down Ctrl.Input
	39	I	
	40	I	
	41	I	
	42	I	
	43	I	
	44	I	
P2.0 - P2.15	47 - 54	I/O	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions: P2.0 CC0IO CAPCOM: CC0 Cap.-In/Comp.Out P2.7 CC7IO CAPCOM: CC7 Cap.-In/Comp.Out P2.8 CC8IO CAPCOM: CC8 Cap.-In/Comp.Out, EX0IN Fast External Interrupt 0 Input P2.15 CC15IO CAPCOM: CC15 Cap.-In/Comp.Out, EX7IN Fast External Interrupt 7 Input T7IN CAPCOM2 Timer T7 Count Input
	57 - 64	I/O	
	47	I/O	
	
	54	I/O	
	57	I/O	
		I	
	
	64	I/O	
		I	
		I	

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function
P3.0 - P3.13, P3.15	65 - 70, 73 - 80, 81	I/O I/O I/O	Port 3 is a 15-bit (P3.14 is missing) bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:
	65	I	P3.0 T0IN CAPCOM Timer T0 Count Input
	66	O	P3.1 T6OUT GPT2 Timer T6 Toggle Latch Output
	67	I	P3.2 CAPIN GPT2 Register CAPREL Capture Input
	68	O	P3.3 T3OUT GPT1 Timer T3 Toggle Latch Output
	69	I	P3.4 T3EUD GPT1 Timer T3 Ext.Up/Down Ctrl.Input
	70	I	P3.5 T4IN GPT1 Timer T4 Input for Count/Gate/Reload/Capture
	73	I	P3.6 T3IN GPT1 Timer T3 Count/Gate Input
	74	I	P3.7 T2IN GPT1 Timer T2 Input for Count/Gate/Reload/Capture
	75	I/O	P3.8 MRST SSC Master-Rec./Slave-Transmit I/O
	76	I/O	P3.9 MTSR SSC Master-Transmit/Slave-Rec. O/I
	77	O	P3.10 TxD0 ASC0 Clock/Data Output (Asyn./Syn.)
	78	I/O	P3.11 RxD0 ASC0 Data Input (Asyn.) or I/O (Syn.)
	79	O	P3.12 $\overline{\text{BHE}}$ Ext. Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$ Ext. Memory High Byte Write Strobe
	80	I/O	P3.13 SCLK SSC Master Clock Outp./Slave Cl. Inp.
	81	O	P3.15 CLKOUT System Clock Output (=CPU Clock)
P4.0 - P4.7	85 - 92	I/O	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 4 can be used to output the segment address lines:
	85	O	P4.0 Least Significant Segment Addr. Line

	89	O	P4.4 A16 Least Significant Segment Addr. Line
	90	O	P4.5 A21 Segment Address Line,
		I	CAN_RxD CAN Receive Data Input
	91	O	P4.6 A22 Segment Address Line,
		O	CAN_TxD CAN Transmit Data Output
	92	O	P4.7 A23 Most Significant Segment Addr. Line
$\overline{\text{RD}}$	95	O	External Memory Read Strobe. $\overline{\text{RD}}$ is activated for every external instruction or data read access.

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function																		
$\overline{WR}/\overline{WRL}$	96	O	External Memory Write Strobe. In \overline{WR} -mode this pin is activated for every external data write access. In \overline{WRL} -mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.																		
\overline{READY}	97	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level.																		
ALE	98	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.																		
\overline{EA}	99	I	External Access Enable pin. A low level at this pin during and after Reset forces the C167CR to begin instruction execution out of external memory. A high level forces execution out of the internal ROM. ROMless versions must have this pin tied to '0'.																		
PORT0: P0L.0 - P0L.7, P0H.0 - P0H.7	100 - 107 108, 111-117	I/O	<p>PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state.</p> <p>In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes.</p> <p>Demultiplexed bus modes:</p> <table><tr><td>Data Path Width:</td><td>8-bit</td><td>16-bit</td></tr><tr><td>P0L.0 - P0L.7:</td><td>D0 - D7</td><td>D0 - D7</td></tr><tr><td>P0H.0 - P0H.7:</td><td>I/O</td><td>D8 - D15</td></tr></table> <p>Multiplexed bus modes:</p> <table><tr><td>Data Path Width:</td><td>8-bit</td><td>16-bit</td></tr><tr><td>P0L.0 - P0L.7:</td><td>AD0 - AD7</td><td>AD0 - AD7</td></tr><tr><td>P0H.0 - P0H.7:</td><td>A8 - A15</td><td>AD8 - AD15</td></tr></table>	Data Path Width:	8-bit	16-bit	P0L.0 - P0L.7:	D0 - D7	D0 - D7	P0H.0 - P0H.7:	I/O	D8 - D15	Data Path Width:	8-bit	16-bit	P0L.0 - P0L.7:	AD0 - AD7	AD0 - AD7	P0H.0 - P0H.7:	A8 - A15	AD8 - AD15
Data Path Width:	8-bit	16-bit																			
P0L.0 - P0L.7:	D0 - D7	D0 - D7																			
P0H.0 - P0H.7:	I/O	D8 - D15																			
Data Path Width:	8-bit	16-bit																			
P0L.0 - P0L.7:	AD0 - AD7	AD0 - AD7																			
P0H.0 - P0H.7:	A8 - A15	AD8 - AD15																			

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function
PORT1: P1L.0 - P1L.7, P1H.0 - P1H.7	118 - 125 128 - 135	I/O	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. The following PORT1 pins also serve for alternate functions: P1H.4 CC24IO CAPCOM2: CC24 Capture Input P1H.5 CC25IO CAPCOM2: CC25 Capture Input P1H.6 CC26IO CAPCOM2: CC26 Capture Input P1H.7 CC27IO CAPCOM2: CC27 Capture Input
XTAL1	138	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator
XTAL2	137	O	XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
$\overline{\text{RSTIN}}$	140	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the C167CR. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS} .
$\overline{\text{RSTOUT}}$	141	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	142	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C167CR to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
V_{AREF}	37	—	Reference voltage for the A/D converter.
V_{AGND}	38	—	Reference ground for the A/D converter.
V_{PP}	84	—	Flash programming voltage. This pin accepts the programming voltage for flash versions of the C167CR. Note: This pin is not connected (NC) on non-flash versions.

Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Input (I) Output (O)	Function
V_{CC}	17, 46, 56, 72, 82, 93, 109, 126, 136, 144	—	Digital Supply Voltage: + 5 V during normal operation and idle mode. ≥ 2.5 V during power down mode.
V_{SS}	18, 45, 55, 71, 83, 94, 110, 127, 139, 143	—	Digital Ground.

Functional Description

The architecture of the C167CR combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C167CR.

Note: All time specifications refer to a CPU clock of 20 MHz (see definition in the AC Characteristics section).

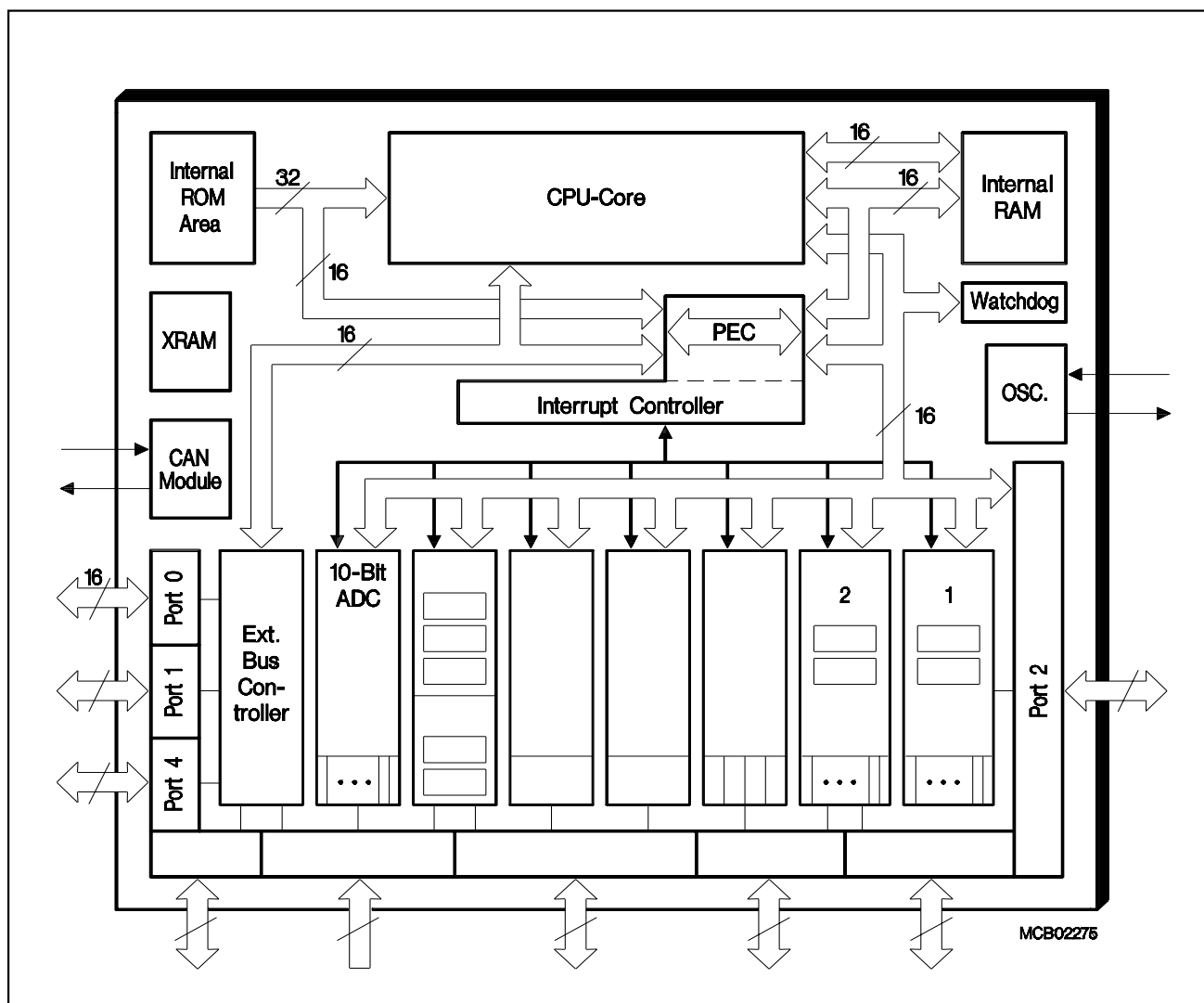


Figure 3 Block Diagram

Memory Organization

The memory space of the C167CR is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed byte-wise or word-wise. Particular portions of the on-chip memory have additionally been made directly bit-addressable.

The C167CR is prepared to incorporate on-chip mask-programmable ROM or Flash Memory for code or constant data. Currently no ROM is integrated.

2 KBytes of on-chip Internal RAM are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C16x family.

2 KBytes of on-chip Extension RAM (XRAM) are provided to store user data, user stacks or code. The XRAM is accessed like external memory and therefore cannot be used for the system stack or for register banks and is not bit-addressable. The XRAM allows 16-bit accesses with maximum speed.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories. In addition, different address ranges may be accessed with different bus characteristics. Up to 5 external \overline{CS} signals can be generated in order to save external glue logic. Access to very slow memories is supported via a particular 'Ready' function. A $\overline{HOLD}/HLDA$ protocol is available for bus arbitration.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte or to 64 KByte. In this case Port 4 outputs four, two or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C167CR's instructions can be executed in just one machine cycle which requires 100 ns at 20-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16×16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

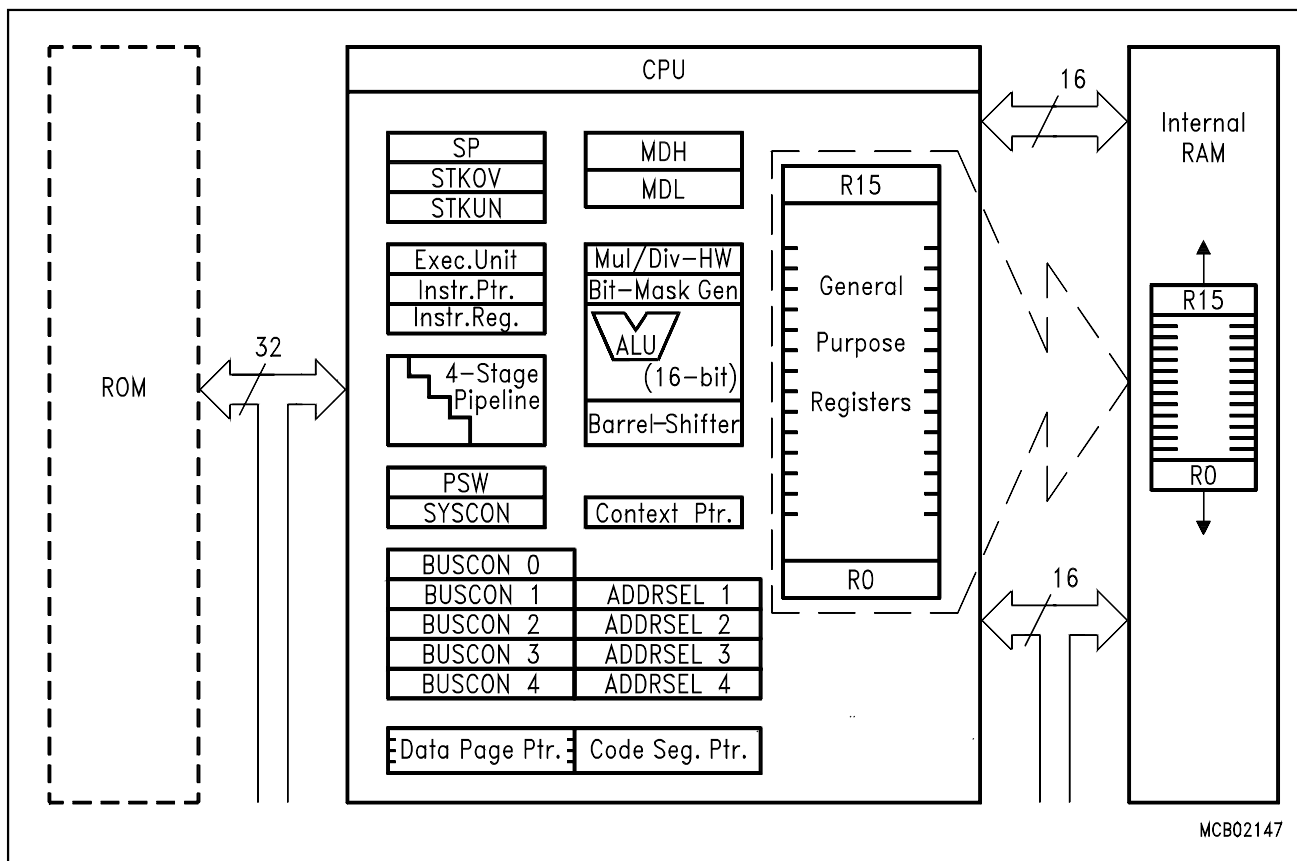


Figure 4
CPU Block Diagram

The CPU disposes of an actual register context consisting of up to 16 wordwide GPRs which are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at a time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 2048 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C167CR instruction set which includes the following instruction classes:

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 250 ns to 600 ns (in case of internal program execution), the C167CR is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C167CR supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C167CR has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

The following table shows all of the possible C167CR interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Note: Three nodes in the table (X-Peripheral nodes) are prepared to accept interrupt requests from integrated X-Bus peripherals. Nodes, where no X-Peripherals are connected, may be used to generate software controlled interrupt requests by setting the respective XPNIR bit.

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	00'0040 _H	10 _H
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	00'0044 _H	11 _H
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	00'0048 _H	12 _H
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	00'004C _H	13 _H
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	00'0050 _H	14 _H
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	00'0054 _H	15 _H
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	00'0058 _H	16 _H
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	00'005C _H	17 _H
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	00'0060 _H	18 _H
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	00'0064 _H	19 _H
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	00'0068 _H	1A _H
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	00'006C _H	1B _H
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	00'0070 _H	1C _H
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	00'0074 _H	1D _H
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	00'0078 _H	1E _H
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	00'007C _H	1F _H
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	00'00C0 _H	30 _H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	00'00C4 _H	31 _H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	00'00C8 _H	32 _H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	00'00CC _H	33 _H
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	00'00D0 _H	34 _H
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	00'00D4 _H	35 _H
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	00'00D8 _H	36 _H
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	00'00DC _H	37 _H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	00'00E0 _H	38 _H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	00'00E4 _H	39 _H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	00'00E8 _H	3A _H
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	00'00EC _H	3B _H
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	00'00E0 _H	3C _H
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	00'0110 _H	44 _H
CAPCOM Register 30	CC30IR	CC30IE	CC30INT	00'0114 _H	45 _H
CAPCOM Register 31	CC31IR	CC31IE	CC31INT	00'0118 _H	46 _H
CAPCOM Timer 0	T0IR	T0IE	T0INT	00'0080 _H	20 _H

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Timer 1	T1IR	T1IE	T1INT	00'0084 _H	21 _H
CAPCOM Timer 7	T7IR	T7IE	T7INT	00'00F4 _H	3D _H
CAPCOM Timer 8	T8IR	T8IE	T8INT	00'00F8 _H	3E _H
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088 _H	22 _H
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008C _H	23 _H
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090 _H	24 _H
GPT2 Timer 5	T5IR	T5IE	T5INT	00'0094 _H	25 _H
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098 _H	26 _H
GPT2 CAPREL Register	CRIR	CRIE	CRINT	00'009C _H	27 _H
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	00'00A0 _H	28 _H
A/D Overrun Error	ADEIR	ADEIE	ADEINT	00'00A4 _H	29 _H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8 _H	2A _H
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011C _H	47 _H
ASC0 Receive	S0RIR	S0RIE	S0RINT	00'00AC _H	2B _H
ASC0 Error	S0EIR	S0EIE	S0EINT	00'00B0 _H	2C _H
SSC Transmit	SCTIR	SCTIE	SCTINT	00'00B4 _H	2D _H
SSC Receive	SCRIR	SCRIE	SCRINT	00'00B8 _H	2E _H
SSC Error	SCEIR	SCEIE	SCEINT	00'00BC _H	2F _H
PWM Channel 0...3	PWMIR	PWMIE	PWMINT	00'00FC _H	3F _H
CAN Interface	XP0IR	XP0IE	XP0INT	00'0100 _H	40 _H
X-Peripheral Node	XP1IR	XP1IE	XP1INT	00'0104 _H	41 _H
X-Peripheral Node	XP2IR	XP2IE	XP2INT	00'0108 _H	42 _H
PLL Unlock	XP3IR	XP3IE	XP3INT	00'010C _H	43 _H

The C167CR also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: Hardware Reset Software Reset Watchdog Timer Overflow		RESET RESET RESET	00'0000 _H 00'0000 _H 00'0000 _H	00 _H 00 _H 00 _H	III III III
Class A Hardware Traps: Non-Maskable Interrupt Stack Overflow Stack Underflow	NMI STKOF STKUF	NMITRAP STOTRAP STUTRAP	00'0008 _H 00'0010 _H 00'0018 _H	02 _H 04 _H 06 _H	II II II
Class B Hardware Traps: Undefined Opcode Protected Instruction Fault Illegal Word Operand Access Illegal Instruction Access Illegal External Bus Access	UNDOPC PRTFLT ILLOPA ILLINA ILLBUS	BTRAP BTRAP BTRAP BTRAP	00'0028 _H 00'0028 _H 00'0028 _H 00'0028 _H	0A _H 0A _H 0A _H 0A _H	I I I I
Reserved			[2C _H – 3C _H]	[0B _H – 0F _H]	
Software Traps TRAP Instruction			Any [00'0000 _H – 00'01FC _H] in steps of 4 _H	Any [00 _H – 7F _H]	Current CPU Priority

Capture/Compare (CAPCOM) Units

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 400 ns (at 20-MHz system clock). The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function. Each register has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin (except for CC24...CC27) to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('capture'd) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare time overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible.

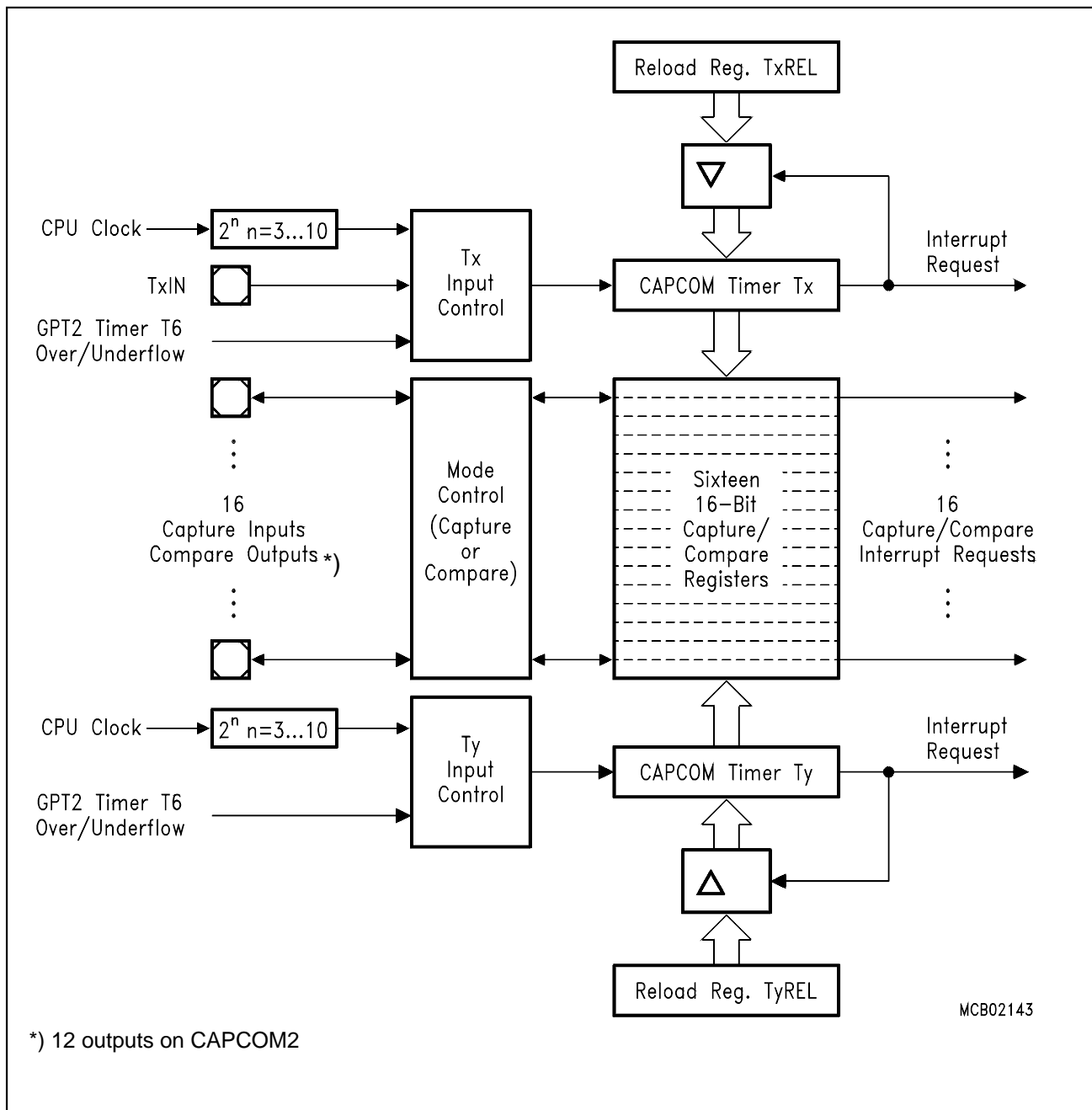


Figure 5
CAPCOM Unit Block Diagram

PWM Module

The Pulse Width Modulation Module can generate up to four PWM output signals using edge-aligned or center-aligned PWM. In addition the PWM module can generate PWM burst signals and single shot outputs. The frequency range of the PWM signals covers 4.8 Hz to 1 MHz (referred to a CPU clock of 20 MHz), depending on the resolution of the PWM output signal. The level of the output signals is selectable and the PWM module can generate interrupt requests.

General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of module GPT1 can be configured individually for one of three basic modes of operation, which are Timer, Gated Timer, and Counter Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 400 ns (@ 20-MHz CPU clock).

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e. g. position tracking.

Timers T3 and T4 have output toggle latches (TxOTL) which change their state on each timer overflow/underflow. The state of these latches may be output on port pins (TxOUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

With its maximum resolution of 200 ns (@ 20 MHz), the GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

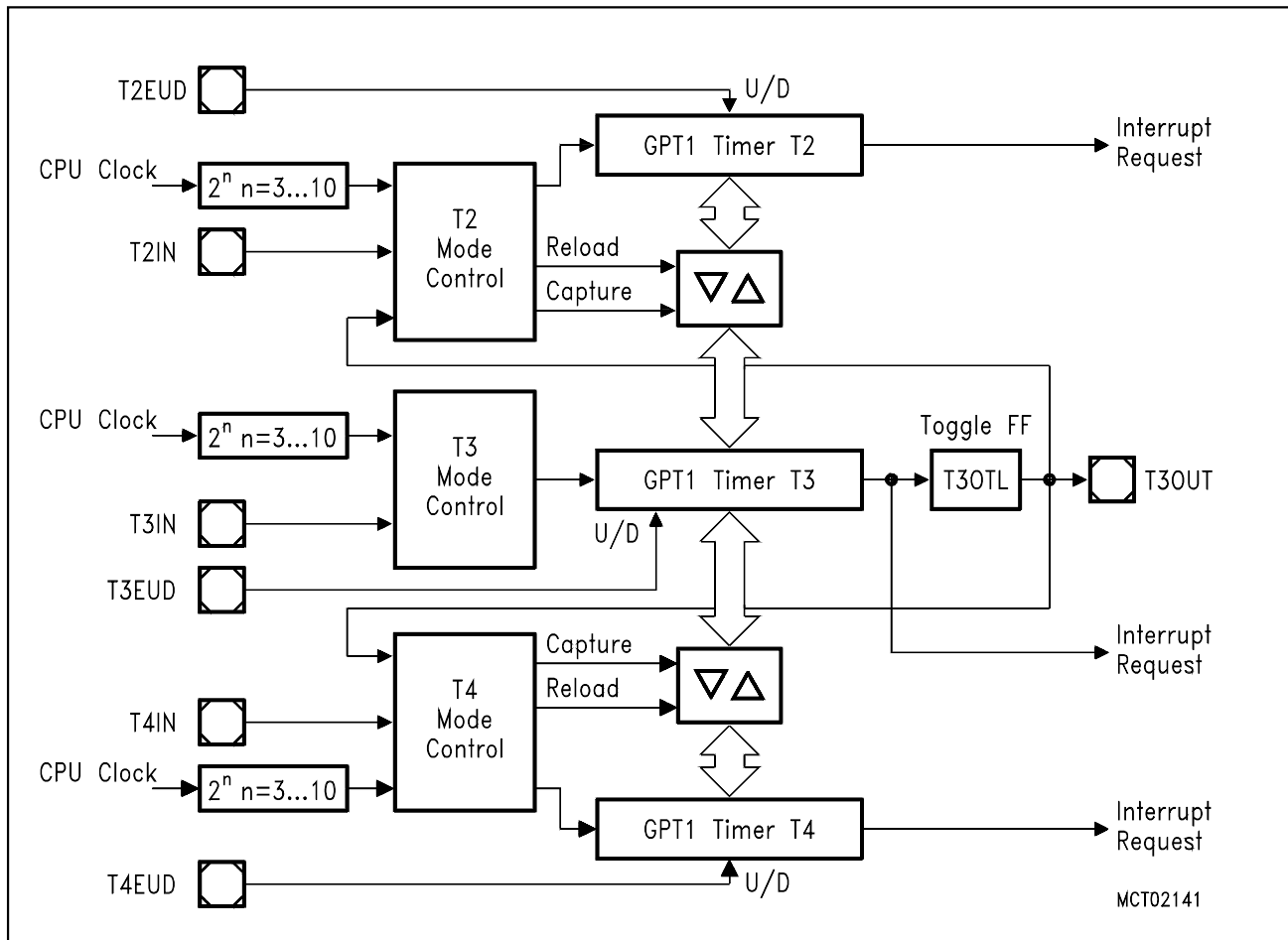


Figure 6
Block Diagram of GPT1

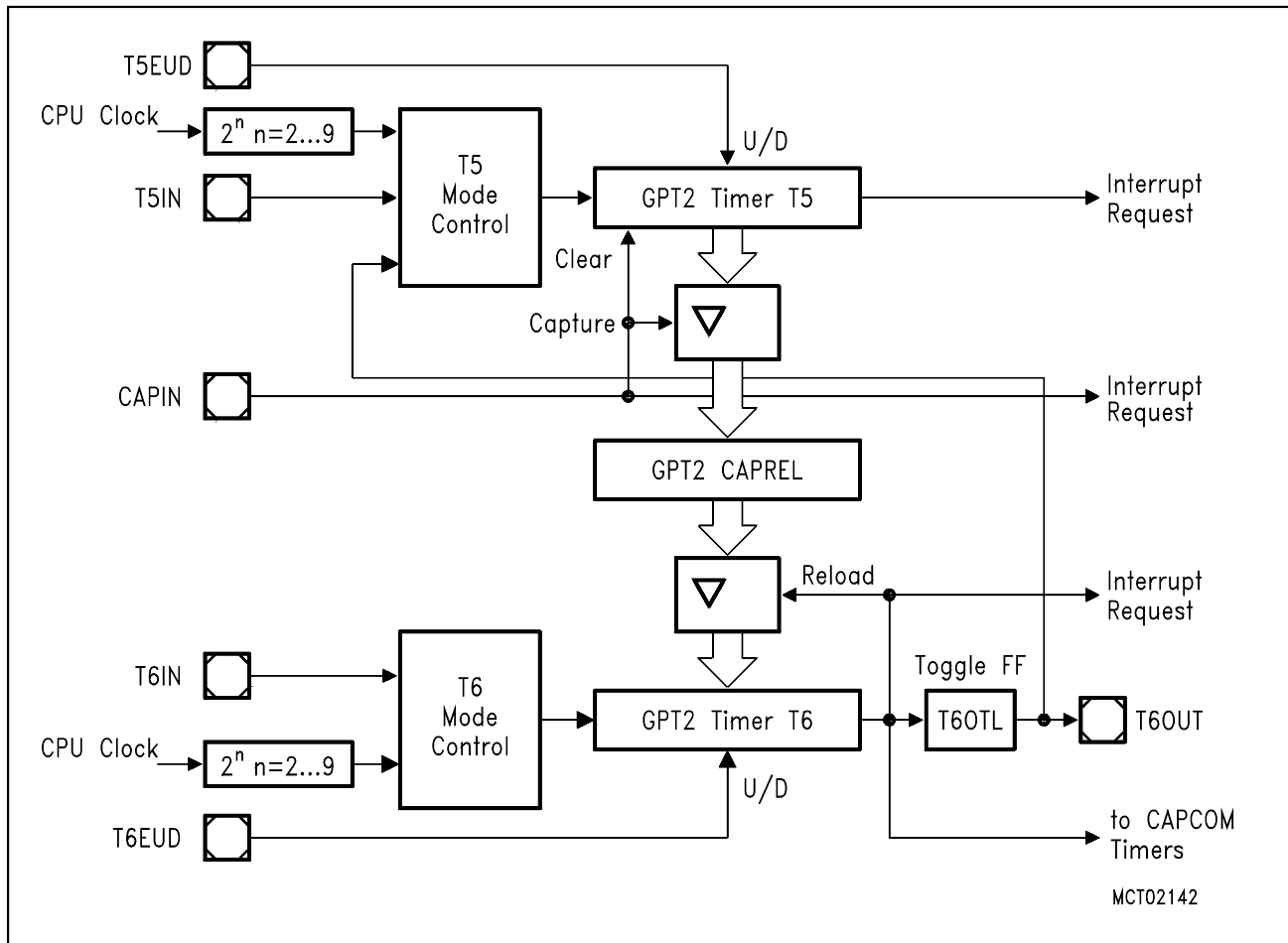


Figure 7
Block Diagram of GPT2

Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 25 μs and 420 ms can be monitored (@ 20 MHz). The default Watchdog Timer interval after reset is 6.55 ms (@ 20 MHz).

A/D Converter

For analog signal measurement, a 10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable and can so be adjusted to the external circuitry.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less than 16 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the C167CR supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the number of prespecified channels is repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (ASC0) and a High-Speed Synchronous Serial Channel (SSC).

ASC0 is upward compatible with the serial ports of the Siemens SAB 8051x microcontroller family and support full-duplex asynchronous communication up to 625 KBaud and half-duplex synchronous communication up to 2.5 Mbaud on the @ 20-MHz system clock.

The SSC allows half duplex synchronous communication up to 5 Mbaud @ 20-MHz system clock.

Two dedicated baud rate generators allow to set up all standard baud rates without oscillator tuning. For transmission, reception, and erroneous reception 3 separate interrupt vectors are provided for each serial channel.

In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode).

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The SSC transmits or receives characters of 2...16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB, while the ASC0 always shifts the LSB first.

A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

CAN-Module

The integrated CAN-Module handles the completely autonomous transmission and reception of CAN frames in accordance with the CAN specification V2.0 part B (active), i.e. the on-chip CAN-Module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

The module provides Full CAN functionality on up to 15 message objects. Message object 15 may be configured for Basic CAN functionality. Both modes provide separate masks for acceptance filtering which allows to accept a number of identifiers in Full CAN mode and also allows to disregard a number of identifiers in Basic CAN mode. All message objects can be updated independent from the other objects and are equipped for the maximum message length of 8 bytes.

The bit timing is derived from the XCLK and is programmable up to a data rate of 1 MBaud. The CAN-Module uses two pins to interface to a bus transceiver.

Parallel Ports

The C167CR provides up to 111 I/O lines which are organized into eight input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of five I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The input threshold of Port 2, Port 3, Port 7 and Port 8 is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17...A16 in systems where segmentation is enabled to access more than 64 KBytes of memory.

Port 2, Port 8 and Port 7 are associated with the capture inputs or compare outputs of the CAPCOM units and/or with the outputs of the PWM module.

Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals.

Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$ and the system clock output (CLKOUT).

Port 5 is used for the analog input channels to the A/D converter or timer control signals.

All port lines that are not used for these alternate functions may be used as general purpose IO lines.

Instruction Set Summary

The table below lists the instructions of the C167CR in a condensed way. The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the “**C16x Family Instruction Set Manual**”.

This document also provides a detailed description of each instruction.

Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand. with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$ -pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on RSTOUT-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

Special Function Registers Overview

The following table lists all SFRs which are implemented in the C167CR in alphabetical order.

Bit-addressable SFRs are marked with the letter “b” in column “Name”. SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter “E” in column “Physical Address”.

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Special Function Registers Overview

Name		Physical Address	8-Bit Address	Description	Reset Value
ADCIC	b	FF98 _H	CC _H	A/D Converter End of Conversion Interrupt Control Register	0000 _H
ADCON	b	FFA0 _H	D0 _H	A/D Converter Control Register	0000 _H
ADDAT		FEA0 _H	50 _H	A/D Converter Result Register	0000 _H
ADDAT2		F0A0 _H E	50 _H	A/D Converter 2 Result Register	0000 _H
ADDRSEL1		FE18 _H	0C _H	Address Select Register 1	0000 _H
ADDRSEL2		FE1A _H	0D _H	Address Select Register 2	0000 _H
ADDRSEL3		FE1C _H	0E _H	Address Select Register 3	0000 _H
ADDRSEL4		FE1E _H	0F _H	Address Select Register 4	0000 _H
ADEIC	b	FF9A _H	CD _H	A/D Converter Overrun Error Interrupt Control Register	0000 _H
BUSCON0	b	FF0C _H	86 _H	Bus Configuration Register 0	0XX0 _H
BUSCON1	b	FF14 _H	8A _H	Bus Configuration Register 1	0000 _H
BUSCON2	b	FF16 _H	8B _H	Bus Configuration Register 2	0000 _H
BUSCON3	b	FF18 _H	8C _H	Bus Configuration Register 3	0000 _H
BUSCON4	b	FF1A _H	8D _H	Bus Configuration Register 4	0000 _H
CAPREL		FE4A _H	25 _H	GPT2 Capture/Reload Register	0000 _H
CC0		FE80 _H	40 _H	CAPCOM Register 0	0000 _H
CC0IC	b	FF78 _H	BC _H	CAPCOM Register 0 Interrupt Control Register	0000 _H
CC1		FE82 _H	41 _H	CAPCOM Register 1	0000 _H
CC1IC	b	FF7A _H	BD _H	CAPCOM Register 1 Interrupt Control Register	0000 _H
CC2		FE84 _H	42 _H	CAPCOM Register 2	0000 _H
CC2IC	b	FF7C _H	BE _H	CAPCOM Register 2 Interrupt Control Register	0000 _H

Special Function Registers Overview (cont'd)

Name		Physical Address	8-Bit Address	Description	Reset Value
CC3		FE86 _H	43 _H	CAPCOM Register 3	0000 _H
CC3IC	b	FF7E _H	BF _H	CAPCOM Register 3 Interrupt Control Register	0000 _H
CC4		FE88 _H	44 _H	CAPCOM Register 4	0000 _H
CC4IC	b	FF80 _H	C0 _H	CAPCOM Register 4 Interrupt Control Register	0000 _H
CC5		FE8A _H	45 _H	CAPCOM Register 5	0000 _H
CC5IC	b	FF82 _H	C1 _H	CAPCOM Register 5 Interrupt Control Register	0000 _H
CC6		FE8C _H	46 _H	CAPCOM Register 6	0000 _H
CC6IC	b	FF84 _H	C2 _H	CAPCOM Register 6 Interrupt Control Register	0000 _H
CC7		FE8E _H	47 _H	CAPCOM Register 7	0000 _H
CC7IC	b	FF86 _H	C3 _H	CAPCOM Register 7 Interrupt Control Register	0000 _H
CC8		FE90 _H	48 _H	CAPCOM Register 8	0000 _H
CC8IC	b	FF88 _H	C4 _H	CAPCOM Register 8 Interrupt Control Register	0000 _H
CC9		FE92 _H	49 _H	CAPCOM Register 9	0000 _H
CC9IC	b	FF8A _H	C5 _H	CAPCOM Register 9 Interrupt Control Register	0000 _H
CC10		FE94 _H	4A _H	CAPCOM Register 10	0000 _H
CC10IC	b	FF8C _H	C6 _H	CAPCOM Register 10 Interrupt Control Register	0000 _H
CC11		FE96 _H	4B _H	CAPCOM Register 11	0000 _H
CC11IC	b	FF8E _H	C7 _H	CAPCOM Register 11 Interrupt Control Register	0000 _H
CC12		FE98 _H	4C _H	CAPCOM Register 12	0000 _H
CC12IC	b	FF90 _H	C8 _H	CAPCOM Register 12 Interrupt Control Register	0000 _H
CC13		FE9A _H	4D _H	CAPCOM Register 13	0000 _H
CC13IC	b	FF92 _H	C9 _H	CAPCOM Register 13 Interrupt Control Register	0000 _H
CC14		FE9C _H	4E _H	CAPCOM Register 14	0000 _H
CC14IC	b	FF94 _H	CA _H	CAPCOM Register 14 Interrupt Control Register	0000 _H
CC15		FE9E _H	4F _H	CAPCOM Register 15	0000 _H
CC15IC	b	FF96 _H	CB _H	CAPCOM Register 15 Interrupt Control Register	0000 _H
CC16		FE60 _H	30 _H	CAPCOM Register 16	0000 _H
CC16IC	b	F160 _H E	B0 _H	CAPCOM Register 16 Interrupt Control Register	0000 _H
CC17		FE62 _H	31 _H	CAPCOM Register 17	0000 _H

Special Function Registers Overview (cont'd)

Name		Physical Address	8-Bit Address	Description	Reset Value
CC17IC	b	F162 _H	E B1 _H	CAPCOM Register 17 Interrupt Control Register	0000 _H
CC18		FE64 _H	32 _H	CAPCOM Register 18	0000 _H
CC18IC	b	F164 _H	E B2 _H	CAPCOM Register 18 Interrupt Control Register	0000 _H
CC19		FE66 _H	33 _H	CAPCOM Register 19	0000 _H
CC19IC	b	F166 _H	E B3 _H	CAPCOM Register 19 Interrupt Control Register	0000 _H
CC20		FE68 _H	34 _H	CAPCOM Register 20	0000 _H
CC20IC	b	F168 _H	E B4 _H	CAPCOM Register 20 Interrupt Control Register	0000 _H
CC21		FE6A _H	35 _H	CAPCOM Register 21	0000 _H
CC21IC	b	F16A _H	E B5 _H	CAPCOM Register 21 Interrupt Control Register	0000 _H
CC22		FE6C _H	36 _H	CAPCOM Register 22	0000 _H
CC22IC	b	F16C _H	E B6 _H	CAPCOM Register 22 Interrupt Control Register	0000 _H
CC23		FE6E _H	37 _H	CAPCOM Register 23	0000 _H
CC23IC	b	F16E _H	E B7 _H	CAPCOM Register 23 Interrupt Control Register	0000 _H
CC24		FE70 _H	38 _H	CAPCOM Register 24	0000 _H
CC24IC	b	F170 _H	E B8 _H	CAPCOM Register 24 Interrupt Control Register	0000 _H
CC25		FE72 _H	39 _H	CAPCOM Register 25	0000 _H
CC25IC	b	F172 _H	E B9 _H	CAPCOM Register 25 Interrupt Control Register	0000 _H
CC26		FE74 _H	3A _H	CAPCOM Register 26	0000 _H
CC26IC	b	F174 _H	E BA _H	CAPCOM Register 26 Interrupt Control Register	0000 _H
CC27		FE76 _H	3B _H	CAPCOM Register 27	0000 _H
CC27IC	b	F176 _H	E BB _H	CAPCOM Register 27 Interrupt Control Register	0000 _H
CC28		FE78 _H	3C _H	CAPCOM Register 28	0000 _H
CC28IC	b	F178 _H	E BC _H	CAPCOM Register 28 Interrupt Control Register	0000 _H
CC29		FE7A _H	3D _H	CAPCOM Register 29	0000 _H
CC29IC	b	F184 _H	E C2 _H	CAPCOM Register 29 Interrupt Control Register	0000 _H
CC30		FE7C _H	3E _H	CAPCOM Register 30	0000 _H
CC30IC	b	F18C _H	E C6 _H	CAPCOM Register 30 Interrupt Control Register	0000 _H
CC31		FE7E _H	3F _H	CAPCOM Register 31	0000 _H
CC31IC	b	F194 _H	E CA _H	CAPCOM Register 31 Interrupt Control Register	0000 _H

Special Function Registers Overview (cont'd)

Name	Physical Address	8-Bit Address	Description	Reset Value
CCM0	b FF52 _H	A9 _H	CAPCOM Mode Control Register 0	0000 _H
CCM1	b FF54 _H	AA _H	CAPCOM Mode Control Register 1	0000 _H
CCM2	b FF56 _H	AB _H	CAPCOM Mode Control Register 2	0000 _H
CCM3	b FF58 _H	AC _H	CAPCOM Mode Control Register 3	0000 _H
CCM4	b FF22 _H	91 _H	CAPCOM Mode Control Register 4	0000 _H
CCM5	b FF24 _H	92 _H	CAPCOM Mode Control Register 5	0000 _H
CCM6	b FF26 _H	93 _H	CAPCOM Mode Control Register 6	0000 _H
CCM7	b FF28 _H	94 _H	CAPCOM Mode Control Register 7	0000 _H
CP	FE10 _H	08 _H	CPU Context Pointer Register	FC00 _H
CRIC	b FF6A _H	B5 _H	GPT2 CAPREL Interrupt Control Register	0000 _H
CSP	FE08 _H	04 _H	CPU Code Segment Pointer Register (read only)	0000 _H
DP0L	b F100 _H E	80 _H	P0L Direction Control Register	00 _H
DP0H	b F102 _H E	81 _H	P0H Direction Control Register	00 _H
DP1L	b F104 _H E	82 _H	P1L Direction Control Register	00 _H
DP1H	b F106 _H E	83 _H	P1H Direction Control Register	00 _H
DP2	b FFC2 _H	E1 _H	Port 2 Direction Control Register	0000 _H
DP3	b FFC6 _H	E3 _H	Port 3 Direction Control Register	0000 _H
DP4	b FFCA _H	E5 _H	Port 4 Direction Control Register	00 _H
DP6	b FFCE _H	E7 _H	Port 6 Direction Control Register	00 _H
DP7	b FFD2 _H	E9 _H	Port 7 Direction Control Register	00 _H
DP8	b FFD6 _H	EB _H	Port 8 Direction Control Register	00 _H
DPP0	FE00 _H	00 _H	CPU Data Page Pointer 0 Register (10 bits)	0000 _H
DPP1	FE02 _H	01 _H	CPU Data Page Pointer 1 Register (10 bits)	0001 _H
DPP2	FE04 _H	02 _H	CPU Data Page Pointer 2 Register (10 bits)	0002 _H
DPP3	FE06 _H	03 _H	CPU Data Page Pointer 3 Register (10 bits)	0003 _H
EXICON	b F1C0 _H E	E0 _H	External Interrupt Control Register	0000 _H
MDC	b FF0E _H	87 _H	CPU Multiply Divide Control Register	0000 _H
MDH	FE0C _H	06 _H	CPU Multiply Divide Register – High Word	0000 _H
MDL	FE0E _H	07 _H	CPU Multiply Divide Register – Low Word	0000 _H

Special Function Registers Overview (cont'd)

Name		Physical Address	8-Bit Address	Description	Reset Value
ODP2	b	F1C2 _H	E E1 _H	Port 2 Open Drain Control Register	0000 _H
ODP3	b	F1C6 _H	E E3 _H	Port 3 Open Drain Control Register	0000 _H
ODP6	b	F1CE _H	E E7 _H	Port 6 Open Drain Control Register	00 _H
ODP7	b	F1D2 _H	E E9 _H	Port 7 Open Drain Control Register	00 _H
ODP8	b	F1D6 _H	E EB _H	Port 8 Open Drain Control Register	00 _H
ONES		FF1E _H	8F _H	Constant Value 1's Register (read only)	FFFF _H
P0L	b	FF00 _H	80 _H	Port 0 Low Register (Lower half of PORT0)	00 _H
P0H	b	FF02 _H	81 _H	Port 0 High Register (Upper half of PORT0)	00 _H
P1L	b	FF04 _H	82 _H	Port 1 Low Register (Lower half of PORT1)	00 _H
P1H	b	FF06 _H	83 _H	Port 1 High Register (Upper half of PORT1)	00 _H
P2	b	FFC0 _H	E0 _H	Port 2 Register	0000 _H
P3	b	FFC4 _H	E2 _H	Port 3 Register	0000 _H
P4	b	FFC8 _H	E4 _H	Port 4 Register (8 bits)	00 _H
P5	b	FFA2 _H	D1 _H	Port 5 Register (read only)	XXXX _H
P6	b	FFCC _H	E6 _H	Port 6 Register (8 bits)	00 _H
P7	b	FFD0 _H	E8 _H	Port 7 Register (8 bits)	00 _H
P8	b	FFD4 _H	EA _H	Port 8 Register (8 bits)	00 _H
PECC0		FEC0 _H	60 _H	PEC Channel 0 Control Register	0000 _H
PECC1		FEC2 _H	61 _H	PEC Channel 1 Control Register	0000 _H
PECC2		FEC4 _H	62 _H	PEC Channel 2 Control Register	0000 _H
PECC3		FEC6 _H	63 _H	PEC Channel 3 Control Register	0000 _H
PECC4		FEC8 _H	64 _H	PEC Channel 4 Control Register	0000 _H
PECC5		FECA _H	65 _H	PEC Channel 5 Control Register	0000 _H
PECC6		FECC _H	66 _H	PEC Channel 6 Control Register	0000 _H
PECC7		FECE _H	67 _H	PEC Channel 7 Control Register	0000 _H
PICON		F1C4 _H	E E2 _H	Port Input Threshold Control Register	0000 _H
PP0		F038 _H	E 1C _H	PWM Module Period Register 0	0000 _H
PP1		F03A _H	E 1D _H	PWM Module Period Register 1	0000 _H
PP2		F03C _H	E 1E _H	PWM Module Period Register 2	0000 _H

Special Function Registers Overview (cont'd)

Name	Physical Address	8-Bit Address	Description	Reset Value
PP3	F03E _H E	1F _H	PWM Module Period Register 3	0000 _H
PSW b	FF10 _H	88 _H	CPU Program Status Word	0000 _H
PT0	F030 _H E	18 _H	PWM Module Up/Down Counter 0	0000 _H
PT1	F032 _H E	19 _H	PWM Module Up/Down Counter 1	0000 _H
PT2	F034 _H E	1A _H	PWM Module Up/Down Counter 2	0000 _H
PT3	F036 _H E	1B _H	PWM Module Up/Down Counter 3	0000 _H
PW0	FE30 _H	18 _H	PWM Module Pulse Width Register 0	0000 _H
PW1	FE32 _H	19 _H	PWM Module Pulse Width Register 1	0000 _H
PW2	FE34 _H	1A _H	PWM Module Pulse Width Register 2	0000 _H
PW3	FE36 _H	1B _H	PWM Module Pulse Width Register 3	0000 _H
PWMCON0 b	FF30 _H	98 _H	PWM Module Control Register 0	0000 _H
PWMCON1 b	FF32 _H	99 _H	PWM Module Control Register 1	0000 _H
PWMIC b	F17E _H E	BF _H	PWM Module Interrupt Control Register	0000 _H
RP0H b	F108 _H E	84 _H	System Startup Configuration Register (Rd. only)	XX _H
S0BG	FEB4 _H	5A _H	Serial Channel 0 Baud Rate Generator Reload Register	0000 _H
S0CON b	FFB0 _H	D8 _H	Serial Channel 0 Control Register	0000 _H
S0EIC b	FF70 _H	B8 _H	Serial Channel 0 Error Interrupt Control Register	0000 _H
S0RBUF	FEB2 _H	59 _H	Serial Channel 0 Receive Buffer Register (read only)	XX _H
S0RIC b	FF6E _H	B7 _H	Serial Channel 0 Receive Interrupt Control Register	0000 _H
S0TBIC b	F19C _H E	CE _H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000 _H
S0TBUF	FEB0 _H	58 _H	Serial Channel 0 Transmit Buffer Register (write only)	00 _H
S0TIC b	FF6C _H	B6 _H	Serial Channel 0 Transmit Interrupt Control Register	0000 _H
SP	FE12 _H	09 _H	CPU System Stack Pointer Register	FC00 _H
SSCBR	F0B4 _H E	5A _H	SSC Baudrate Register	0000 _H
SSCCON b	FFB2 _H	D9 _H	SSC Control Register	0000 _H

Special Function Registers Overview (cont'd)

Name		Physical Address	8-Bit Address	Description	Reset Value
SSCEIC	b	FF76 _H	BB _H	SSC Error Interrupt Control Register	0000 _H
SSCRB		F0B2 _H	E 59 _H	SSC Receive Buffer (read only)	XXXX _H
SSCRIC	b	FF74 _H	BA _H	SSC Receive Interrupt Control Register	0000 _H
SSCTB		F0B0 _H	E 58 _H	SSC Transmit Buffer (write only)	0000 _H
SSCTIC	b	FF72 _H	B9 _H	SSC Transmit Interrupt Control Register	0000 _H
STKOV		FE14 _H	0A _H	CPU Stack Overflow Pointer Register	FA00 _H
STKUN		FE16 _H	0B _H	CPU Stack Underflow Pointer Register	FC00 _H
SYSCON	b	FF12 _H	89 _H	CPU System Configuration Register	0xx0 _H ¹⁾
T0		FE50 _H	28 _H	CAPCOM Timer 0 Register	0000 _H
T01CON	b	FF50 _H	A8 _H	CAPCOM Timer 0 and Timer 1 Control Register	0000 _H
T0IC	b	FF9C _H	CE _H	CAPCOM Timer 0 Interrupt Control Register	0000 _H
T0REL		FE54 _H	2A _H	CAPCOM Timer 0 Reload Register	0000 _H
T1		FE52 _H	29 _H	CAPCOM Timer 1 Register	0000 _H
T1IC	b	FF9E _H	CF _H	CAPCOM Timer 1 Interrupt Control Register	0000 _H
T1REL		FE56 _H	2B _H	CAPCOM Timer 1 Reload Register	0000 _H
T2		FE40 _H	20 _H	GPT1 Timer 2 Register	0000 _H
T2CON	b	FF40 _H	A0 _H	GPT1 Timer 2 Control Register	0000 _H
T2IC	b	FF60 _H	B0 _H	GPT1 Timer 2 Interrupt Control Register	0000 _H
T3		FE42 _H	21 _H	GPT1 Timer 3 Register	0000 _H
T3CON	b	FF42 _H	A1 _H	GPT1 Timer 3 Control Register	0000 _H
T3IC	b	FF62 _H	B1 _H	GPT1 Timer 3 Interrupt Control Register	0000 _H
T4		FE44 _H	22 _H	GPT1 Timer 4 Register	0000 _H
T4CON	b	FF44 _H	A2 _H	GPT1 Timer 4 Control Register	0000 _H
T4IC	b	FF64 _H	B2 _H	GPT1 Timer 4 Interrupt Control Register	0000 _H
T5		FE46 _H	23 _H	GPT2 Timer 5 Register	0000 _H
T5CON	b	FF46 _H	A3 _H	GPT2 Timer 5 Control Register	0000 _H
T5IC	b	FF66 _H	B3 _H	GPT2 Timer 5 Interrupt Control Register	0000 _H
T6		FE48 _H	24 _H	GPT2 Timer 6 Register	0000 _H
T6CON	b	FF48 _H	A4 _H	GPT2 Timer 6 Control Register	0000 _H

Special Function Registers Overview (cont'd)

Name		Physical Address	8-Bit Address	Description	Reset Value
T6IC	b	FF68 _H	B4 _H	GPT2 Timer 6 Interrupt Control Register	0000 _H
T7		F050 _H	E 28 _H	CAPCOM Timer 7 Register	0000 _H
T78CON	b	FF20 _H	90 _H	CAPCOM Timer 7 and 8 Control Register	0000 _H
T7IC	b	F17A _H	E BE _H	CAPCOM Timer 7 Interrupt Control Register	0000 _H
T7REL		F054 _H	E 2A _H	CAPCOM Timer 7 Reload Register	0000 _H
T8		F052 _H	E 29 _H	CAPCOM Timer 8 Register	0000 _H
T8IC	b	F17C _H	E BF _H	CAPCOM Timer 8 Interrupt Control Register	0000 _H
T8REL		F056 _H	E 2B _H	CAPCOM Timer 8 Reload Register	0000 _H
TFR	b	FFAC _H	D6 _H	Trap Flag Register	0000 _H
WDT		FEAE _H	57 _H	Watchdog Timer Register (read only)	0000 _H
WDTCON		FFAE _H	D7 _H	Watchdog Timer Control Register	000X _H ²⁾
XP0IC	b	F186 _H	E C3 _H	CAN Module Interrupt Control Register	0000 _H
XP1IC	b	F18E _H	E C7 _H	X-Peripheral 1 Interrupt Control Register	0000 _H
XP2IC	b	F196 _H	E CB _H	X-Peripheral 2 Interrupt Control Register	0000 _H
XP3IC	b	F19E _H	E CF _H	PLL Interrupt Control Register	0000 _H
ZEROS	b	FF1C _H	8E _H	Constant Value 0's Register (read only)	0000 _H

1) The system configuration is selected during reset.

2) Bit WDTR indicates a watchdog timer triggered reset.

Note: The Interrupt Control Registers XPnIC are prepared to control interrupt requests from integrated X-Bus peripherals. Nodes, where no X-Peripherals are connected, may be used to generate software controlled interrupt requests by setting the respective XPnIR bit.

Absolute Maximum Ratings

Ambient temperature under bias (T_A):

SAB-C167CR-LM.....0 to + 70 °C

SAF-C167CR-LM.....– 40 to + 85 °C

SAK-C167CR-LM.....– 40 to + 125 °C

Storage temperature (T_{ST}).....– 65 to + 150 °C

Voltage on V_{CC} pins with respect to ground (V_{SS})– 0.5 to + 6.5 V

Voltage on any pin with respect to ground (V_{SS}).....– 0.5 to $V_{CC} + 0.5$ V

Input current on any pin during overload condition– 10 to + 10 mA

Absolute sum of all input currents during overload condition..... |100 mA|

Power dissipation..... 1.5 W

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C167CR and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (Controller Characteristics):

The logic of the C167CR will provide signals with the respective timing characteristics.

SR (System Requirement):

The external system must provide signals with the respective timing characteristics to the C167CR.

DC Characteristics

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$; $f_{CPU} = 20\text{ MHz}$; Reset active
 $T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$ for SAB-C167CR-LM
 $T_A = -40\text{ to }+85\text{ }^{\circ}\text{C}$ for SAF-C167CR-LM
 $T_A = -40\text{ to }+125\text{ }^{\circ}\text{C}$ for SAK-C167CR-LM

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (TTL)	V_{IL} SR	-0.5	$0.2 V_{CC} - 0.1$	V	—
Input low voltage (Special Threshold)	V_{ILS} SR	-0.5	2.0	V	—
Input high voltage, all except \overline{RSTIN} and XTAL1 (TTL)	V_{IH} SR	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V	—
Input high voltage \overline{RSTIN}	V_{IH1} SR	$0.6 V_{CC}$	$V_{CC} + 0.5$	V	—
Input high voltage XTAL1	V_{IH2} SR	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	—
Input high voltage (Special Threshold)	V_{IHS} SR	$0.8 V_{CC} - 0.2$	$V_{CC} + 0.5$	V	—
Input Hysteresis (Special Threshold)	HYS	400	—	mV	—
Output low voltage (PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT, \overline{RSTOUT})	V_{OL} CC	—	0.45	V	$I_{OL} = 2.4\text{ mA}$
Output low voltage (all other outputs)	V_{OL1} CC	—	0.45	V	$I_{OL1} = 1.6\text{ mA}$
Output high voltage (PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT, \overline{RSTOUT})	V_{OH} CC	$0.9 V_{CC}$ 2.4	—	V	$I_{OH} = -500\text{ }\mu\text{A}$ $I_{OH} = -2.4\text{ mA}$
Output high voltage ¹⁾ (all other outputs)	V_{OH1} CC	$0.9 V_{CC}$ 2.4	—	V V	$I_{OH} = -250\text{ }\mu\text{A}$ $I_{OH} = -1.6\text{ mA}$
Input leakage current (Port 5)	I_{OZ1} CC	—	± 200	nA	$0.45\text{ V} < V_{IN} < V_{CC}$
Input leakage current (all other)	I_{OZ2} CC	—	± 500	nA	$0.45\text{ V} < V_{IN} < V_{CC}$
Overload current	I_{OV} SR	—	± 5	mA	5) 8)
\overline{RSTIN} pullup resistor	R_{RST} CC	50	250	k Ω	—
Read/Write inactive current ⁴⁾	I_{RWH} ²⁾	—	-40	μA	$V_{OUT} = 2.4\text{ V}$
Read/Write active current ⁴⁾	I_{RWL} ³⁾	-500	—	μA	$V_{OUT} = V_{OLmax}$
ALE inactive current ⁴⁾	I_{ALEL} ²⁾	—	40	μA	$V_{OUT} = V_{OLmax}$
ALE active current ⁴⁾	I_{ALEH} ³⁾	500	—	μA	$V_{OUT} = 2.4\text{ V}$
Port 6 inactive current ⁴⁾	I_{P6H} ²⁾	—	-40	μA	$V_{OUT} = 2.4\text{ V}$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Port 6 active current ⁴⁾	I_{P6L} ³⁾	– 500	–	μA	$V_{OUT} = V_{OL1max}$
PORT0 configuration current ⁴⁾	I_{P0H} ²⁾	–	– 10	μA	$V_{IN} = V_{IHmin}$
	I_{P0L} ³⁾	– 100	–	μA	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	± 20	μA	$0\text{ V} < V_{IN} < V_{CC}$
Pin capacitance ⁵⁾ (digital inputs/outputs)	C_{IO} CC	–	10	pF	$f = 1\text{ MHz}$ $T_A = 25\text{ °C}$
Power supply current	I_{CC}	–	$20 + 5 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL2}$ f_{CPU} in [MHz] ⁶⁾
Idle mode supply current	I_{ID}	–	$20 + 2 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] ⁶⁾
Power-down mode supply current	I_{PD}	–	100	μA	$V_{CC} = 5.5\text{ V}$ ⁷⁾

Notes

- 1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.
- 2) The maximum current may be drawn while the respective signal line remains inactive.
- 3) The minimum current must be drawn in order to drive the respective signal line active.
- 4) This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected, if they are used for \overline{CS} output and the open drain function is not enabled.
- 5) Not 100 % tested, guaranteed by design characterization.
- 6) The supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{CCmax} and 20 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH} .
- 7) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{CC} - 0.1\text{ V}$ to V_{CC} , $V_{REF} = 0\text{ V}$, all outputs (including pins configured as outputs) disconnected.
- 8) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{CC} + 0.5\text{ V}$ or $V_{OV} < V_{SS} - 0.5\text{ V}$). The absolute sum of input overload currents on all port pins may not exceed **50 mA**.

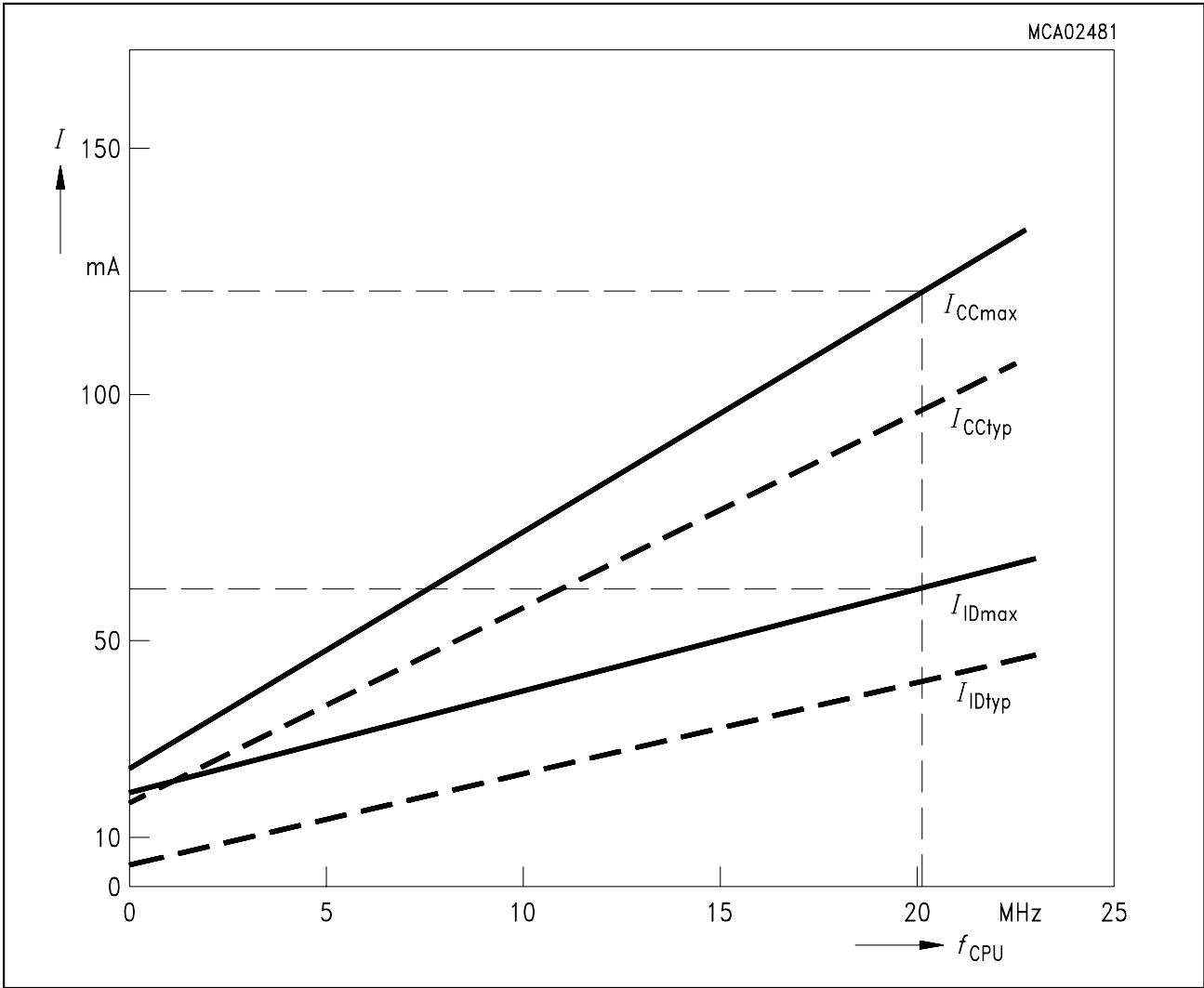


Figure 8
Supply/Idle Current as a Function of Operating Frequency

A/D Converter Characteristics

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$ for SAB-C167CR-LM

$T_A = -40\text{ to }+85\text{ }^{\circ}\text{C}$ for SAF-C167CR-LM

$T_A = -40\text{ to }+125\text{ }^{\circ}\text{C}$ for SAK-C167CR-LM

$4.0\text{ V} \leq V_{AREF} \leq V_{CC} + 0.1\text{ V}$; $V_{SS} - 0.1\text{ V} \leq V_{AGND} \leq V_{SS} + 0.2\text{ V}$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage range	V_{AIN} SR	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S CC	–	$2\ t_{SC}$		2) 4)
Conversion time	t_C CC	–	$14\ t_{CC} + t_S + 4TCL$		3) 4)
Total unadjusted error	TUE CC	–	± 2	LSB	5)
Internal resistance of reference voltage source	R_{AREF} SR	–	$t_{CC} / 165 - 0.25$	k Ω	t_{CC} in [ns] ^{6) 7)}
Internal resistance of analog source	R_{ASRC} SR	–	$t_S / 330 - 0.25$	k Ω	t_S in [ns] ^{2) 7)}
ADC input capacitance	C_{AIN} CC	–	33	pF	7)

Sample time and conversion time of the C167CR's ADC are programmable. The table below should be used to calculate the above timings.

ADCON.15 14 (ADCTC)	Conversion Clock t_{CC}	ADCON.13 12 (ADSTC)	Sample Clock t_{SC}
00	$TCL \times 24$	00	t_{CC}
01	Reserved, do not use	01	$t_{CC} \times 2$
10	$TCL \times 96$	10	$t_{CC} \times 4$
11	$TCL \times 48$	11	$t_{CC} \times 8$

Notes

- 1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.
- 2) During the sample time the input capacitance C_I can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S . After the end of the sample time t_S , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{SC} depend on programming and can be taken from the table above.
- 3) This parameter includes the sample time t_S , the time for determining the digital result and the time to load the result register with the conversion result. Values for the conversion clock t_{CC} depend on programming and can be taken from the table above.
- 4) This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.
- 5) TUE is tested at $V_{AREF} = 5.0\text{ V}$, $V_{AGND} = 0\text{ V}$, $V_{CC} = 4.9\text{ V}$. It is guaranteed by design characterization for all other voltages within the defined voltage range.
The specified TUE is guaranteed only if an overload condition (see I_{OV} specification) occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be $\pm 4\text{ LSB}$.
- 6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within t_{CC} . The maximum internal resistance results from the programmed conversion timing.
- 7) Not 100 % tested, guaranteed by design characterization.

Testing Waveforms

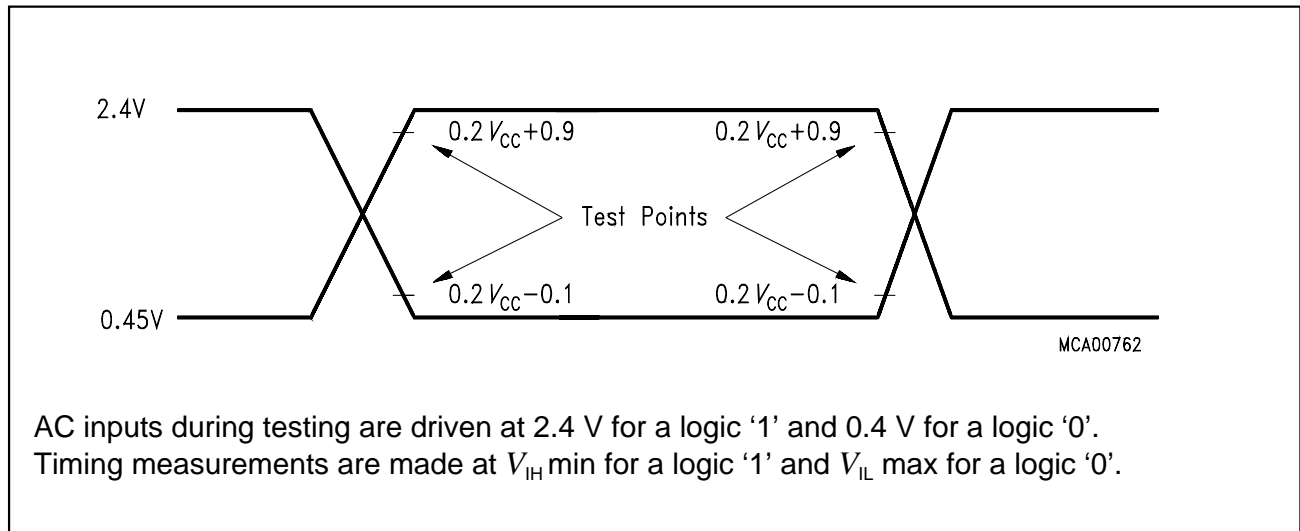


Figure 9
Input Output Waveforms

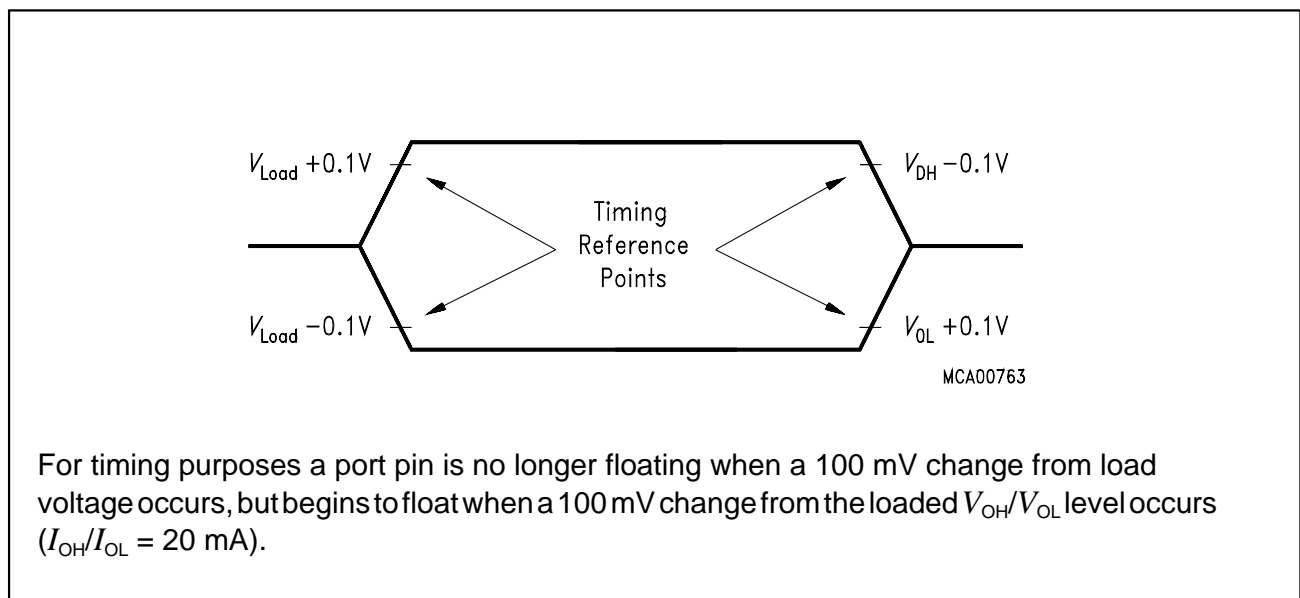


Figure 10
Float Waveforms

AC Characteristics

Definition of Internal Timing

The internal operation of the C167CR is controlled by the internal CPU clock f_{CPU} . Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called "TCL" (see figure below).

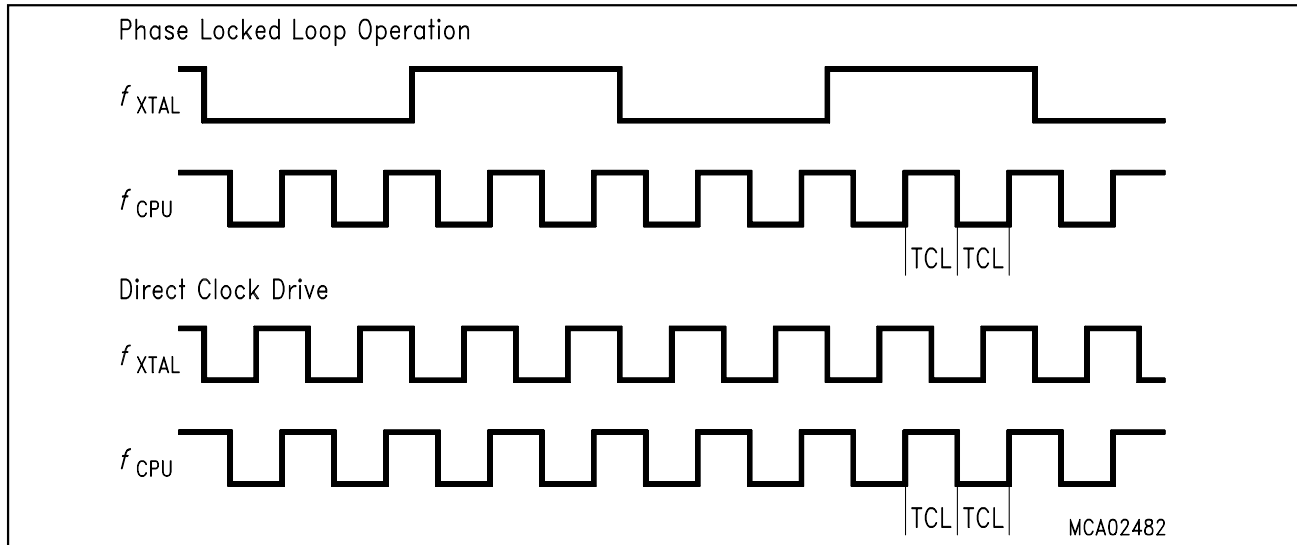


Figure 11
Generation Mechanisms for the CPU Clock

The CPU clock signal can be generated via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU} . This influence must be regarded when calculating the timings for the C167CR.

Direct Drive

When pin P0.15 (P0H.7) is low ('0') during reset the on-chip phase locked loop is disabled and the CPU clock is directly driven from the oscillator with the input clock signal.

The frequency of f_{CPU} directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL} .

The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$\text{TCL}_{\min} = 1/f_{\text{XTAL}} \times \text{DC}_{\min} \quad (\text{DC} = \text{duty cycle})$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{XTAL} is compensated so the duration of 2TCL is always $1/f_{\text{XTAL}}$. The minimum value TCL_{\min} therefore has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula $2\text{TCL} = 1/f_{\text{XTAL}}$.

Note: The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($\text{TCL}_{\max} = 1/f_{\text{XTAL}} \times \text{DC}_{\max}$) instead of TCL_{\min} .

Phase Locked Loop

When pin P0.15 (P0H.7) is high ('1') during reset the on-chip phase locked loop is enabled and provides the CPU clock. The PLL multiplies the input frequency by 4 (i.e. $f_{\text{CPU}} = f_{\text{XTAL}} \times 4$). With every fourth transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{XTAL} . The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and figure below).

For a period of $N \times \text{TCL}$ the minimum value is computed using the corresponding deviation D_N :

$$\text{TCL}_{\min} = \text{TCL}_{\text{NOM}} \times (1 - D_N / 100) \quad D_N = \pm (4 - N/15) \text{ [\%]},$$

where N = number of consecutive TCLs
and $1 \leq N \leq 40$.

So for a period of 3 TCLs (i.e. $N = 3$): $D_3 = 4 - 3/15 = 3.8 \text{ \%,}$

and $\text{TCL}_{\min} = \text{TCL}_{\text{NOM}} \times (1 - 3.8 / 100) = \text{TCL}_{\text{NOM}} \times 0.962$ (24.1 nsec @ $f_{\text{CPU}} = 20 \text{ MHz}$).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

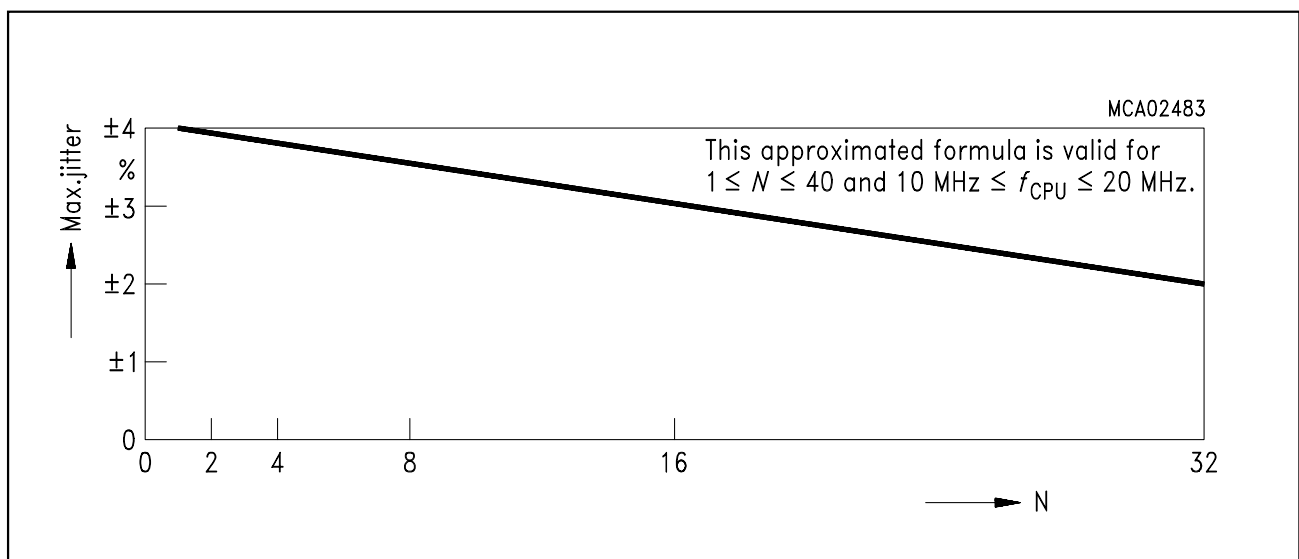


Figure 12
Approximated Maximum PLL Jitter

AC Characteristics

External Clock Drive XTAL1

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$
 $T_A = 0\text{ to } +70\text{ }^{\circ}\text{C}$ for SAB-C167CR-LM
 $T_A = -40\text{ to } +85\text{ }^{\circ}\text{C}$ for SAF-C167CR-LM
 $T_A = -40\text{ to } +125\text{ }^{\circ}\text{C}$ for SAK-C167CR-LM

Parameter	Symbol		Direct Drive 1:1		PLL 1:4		Unit
			min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	50	1000	200	333	ns
High time	t_1	SR	23 ^{1) 2)}	—	10	—	ns
Low time	t_2	SR	23 ^{1) 2)}	—	10	—	ns
Rise time	t_3	SR	—	10 ²⁾	—	10 ²⁾	ns
Fall time	t_4	SR	—	10 ²⁾	—	10 ²⁾	ns

1) For temperatures above $T_A = +85\text{ }^{\circ}\text{C}$ the minimum value for t_1 and t_2 is 25 ns.

2) The clock input signal must reach the defined levels V_{IL} and V_{IH2} .

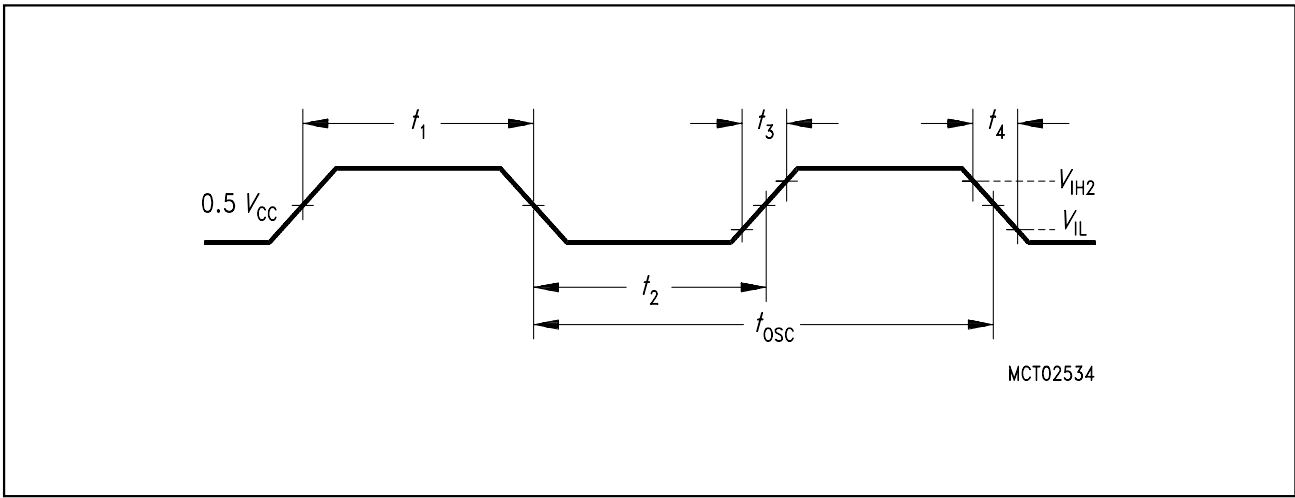


Figure 13
External Clock Drive XTAL1

Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Description	Symbol	Values
ALE Extension	t_A	$TCL \times \langle ALECTL \rangle$
Memory Cycle Time Waitstates	t_C	$2TCL \times (15 - \langle MCTC \rangle)$
Memory Tristate Time	t_F	$2TCL \times (1 - \langle MTTC \rangle)$

AC Characteristics Multiplexed Bus

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }+70\text{ }^\circ\text{C}$ for SAB-C167CR-LM

$T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ for SAF-C167CR-LM

$T_A = -40\text{ to }+125\text{ }^\circ\text{C}$ for SAK-C167CR-LM

C_L (for PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT) = 100 pF

C_L (for Port 6, \overline{CS}) = 100 pF

ALE cycle time = $6\text{ TCL} + 2t_A + t_C + t_F$ (150 ns at 20-MHz CPU clock without waitstates)

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
ALE high time	t_5 CC	$15 + t_A$	—	$TCL - 10 + t_A$	—	ns
Address setup to ALE	t_6 CC	$10 + t_A$	—	$TCL - 15 + t_A$	—	ns
Address hold after ALE	t_7 CC	$15 + t_A$	—	$TCL - 10 + t_A$	—	ns
ALE falling edge to \overline{RD} , \overline{WR} (with RW-delay)	t_8 CC	$15 + t_A$	—	$TCL - 10 + t_A$	—	ns
ALE falling edge to \overline{RD} , \overline{WR} (no RW-delay)	t_9 CC	$-10 + t_A$	—	$-10 + t_A$	—	ns
Address float after \overline{RD} , \overline{WR} (with RW-delay)	t_{10} CC	—	5	—	5	ns
Address float after \overline{RD} , \overline{WR} (no RW-delay)	t_{11} CC	—	30	—	$TCL + 5$	ns
\overline{RD} , \overline{WR} low time (with RW-delay)	t_{12} CC	$40 + t_C$	—	$2TCL - 10 + t_C$	—	ns
\overline{RD} , \overline{WR} low time (no RW-delay)	t_{13} CC	$65 + t_C$	—	$3TCL - 10 + t_C$	—	ns

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
$\overline{\text{RD}}$ to valid data in (with RW-delay)	t_{14} SR	–	$30 + t_C$	–	$2\text{TCL} - 20 + t_C$	ns
$\overline{\text{RD}}$ to valid data in (no RW-delay)	t_{15} SR	–	$55 + t_C$	–	$3\text{TCL} - 20 + t_C$	ns
ALE low to valid data in	t_{16} SR	–	$55 + t_A + t_C$	–	$3\text{TCL} - 20 + t_A + t_C$	ns
Address to valid data in	t_{17} SR	–	$70 + 2t_A + t_C$	–	$4\text{TCL} - 30 + 2t_A + t_C$	ns
Data hold after $\overline{\text{RD}}$ rising edge	t_{18} SR	0	–	0	–	ns
Data float after $\overline{\text{RD}}$	t_{19} SR	–	$35 + t_F$	–	$2\text{TCL} - 15 + t_F$	ns
Data valid to $\overline{\text{WR}}$	t_{22} SR	$25 + t_C$	–	$2\text{TCL} - 25 + t_C$	–	ns
Data hold after $\overline{\text{WR}}$	t_{23} CC	$35 + t_F$	–	$2\text{TCL} - 15 + t_F$	–	ns
ALE rising edge after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{25} CC	$35 + t_F$	–	$2\text{TCL} - 15 + t_F$	–	ns
Address hold after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{27} CC	$35 + t_F$	–	$2\text{TCL} - 15 + t_F$	–	ns
ALE falling edge to $\overline{\text{CS}}$	t_{38} CC	$-5 - t_A$	$10 - t_A$	$-5 - t_A$	$10 - t_A$	ns
$\overline{\text{CS}}$ low to Valid Data In	t_{39} SR	–	$55 + t_C + 2t_A$	–	$3\text{TCL} - 20 + t_C + 2t_A$	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{40} CC	$60 + t_F$	–	$3\text{TCL} - 15 + t_F$	–	ns
ALE fall. edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (with RW delay)	t_{42} CC	$20 + t_A$	–	$\text{TCL} - 5 + t_A$	–	ns
ALE fall. edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW delay)	t_{43} CC	$-5 + t_A$	–	$-5 + t_A$	–	ns
Address float after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (with RW delay)	t_{44} CC	–	0	–	0	ns
Address float after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW delay)	t_{45} CC	–	25	–	TCL	ns
$\overline{\text{RdCS}}$ to Valid Data In (with RW delay)	t_{46} SR	–	$25 + t_C$	–	$2\text{TCL} - 25 + t_C$	ns

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
RdCS to Valid Data In (no RW delay)	t_{47} SR	–	$50 + t_C$	–	$3TCL - 25 + t_C$	ns
RdCS, WrCS Low Time (with RW delay)	t_{48} CC	$40 + t_C$	–	$2TCL - 10 + t_C$	–	ns
RdCS, WrCS Low Time (no RW delay)	t_{49} CC	$65 + t_C$	–	$3TCL - 10 + t_C$	–	ns
Data valid to $\overline{\text{WrCS}}$	t_{50} CC	$35 + t_C$	–	$2TCL - 15 + t_C$	–	ns
Data hold after $\overline{\text{RdCS}}$	t_{51} SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$	t_{52} SR	–	$30 + t_F$	–	$2TCL - 20 + t_F$	ns
Address hold after RdCS, WrCS	t_{54} CC	$30 + t_F$	–	$2TCL - 20 + t_F$	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{56} CC	$30 + t_F$	–	$2TCL - 20 + t_F$	–	ns

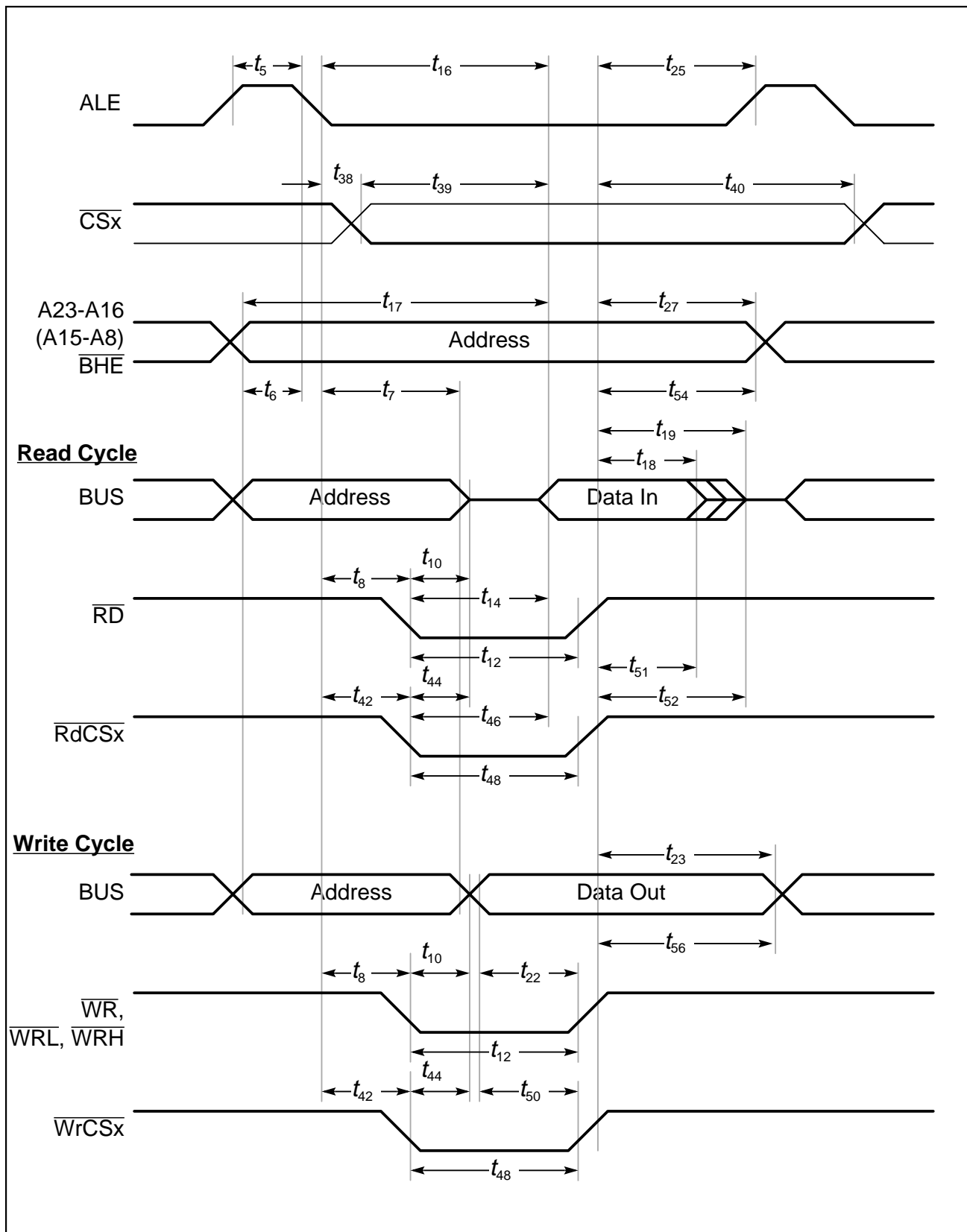


Figure 14-1
External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE

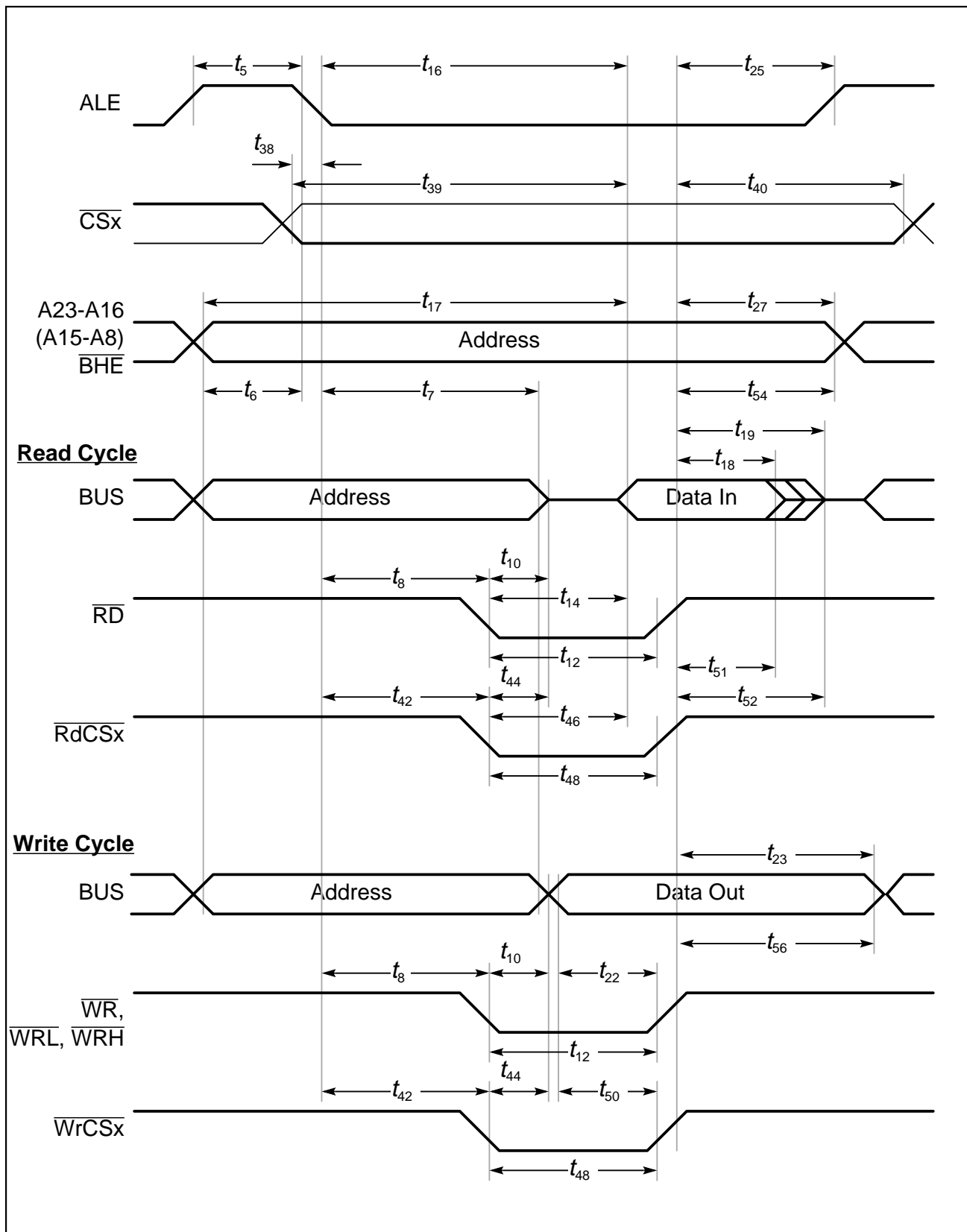


Figure 14-2
External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Extended ALE

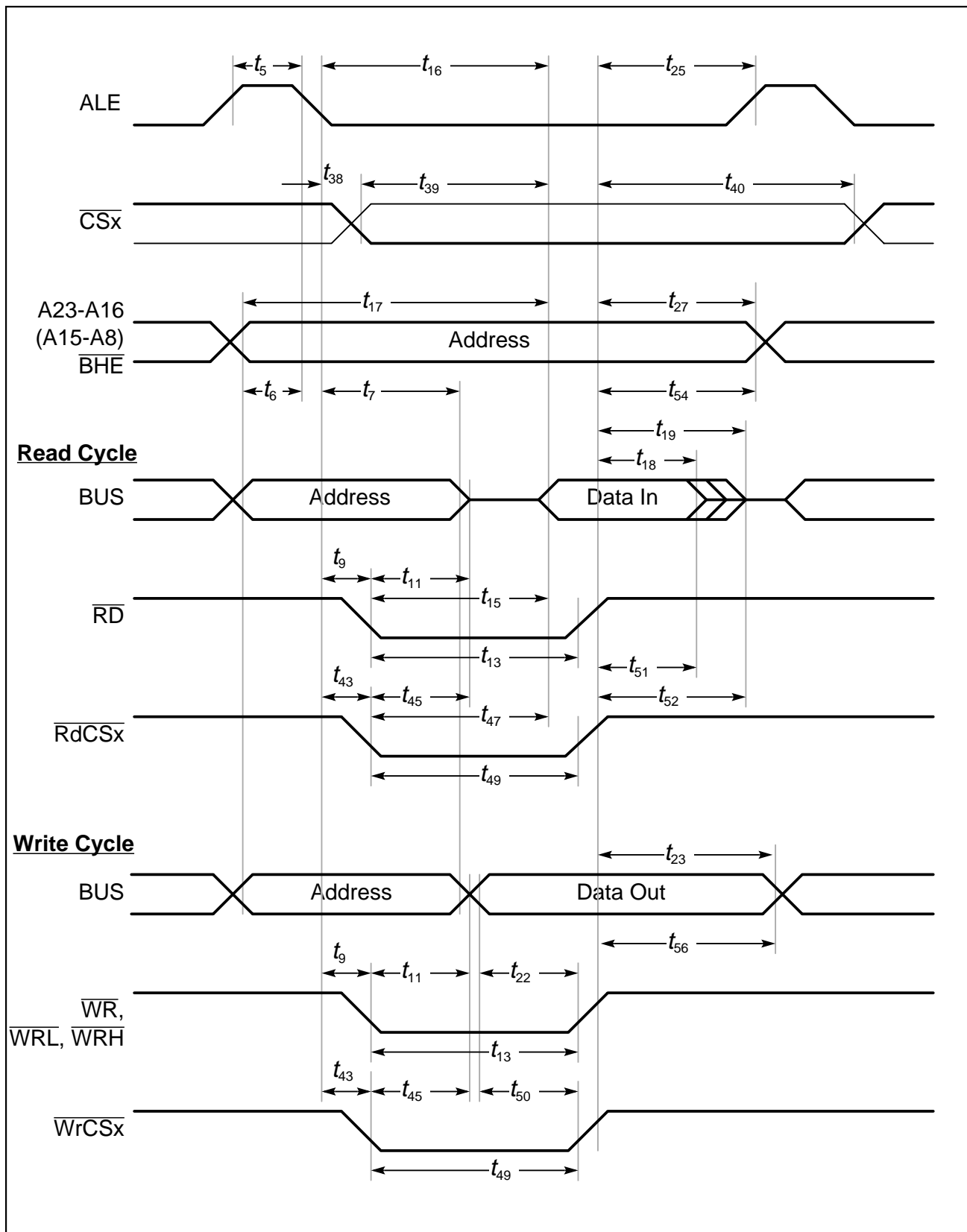


Figure 14-3
External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Normal ALE

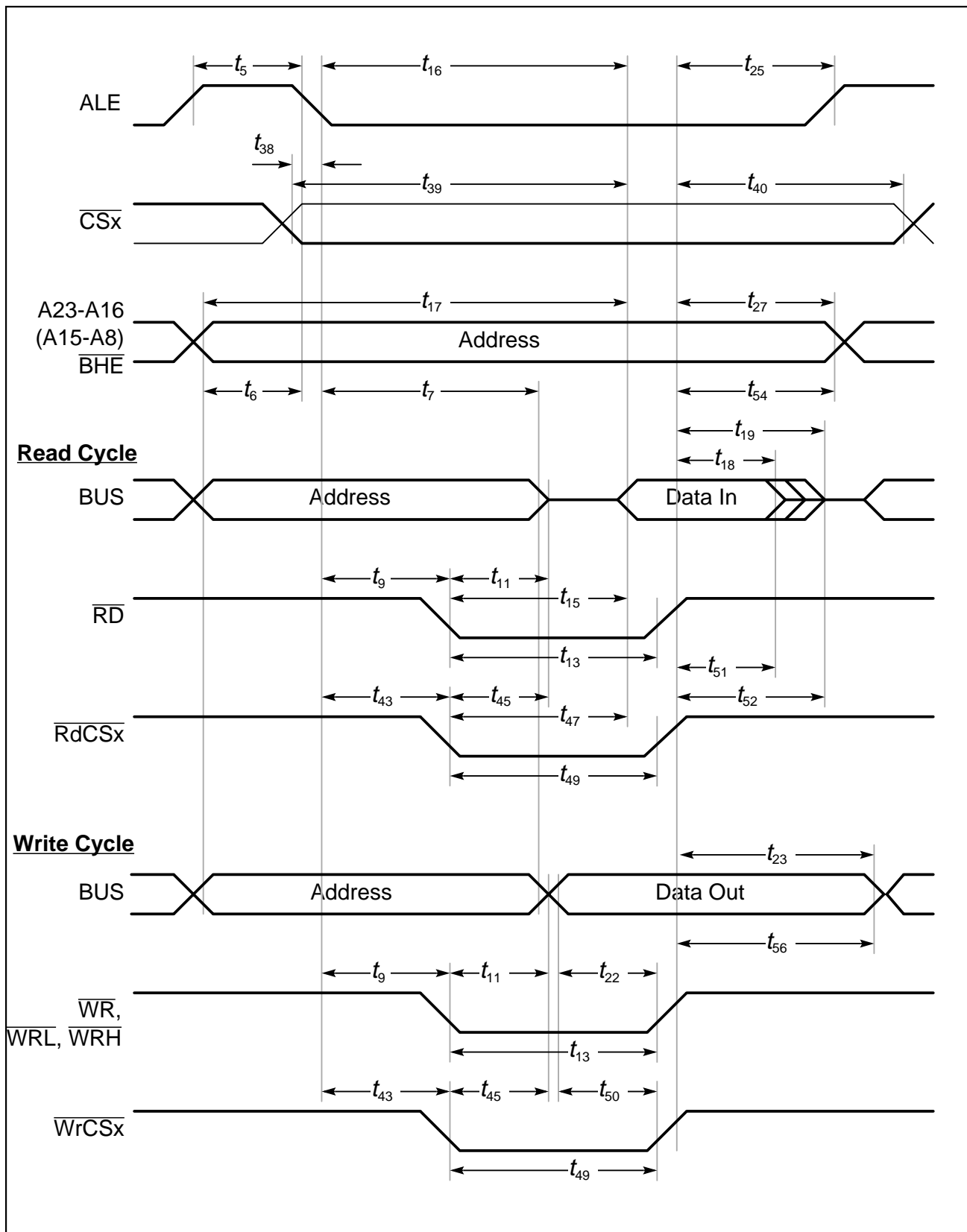


Figure 14-4
External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics

Demultiplexed Bus

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$ for SAB-C167CR-LM

$T_A = -40\text{ to }+85\text{ }^{\circ}\text{C}$ for SAF-C167CR-LM

$T_A = -40\text{ to }+125\text{ }^{\circ}\text{C}$ for SAK-C167CR-LM

C_L (for PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT) = 100 pF

C_L (for Port 6, \overline{CS}) = 100 pF

ALE cycle time = $4\text{ TCL} + 2t_A + t_C + t_F$ (100 ns at 20-MHz CPU clock without waitstates)

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
		min.	max.	min.	max.	
ALE high time	t_5 CC	$15 + t_A$	—	$\text{TCL} - 10 + t_A$	—	ns
Address setup to ALE	t_6 CC	$10 + t_A$	—	$\text{TCL} - 15 + t_A$	—	ns
ALE falling edge to \overline{RD} , \overline{WR} (with RW-delay)	t_8 CC	$15 + t_A$	—	$\text{TCL} - 10 + t_A$	—	ns
ALE falling edge to \overline{RD} , \overline{WR} (no RW-delay)	t_9 CC	$-10 + t_A$	—	$-10 + t_A$	—	ns
\overline{RD} , \overline{WR} low time (with RW-delay)	t_{12} CC	$40 + t_C$	—	$2\text{TCL} - 10 + t_C$	—	ns
\overline{RD} , \overline{WR} low time (no RW-delay)	t_{13} CC	$65 + t_C$	—	$3\text{TCL} - 10 + t_C$	—	ns
\overline{RD} to valid data in (with RW-delay)	t_{14} SR	—	$30 + t_C$	—	$2\text{TCL} - 20 + t_C$	ns
\overline{RD} to valid data in (no RW-delay)	t_{15} SR	—	$55 + t_C$	—	$3\text{TCL} - 20 + t_C$	ns
ALE low to valid data in	t_{16} SR	—	$55 + t_A + t_C$	—	$3\text{TCL} - 20 + t_A + t_C$	ns
Address to valid data in	t_{17} SR	—	$70 + 2t_A + t_C$	—	$4\text{TCL} - 30 + 2t_A + t_C$	ns
Data hold after \overline{RD} rising edge	t_{18} SR	0	—	0	—	ns
Data float after \overline{RD} rising edge (with RW-delay ¹⁾)	t_{20} SR	—	$35 + t_F$	—	$2\text{TCL} - 15 + 2t_A + t_F$ ¹⁾	ns
Data float after \overline{RD} rising edge (no RW-delay ¹⁾)	t_{21} SR	—	$15 + t_F$	—	$\text{TCL} - 10 + 2t_A + t_F$ ¹⁾	ns
Data valid to \overline{WR}	t_{22} CC	$25 + t_C$	—	$2\text{TCL} - 25 + t_C$	—	ns
Data hold after \overline{WR}	t_{24} CC	$15 + t_F$	—	$\text{TCL} - 10 + t_F$	—	ns

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
ALE rising edge after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{26}	CC	$-10 + t_F$	—	$-10 + t_F$	—	ns
Address hold after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{28}	CC	$0 + t_F$	—	$0 + t_F$	—	ns
ALE falling edge to $\overline{\text{CS}}$	t_{38}	CC	$-5 - t_A$	$10 - t_A$	$-5 - t_A$	$10 - t_A$	ns
$\overline{\text{CS}}$ low to Valid Data In	t_{39}	SR	—	$55 + t_C + 2t_A$	—	$3\text{TCL} - 20 + t_C + 2t_A$	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{41}	CC	$10 + t_F$	—	$\text{TCL} - 15 + t_F$	—	ns
ALE falling edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (with RW-delay)	t_{42}	CC	$20 + t_A$	—	$\text{TCL} - 5 + t_A$	—	ns
ALE falling edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW-delay)	t_{43}	CC	$-5 + t_A$	—	$-5 + t_A$	—	ns
$\overline{\text{RdCS}}$ to Valid Data In (with RW-delay)	t_{46}	SR	—	$25 + t_C$	—	$2\text{TCL} - 25 + t_C$	ns
$\overline{\text{RdCS}}$ to Valid Data In (no RW-delay)	t_{47}	SR	—	$50 + t_C$	—	$3\text{TCL} - 25 + t_C$	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (with RW-delay)	t_{48}	CC	$40 + t_C$	—	$2\text{TCL} - 10 + t_C$	—	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (no RW-delay)	t_{49}	CC	$65 + t_C$	—	$3\text{TCL} - 10 + t_C$	—	ns
Data valid to $\overline{\text{WrCS}}$	t_{50}	CC	$35 + t_C$	—	$2\text{TCL} - 15 + t_C$	—	ns
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	—	0	—	ns
Data float after $\overline{\text{RdCS}}$ (with RW-delay)	t_{53}	SR	—	$30 + t_F$	—	$2\text{TCL} - 20 + t_F$	ns
Data float after $\overline{\text{RdCS}}$ (no RW-delay)	t_{68}	SR	—	$5 + t_F$	—	$\text{TCL} - 20 + t_F$	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55}	CC	$-10 + t_F$	—	$-10 + t_F$	—	ns
Data hold after $\overline{\text{WrCS}}$	t_{57}	CC	$10 + t_F$	—	$\text{TCL} - 15 + t_F$	—	ns

1) RW-delay and t_A refer to the next following bus cycle.

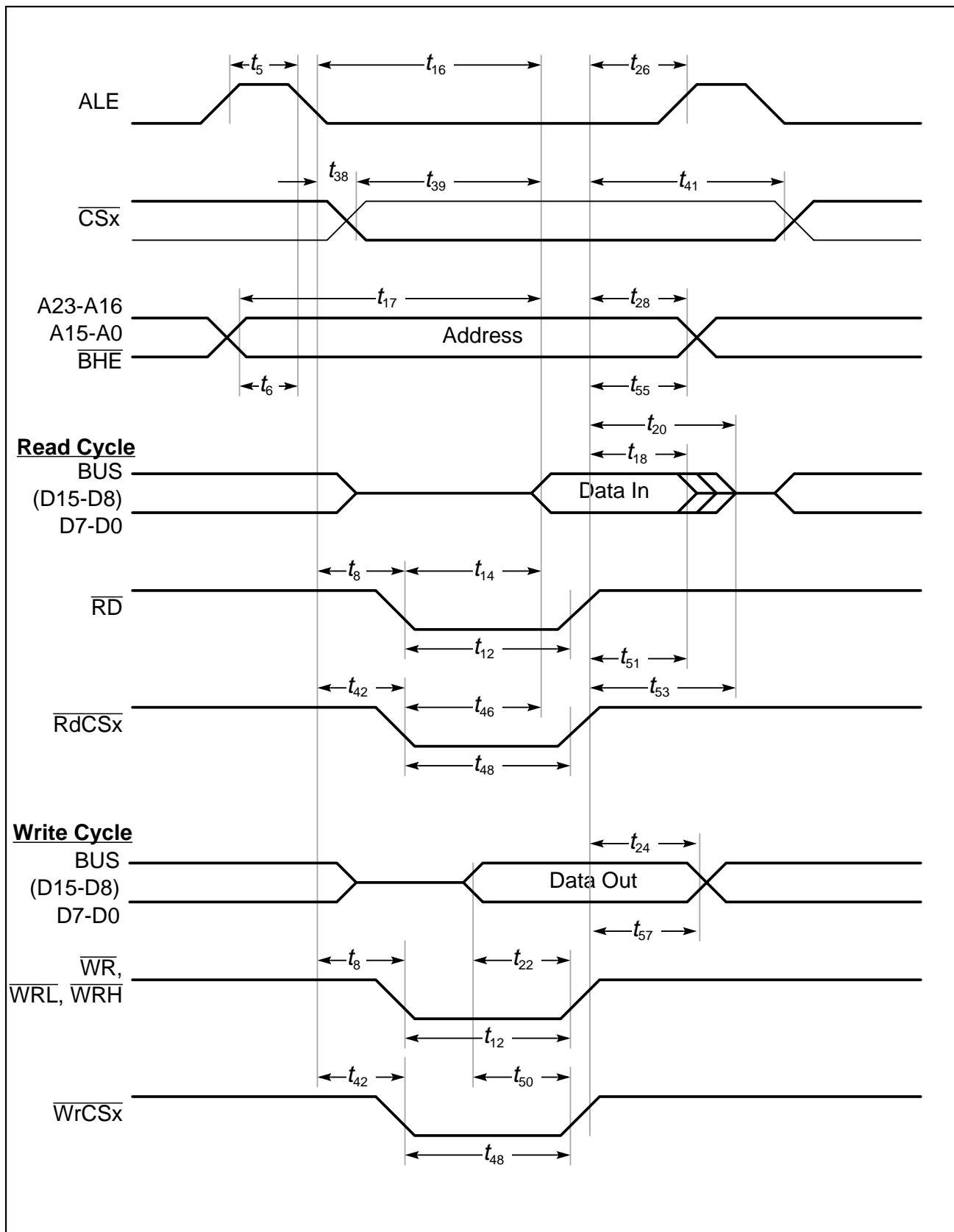


Figure 15-1
External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Normal ALE

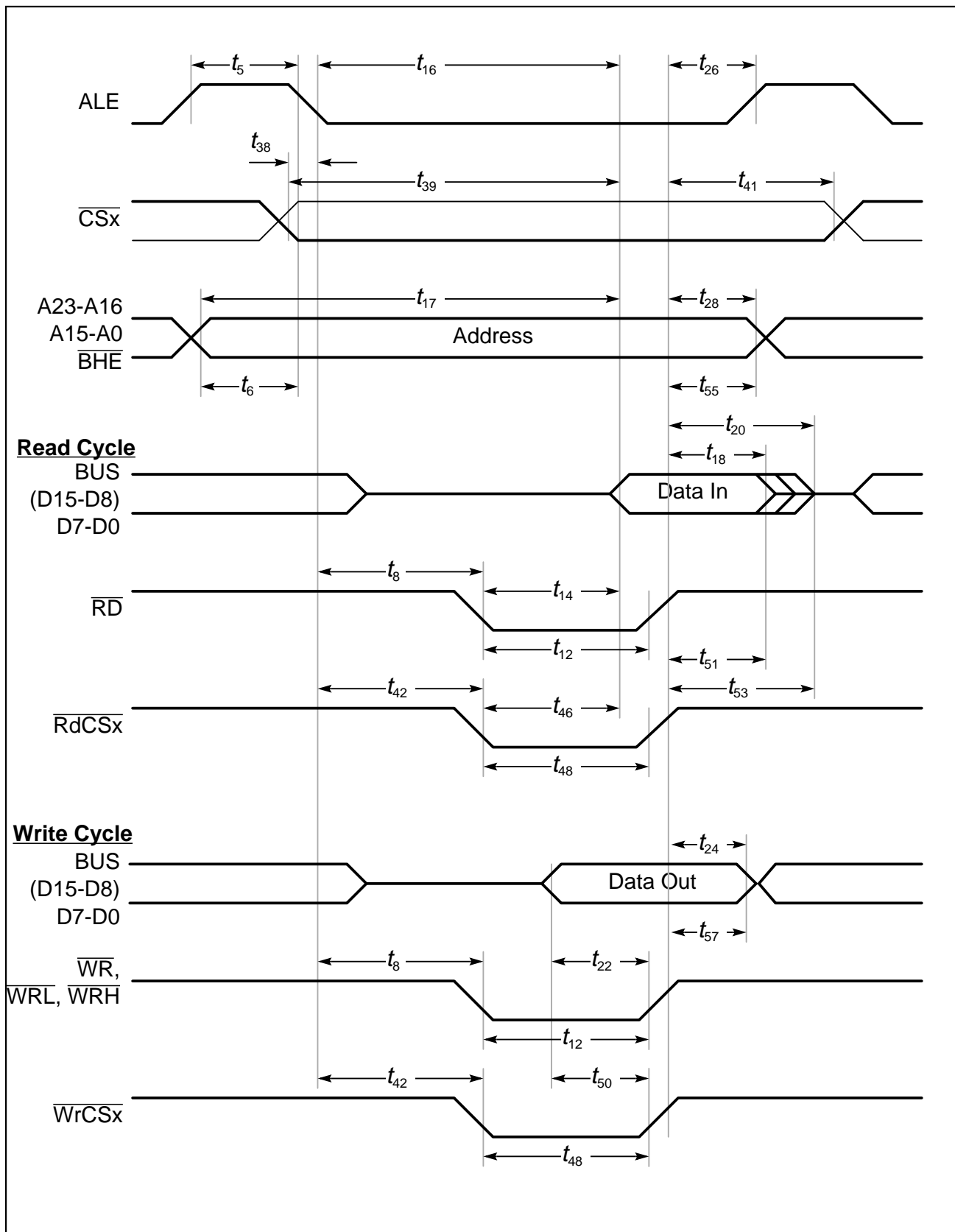


Figure 15-2
External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE

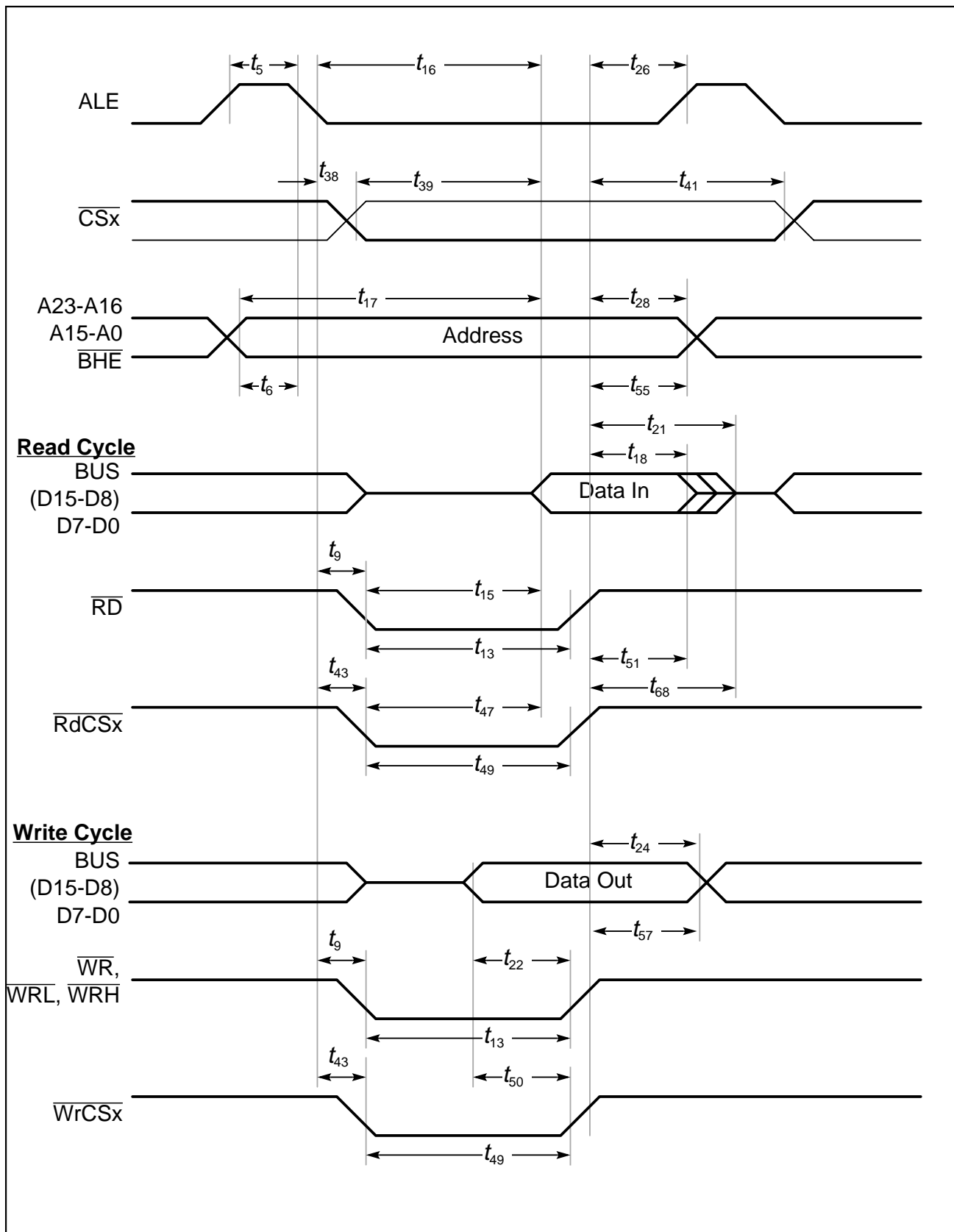


Figure 15-3
External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE

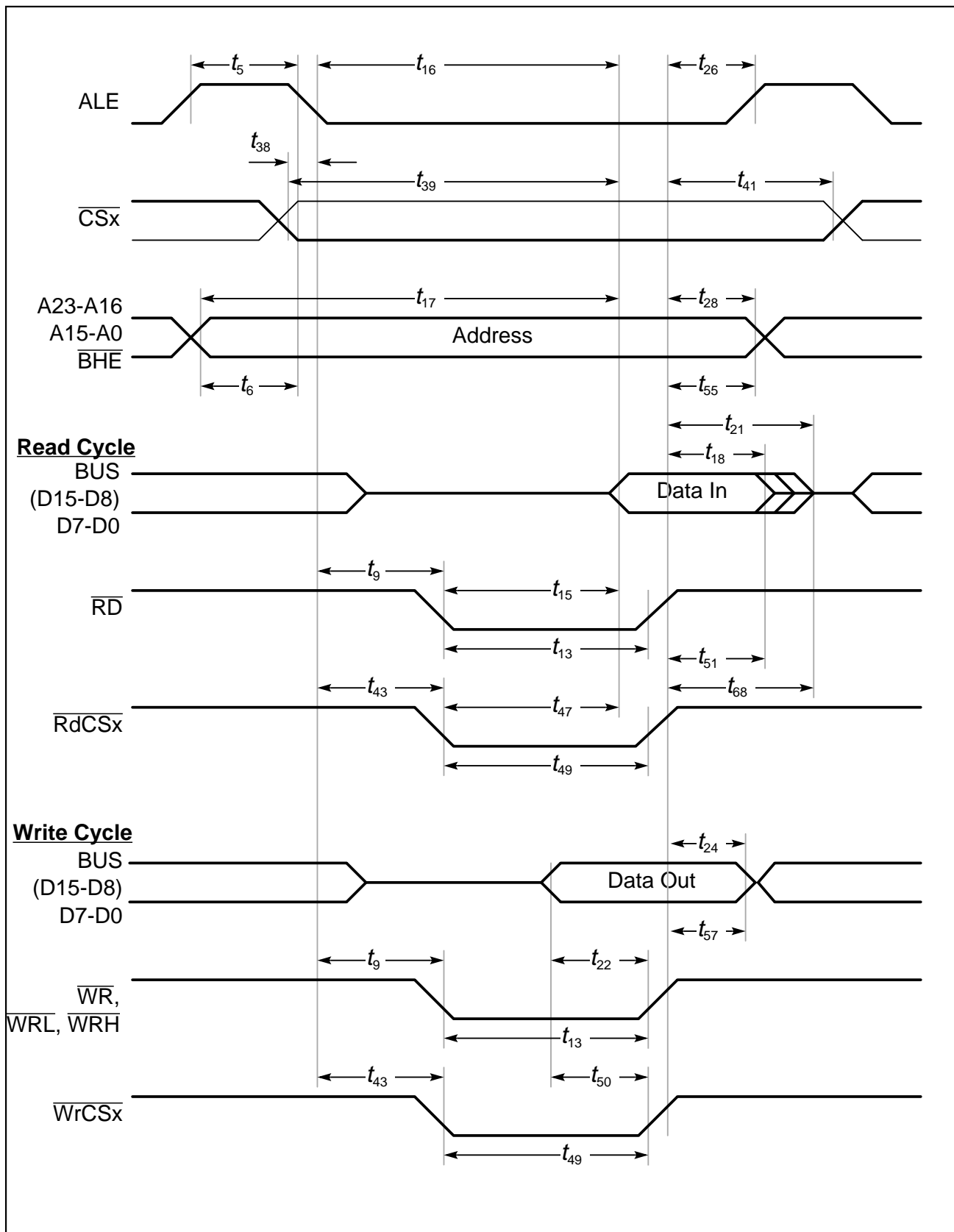


Figure 15-4
External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics CLKOUT and READY

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$ for SAB-C167CR-LM

$T_A = -40\text{ to }+85\text{ }^{\circ}\text{C}$ for SAF-C167CR-LM

$T_A = -40\text{ to }+125\text{ }^{\circ}\text{C}$ for SAK-C167CR-LM

C_L (for PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT) = 100 pF

C_L (for Port 6, $\overline{\text{CS}}$) = 100 pF

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	50	50	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	20	–	TCL – 5	–	ns
CLKOUT low time	t_{31}	CC	15	–	TCL – 10	–	ns
CLKOUT rise time	t_{32}	CC	–	5	–	5	ns
CLKOUT fall time	t_{33}	CC	–	5	–	5	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	$0 + t_A$	$10 + t_A$	$0 + t_A$	$10 + t_A$	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35}	SR	15	–	15	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36}	SR	0	–	0	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37}	SR	65	–	2TCL + 15	–	ns
Asynchronous $\overline{\text{READY}}$ setup time ¹⁾	t_{58}	SR	15	–	15	–	ns
Asynchronous $\overline{\text{READY}}$ hold time ¹⁾	t_{59}	SR	0	–	0	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) ²⁾	t_{60}	SR	0	$0 + 2t_A + t_F$ ²⁾	0	TCL - 25 + $2t_A + t_F$ ²⁾	ns

Notes

- ¹⁾ These timings are given for test purposes only, in order to assure recognition at a specific clock edge.
- ²⁾ Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.
The $2t_A$ refer to the next following bus cycle.

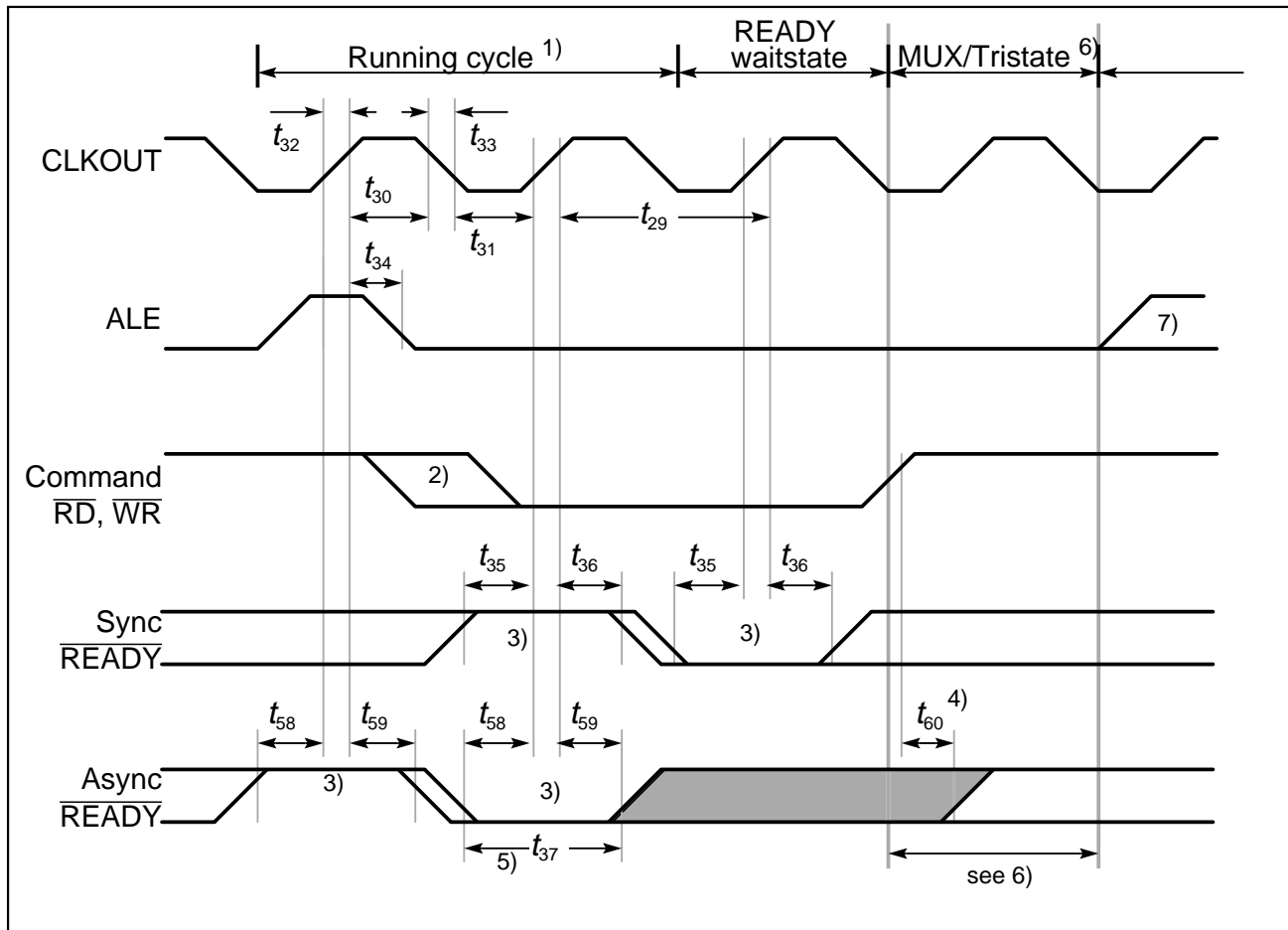


Figure 16
CLKOUT and $\overline{\text{READY}}$

Notes

- 1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
- 2) The leading edge of the respective command depends on RW-delay.
- 3) $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled waitstate, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.
- 4) $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).
- 5) If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if $\overline{\text{READY}}$ is removed in response to the command (see Note 4)).
- 6) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.
- 7) The next external bus cycle may start here.

AC Characteristics

External Bus Arbitration

$V_{CC} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$ for SAB-C167CR-LM

$T_A = -40\text{ to }+85\text{ }^{\circ}\text{C}$ for SAF-C167CR-LM

$T_A = -40\text{ to }+125\text{ }^{\circ}\text{C}$ for SAK-C167CR-LM

C_L (for PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT) = 100 pF

C_L (for Port 6, \overline{CS}) = 100 pF

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1/2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
HOLD input setup time to CLKOUT	t_{61}	SR	20	–	20	–	ns
CLKOUT to \overline{HLDA} high or \overline{BREQ} low delay	t_{62}	CC	–	20	–	20	ns
CLKOUT to \overline{HLDA} low or \overline{BREQ} high delay	t_{63}	CC	–	20	–	20	ns
\overline{CSx} release	t_{64}	CC	–	20	–	20	ns
\overline{CSx} drive	t_{65}	CC	– 5	25	– 5	25	ns
Other signals release	t_{66}	CC	–	20	–	20	ns
Other signals drive	t_{67}	CC	– 5	25	– 5	25	ns

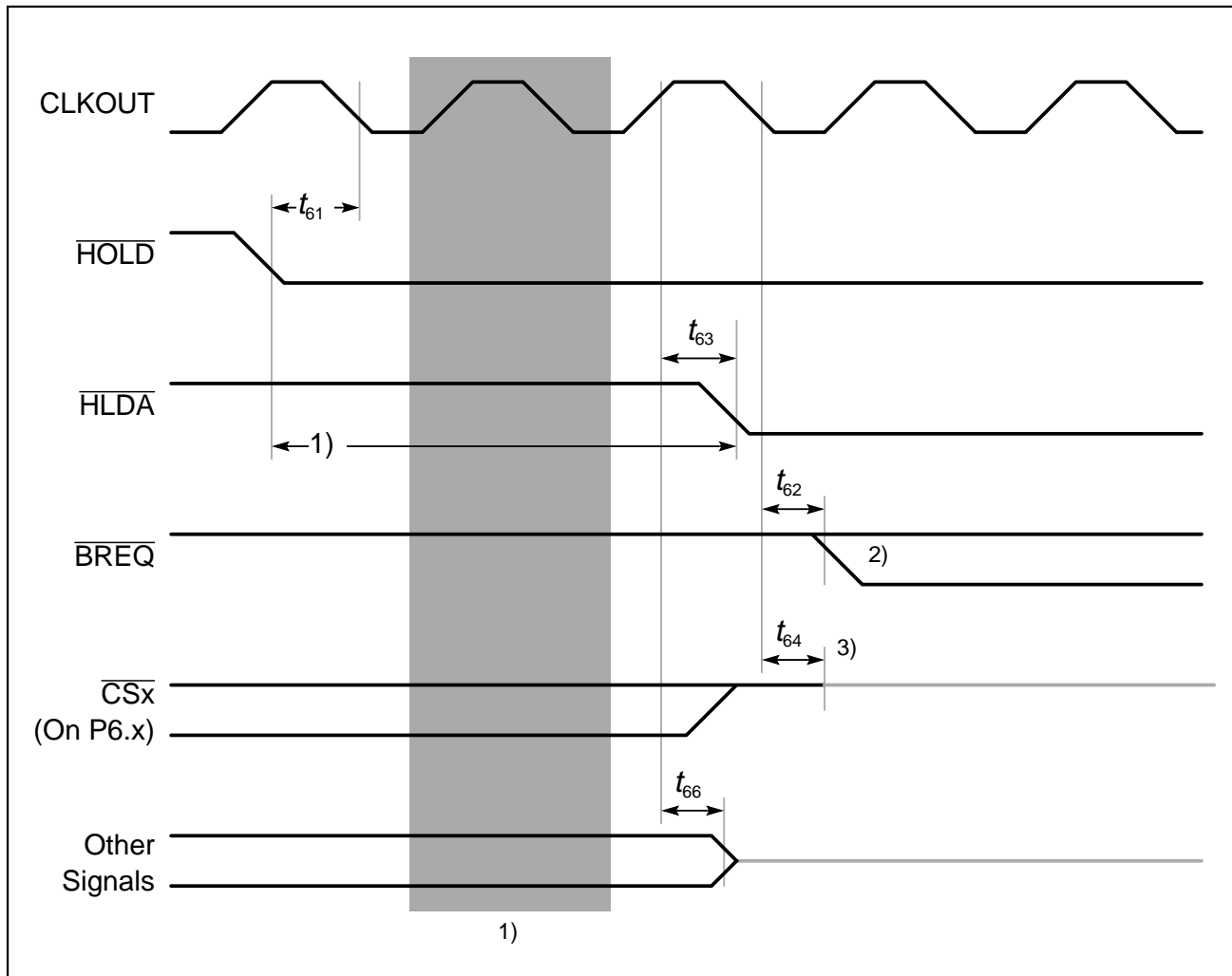


Figure 17
External Bus Arbitration, Releasing the Bus

Notes

- 1) The C167CR will complete the currently running bus cycle before granting bus access.
- 2) This is the first possibility for $\overline{\text{BREQ}}$ to get active.
- 3) The $\overline{\text{CS}}$ outputs will be resistive high (pullup) after t_{64} .

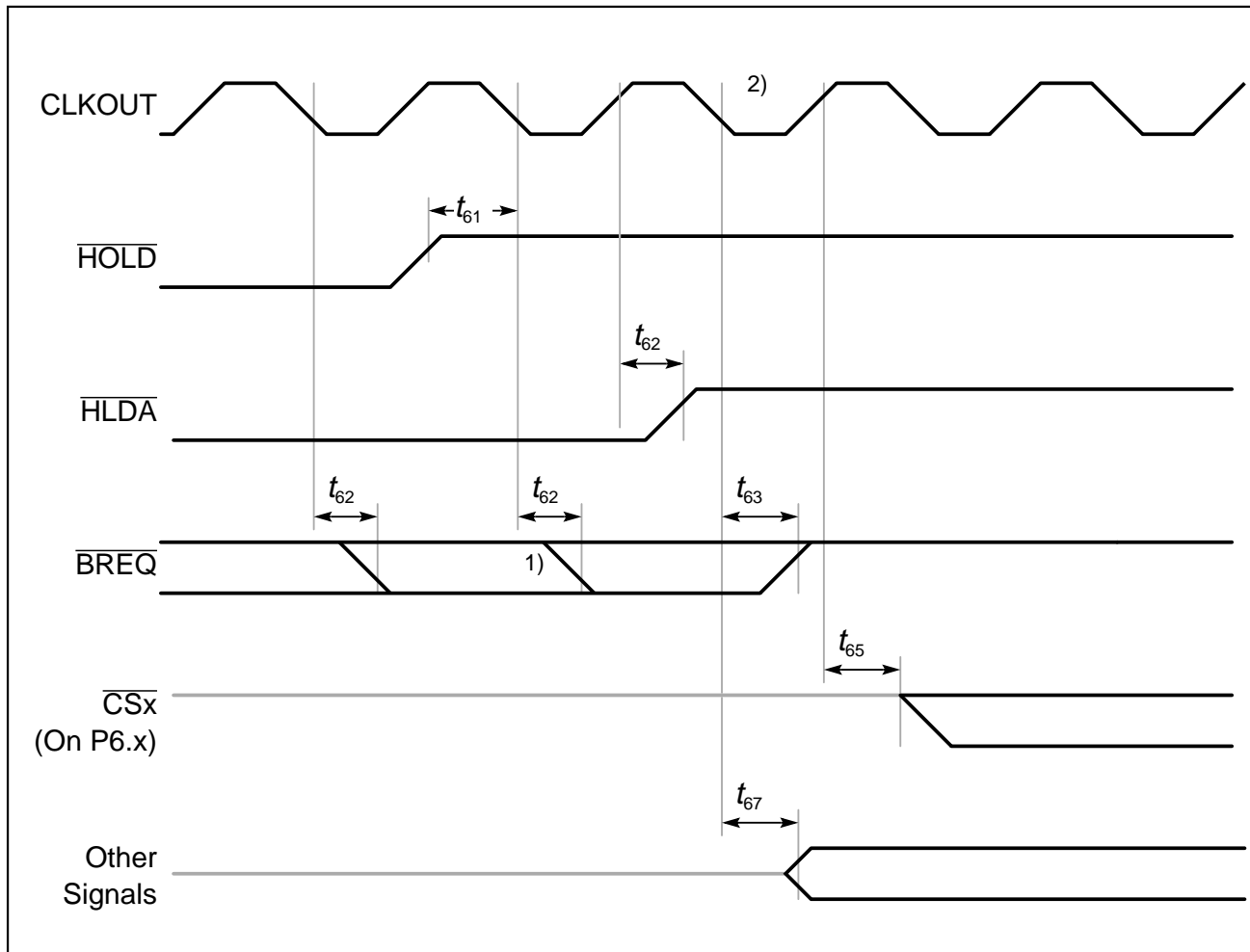


Figure 18
External Bus Arbitration, (Regaining the Bus)

Notes

- 1) This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence. Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high. Please note that $\overline{\text{HOLD}}$ may also be deactivated without the C167CR requesting the bus.
- 2) The next C167CR driven bus cycle may start here.