

2SK3000

Silicon N Channel MOS FET
Low Frequency Power Switching

HITACHI

ADE-208-585 (Z)

1st. Edition

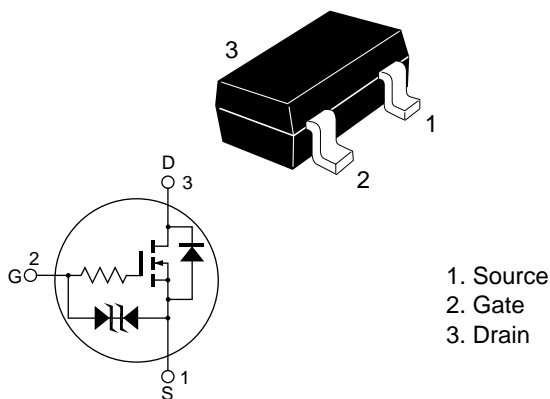
December 1997

Features

- Low on-resistance
 $R_{DS(on)} = 0.25\Omega$ typ. ($V_{GS} = 10\text{ V}$, $I_D = 450\text{ mA}$)
- 4V gate drive devices.
- Small package (MPAK)
- Expansive drain to source surge power capability

Outline

MPAK



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	± 10	V
Drain current	I_D	1.0	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	4.0	A
Reverse drain current	I_{DR}	1.0	A
Channel dissipation	P_{ch} ^{Note2}	400	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

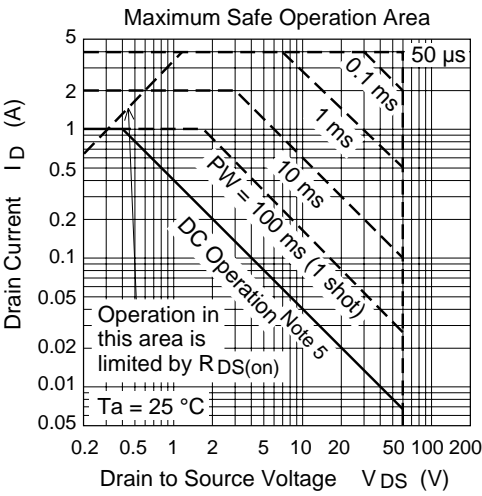
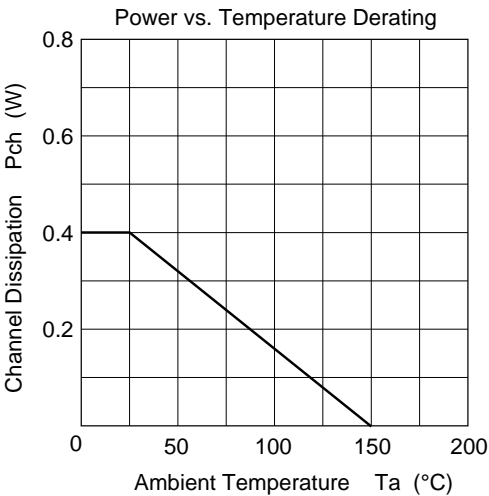
Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
2. When using the glass epoxy board (10 mm x 10 mm x 1 mm¹)

Electrical Characteristics (Ta = 25°C)

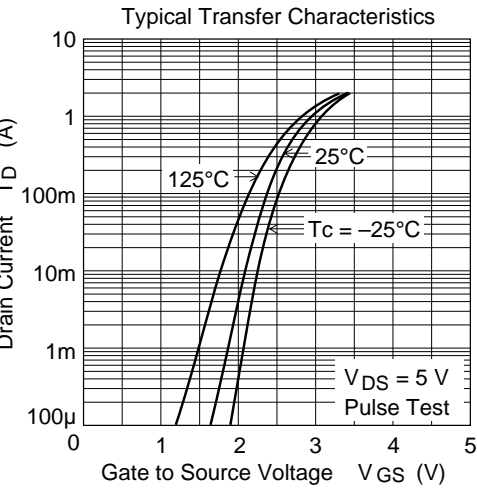
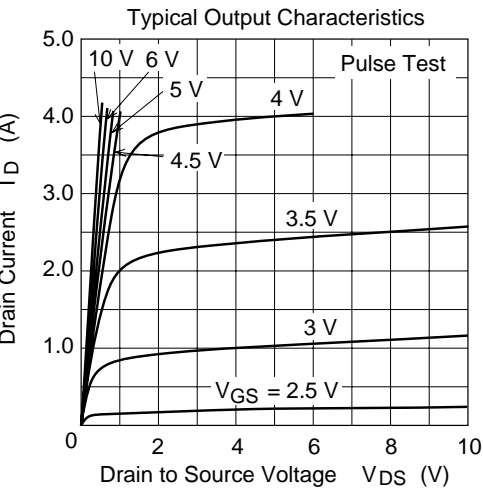
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	60	V	$I_D = 100\mu A$, $V_{GS} = 0$
Drain to source voltage	$V_{DS(SUS)}$	40	—	—	V	$L = 100\mu H$, $I_D = 3 A$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 10	—	—	V	$I_G = \pm 100\mu A$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1.0	μA	$V_{DS} = 40 V$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 6.5 V$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.1	—	2.1	V	$I_D = 10\mu A$, $V_{DS} = 5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.5	Ω	$I_D = 450 mA$ $V_{GS} = 4 V$ ^{Note3}
Static drain to source on state resistance	$R_{DS(on)}$	—	0.25	0.3	Ω	$I_D = 450 mA$ $V_{GS} = 10 V$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	0.5	1.2	—	S	$I_D = 450 mA$ $V_{DS} = 10 V$ ^{Note3}
Input capacitance	C_{iss}	—	14.0	—	pF	$V_{DS} = 10 V$
Output capacitance	C_{oss}	—	68	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	3.0	—	pF	$f = 1 MHz$
Turn-on delay time	$t_{d(on)}$	—	0.12	—	μs	$V_{GS} = 4 V$, $I_D = 450 mA$
Rise time	t_r	—	0.6	—	μs	$R_L = 22 \Omega$
Turn-off delay time	$t_{d(off)}$	—	1.7	—	μs	
Fall time	t_f	—	1.4	—	μs	

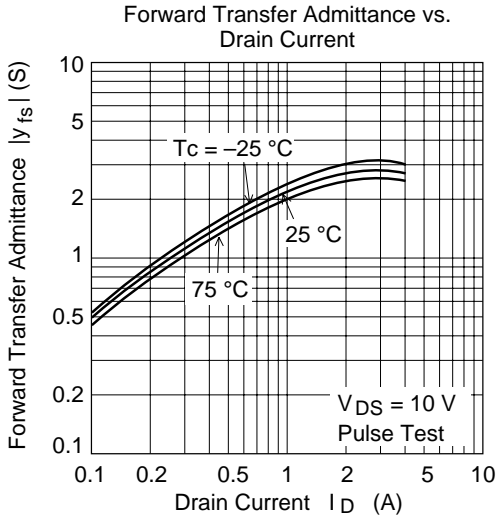
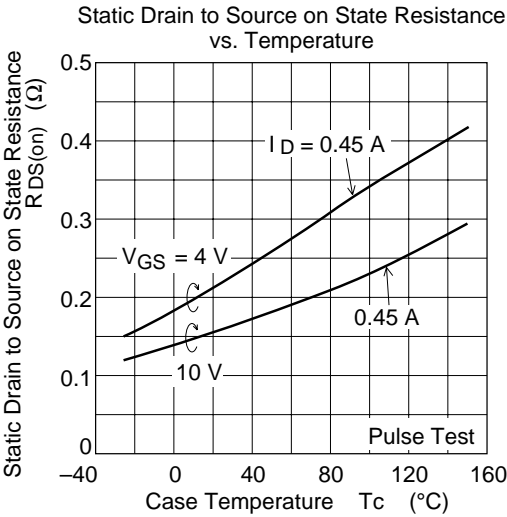
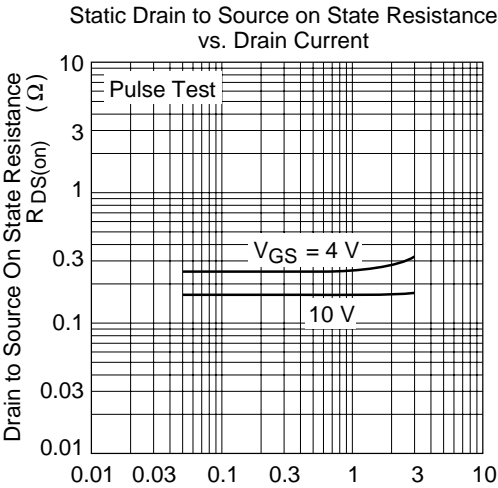
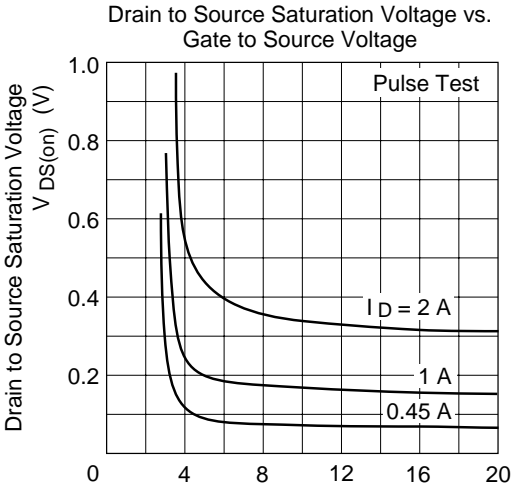
Note: 3. Pulse test
4. Marking is “ZY”.

Main Characteristics

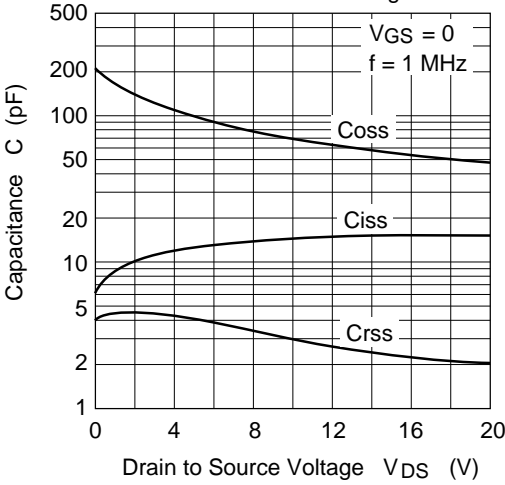


Note5 : When using the glass epoxy board (10mm x 10mm x 1mm^t)

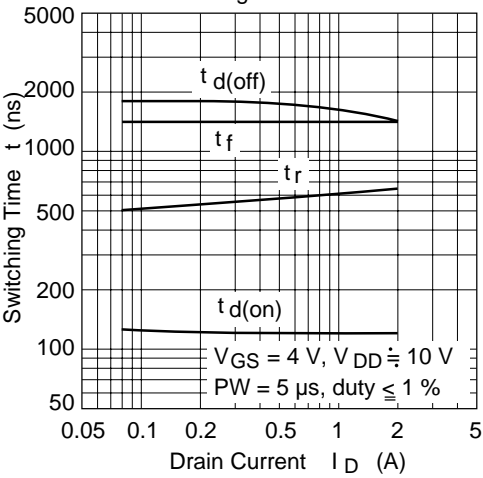




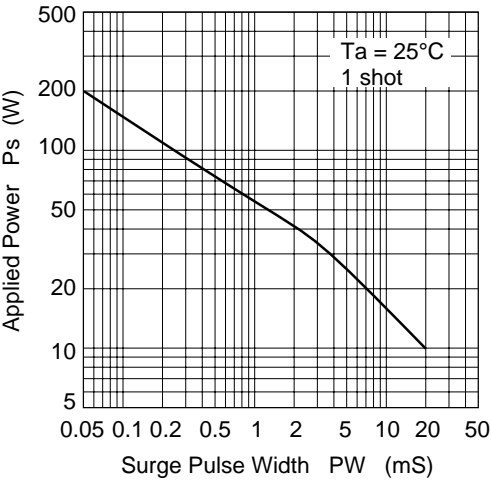
Typical Capacitance vs.
Drain to Source Voltage



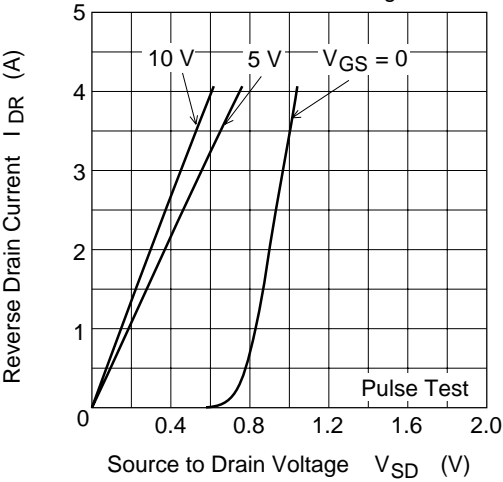
Switching Characteristics



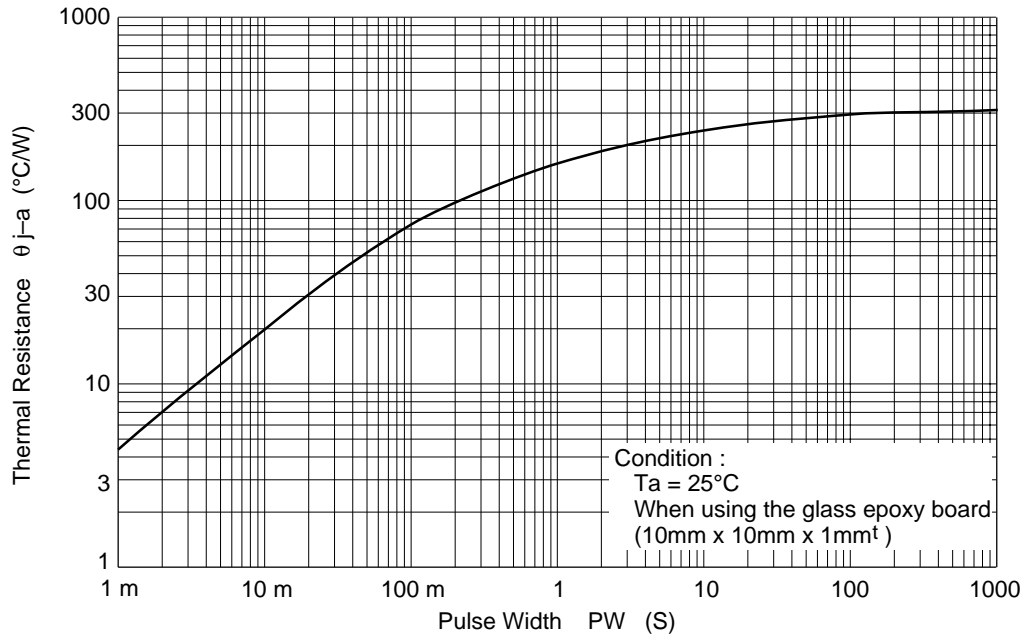
Drain to Source Diode Reverse Surge
Destruction Characteristics



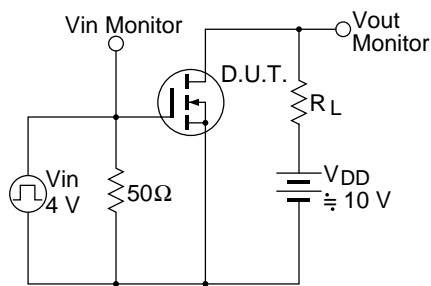
Reverse Drain Current vs.
Source to Drain Voltage



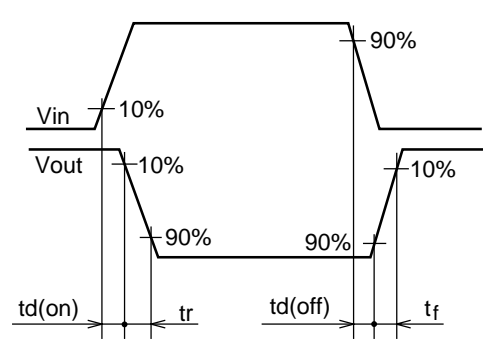
Transient Thermal Resistance



Switching Time Test Circuit

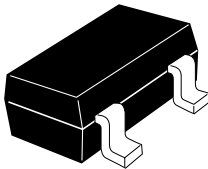
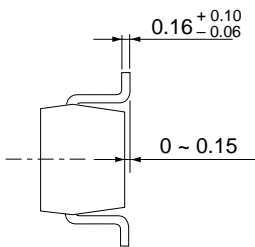
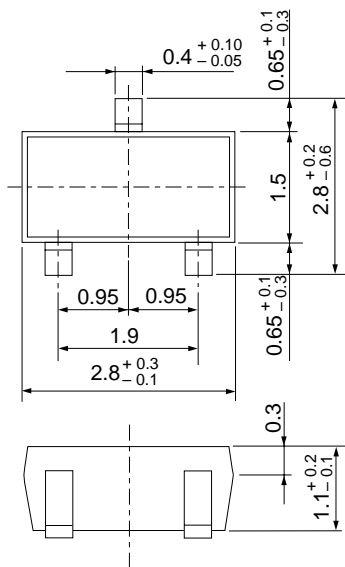


Switching Time Waveforms



Package Dimensions

Unit: mm



Hitachi Code	MPAK
EIAJ	SC-59A
JEDEC	TO-236Mod.

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