

SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

- Meet or Exceed the Requirements of ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.10 and V.11
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noise Environments
- Driver Positive- and Negative-Current Limiting
- Thermal Shutdown Protection
- Driver 3-State Outputs
- Receiver Common-Mode Input Voltage Range of -12 V to 12 V
- Receiver Input Sensitivity . . . $\pm 200\text{ mV}$
- Receiver Hysteresis . . . 50 mV Typ
- Receiver Input Impedance . . . $12\text{ k}\Omega\text{ Min}$
- Receiver 3-State Outputs (SN751177 Only)
- Operate From Single 5-V Supply

description

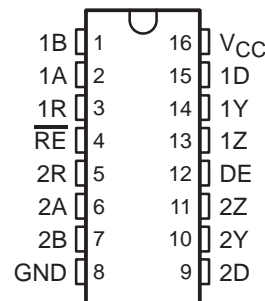
The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits that are designed for balanced multipoint bus transmission at rates up to 10 Mbit/s. They are designed to improve the performance of full-duplex data communications over long bus lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.10 and V.11.

The SN751177 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal-shutdown protection from line-fault conditions on the transmission bus line.

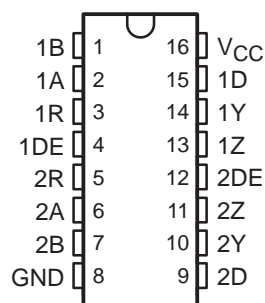
The receiver features high input impedance of at least $12\text{ k}\Omega$, an input sensitivity of $\pm 200\text{ mV}$ over a common-mode input voltage range of -12 V to 12 V , and typical input hysteresis of 50 mV . Fail-safe design ensures that if the receiver inputs are open, the receiver outputs always will be high.

The SN751177 and SN751178 are characterized for operation from -20°C to 85°C .

SN751177 . . . N OR NS[†] PACKAGE
(TOP VIEW)



SN751178 . . . N OR NS[†] PACKAGE
(TOP VIEW)



[†] The NS package is only available taped and reeled.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

Function Tables

SN751177, SN751178
(each driver)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

SN751177
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

SN751178
(each receiver)

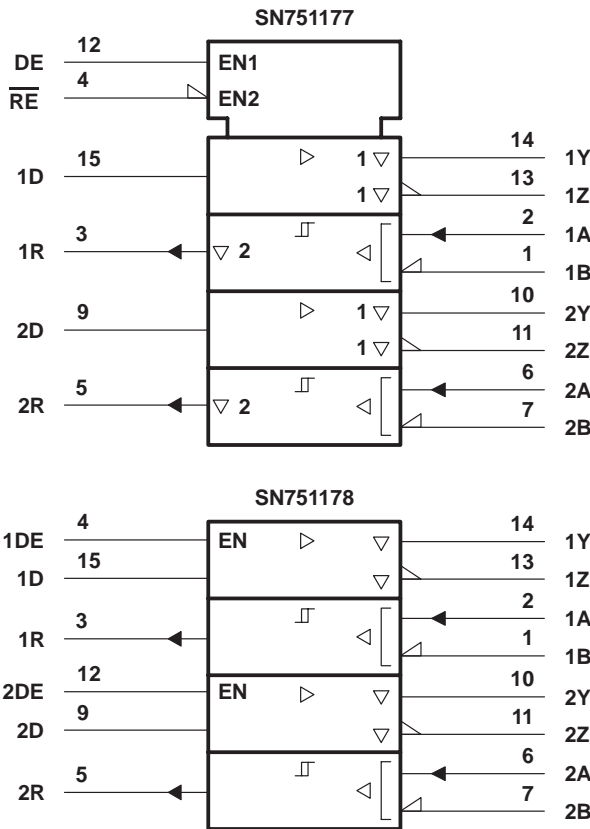
DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$?
$V_{ID} \leq -0.2 \text{ V}$	L

H = high level, L = low level,
? = indeterminate

SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

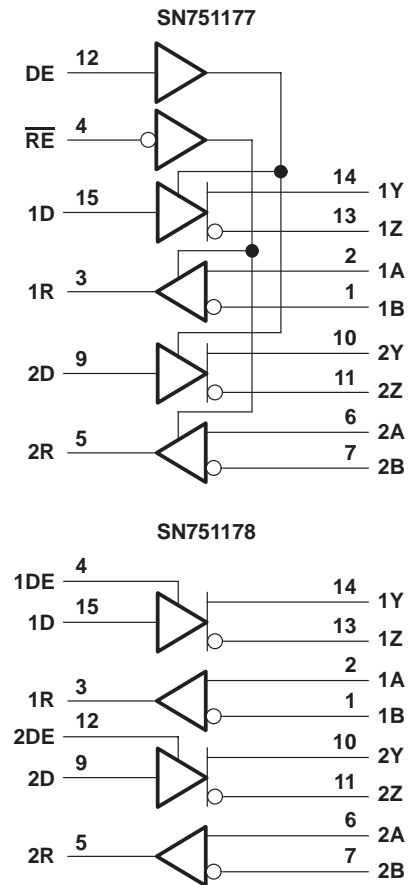
SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

logic symbols†

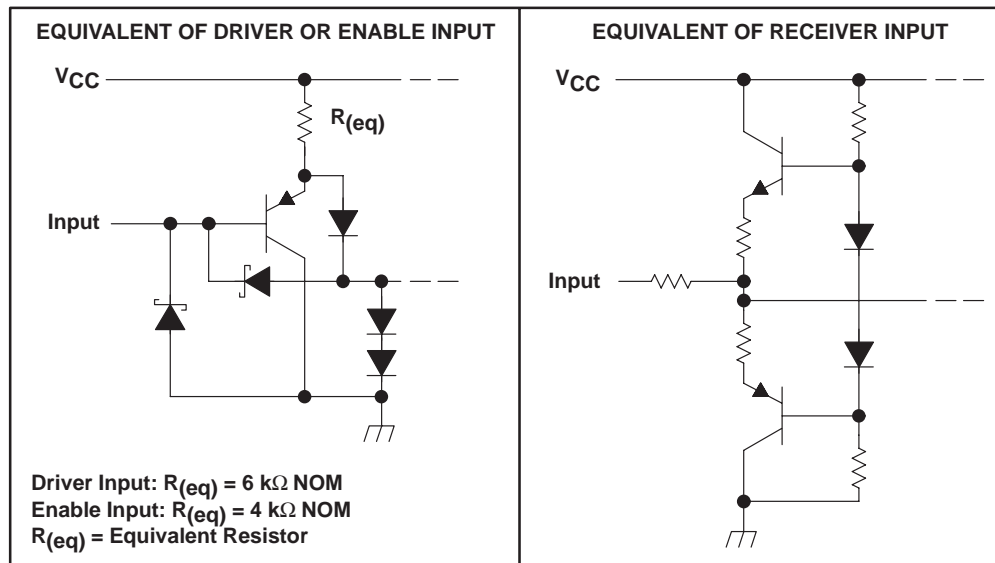


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



schematics of inputs

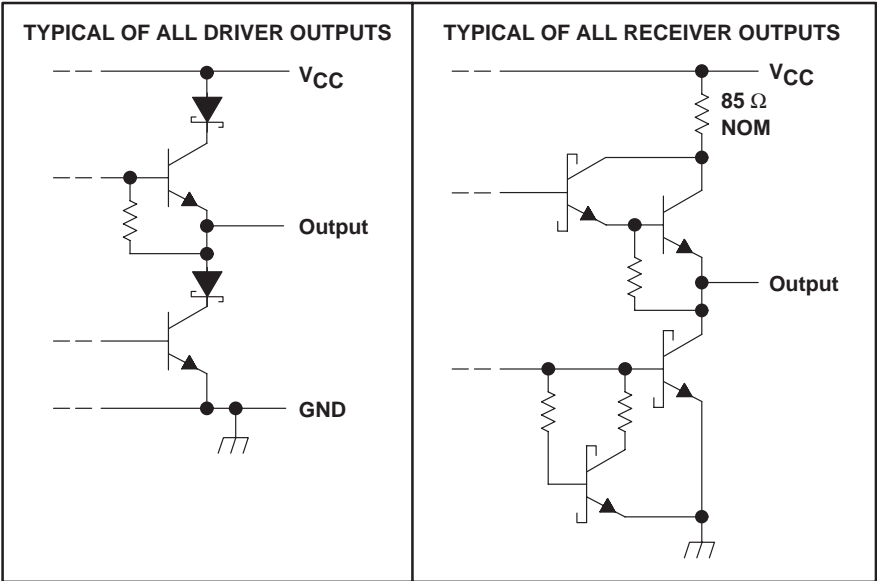


All resistor values are nominal.

SN751177, SN751178
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

schematics of outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I (DE, \overline{RE} , and D inputs)	7 V
Receiver input voltage range, V_I (A or B inputs)	–25 V to 25 V
Receiver differential input voltage range, V_{ID} (see Note 2)	–25 V to 25 V
Driver output voltage range, V_O	–10 V to 15 V
Receiver low-level output current, I_{OL}	50 mA
Package thermal impedance, θ_{JA} (see Note 3): N package	78°C/W
NS package	111°C/W
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
High-level input voltage, V _{IH}	DE, \overline{RE} , and D inputs	2			V
Low-level input voltage, V _{IL}		0.8			V
Common-mode output voltage, V _{OC}	Driver	−7†			V
High-level output current, I _{OH}		−60			mA
Low-level output current, I _{OL}		60			mA
Common-mode input voltage, V _{IC}	Receiver	±12			V
Differential input voltage, V _{ID}		±12			V
High-level output current, I _{OH}		−400			μA
Low-level output current, I _{OL}		16			mA
Operating free-air temperature, T _A		−20			85 °C

[†] The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

SN751177, SN751178

DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

DRIVER SECTIONS

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18\text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OH} = -33\text{ mA}$		3.7		V
V_{OL} Low-level output voltage	$V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OH} = 33\text{ mA}$		1.1		V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		6	V
$ V_{OD2} $ Differential output voltage	$R_L = 100\ \Omega$, See Figure 1	2 or $1/2 V_{OD1}^\ddagger$			V
	$R_L = 54\ \Omega$, See Figure 1	1.5		5	
V_{OD3} Differential output voltage	See Note 4	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of differential output voltage (see Note 5)	$R_L = 54\ \Omega$ or $100\ \Omega$, See Figure 1			± 0.2	V
V_{OC} Common-mode output voltage		-1 §		3	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage (see Note 5)				± 0.2	V
I_O Output current with power off	$V_{CC} = 0$, $V_O = -7\text{ V to }12\text{ V}$			± 100	μA
I_{OZ} High-impedance-state output current	$V_O = -7\text{ V to }12\text{ V}$			± 100	μA
I_{IH} High-level input current	$V_{IH} = 2.7\text{ V}$			20	μA
I_{IL} Low-level input current	$V_{IL} = 0.4\text{ V}$			-100	μA
I_{OS} Short-circuit output current (see Note 6)	$V_O = -7\text{ V}$			-250	mA
	$V_O = V_{CC}$			250	
	$V_O = 12\text{ V}$			250	
I_{CC} Supply current	No load	Outputs enabled		80	mA
		Outputs disabled		50	

† All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

‡ The minimum V_{OD2} with a $100\text{-}\Omega$ load is either $1/2 V_{OD1}$ or 2 V , whichever is greater.

§ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 4. See TIA/EIA-485-A Figure 3.5, Test Termination Measurement 2

5. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics at $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_d(\text{OD})$ Differential output delay time	$R_L = 54\ \Omega$, See Figure 3		20	25	ns
$t_t(\text{OD})$ Differential output transition time			27	35	ns
t_{PLH} Propagation delay time, low- to high-level output	$R_L = 27\ \Omega$, See Figure 4		20	25	ns
t_{PHL} Propagation delay time, high- to low-level output			20	25	ns
t_{PZH} Output enable time to high level	$R_L = 110\ \Omega$, See Figure 5		80	120	ns
t_{PZL} Output enable time to low level	$R_L = 110\ \Omega$, See Figure 6		40	60	ns
t_{PHZ} Output disable time from high level	$R_L = 110\ \Omega$, See Figure 5		90	120	ns
t_{PLZ} Output disable time from low level	$R_L = 110\ \Omega$, See Figure 6		30	45	ns



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
$ V_{OD1} $	V_O	V_O
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $		V_t (Test Termination Measurement 2)
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{OS} $	$ V_{OS} $
$\Delta V_{OC} $	$ V_{OS} - \bar{V}_{OS} $	$ V_{OS} - \bar{V}_{OS} $
I_{OS}	$ I_{sa} , I_{sb} $	
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

RECEIVER SECTIONS

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+} Positive-going input threshold voltage	$V_O = 2.7 \text{ V}$, $I_O = -0.4 \text{ mA}$			0.2	V
V_{IT-} Negative-going input threshold voltage	$V_O = 0.5 \text{ V}$, $I_O = 16 \text{ mA}$	-0.2‡			V
V_{hys} Input hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV
V_{IK} Enable clamp voltage	SN751177 $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{ID} = 200 \text{ mV}$, $I_{OH} = -400 \mu\text{A}$	2.7			V
V_{OL} Low-level output voltage	$V_{ID} = -200 \text{ mV}$			0.45	V
				0.5	
I_{OZ} High-impedance-state output current	SN751177 $V_O = 0.4 \text{ V to } 2.4 \text{ V}$			±20	μA
I_I Line input current (see Note 7)	Other input at 0 V			1	mA
				-0.8	
I_{IH} High-level enable input current	SN751177 $V_{IH} = 2.7 \text{ V}$			20	μA
I_{IL} Low-level enable input current	SN751177 $V_{IL} = 0.4 \text{ V}$			-100	μA
I_{OS} Short-circuit output current (see Note 6)		-15		-85	μA
I_{CC} Supply current	No load, Outputs enabled		80	110	mA
r_i Input resistance		12			kΩ

† All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

7. Refer to ANSI Standards TIA/EIA-422-B, TIA/EIA-423-A, and TIA/EIA-485-A for exact conditions.



SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

switching characteristics at $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$, See Figure 7		20	35	ns
t_{PHL} Propagation delay time, high- to low-level output			22	35	ns
t_{PZH} Output enable time to high level	SN751177 See Figure 8		17	25	ns
t_{PZL} Output enable time to low level			20	27	ns
t_{PHZ} Output disable time from high level			25	40	ns
t_{PLZ} Output disable time from low level			30	40	ns

PARAMETER MEASUREMENT INFORMATION

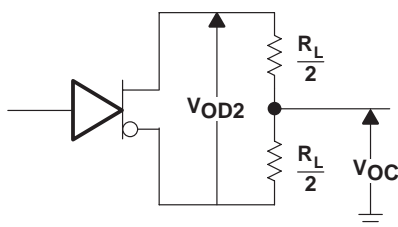


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

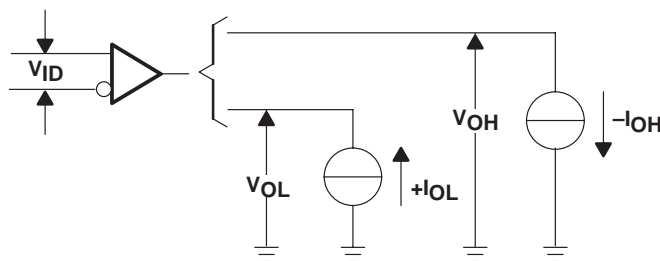
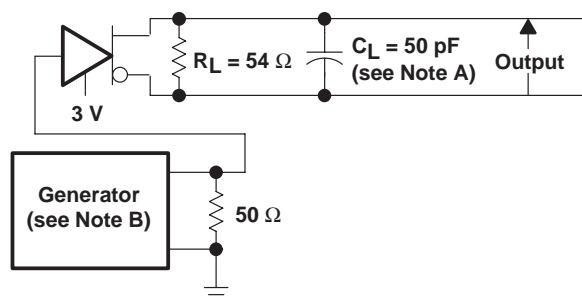
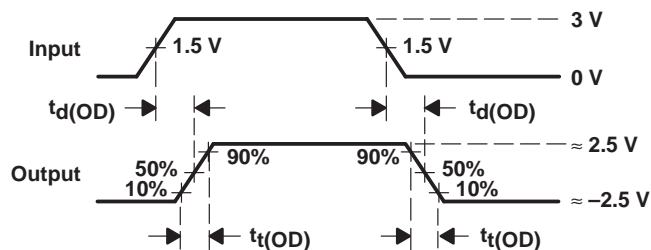


Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}



TEST CIRCUIT



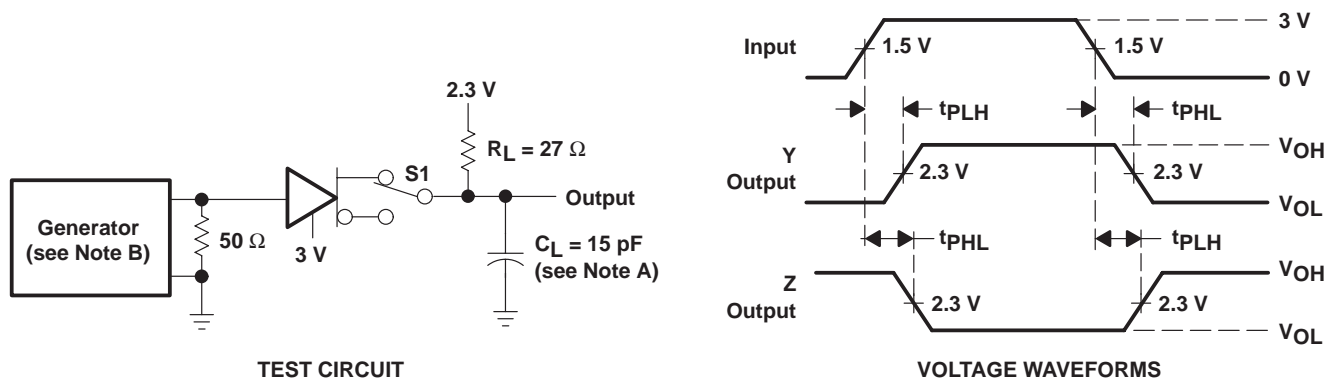
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $Z_O = 50\ \Omega$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$.

Figure 3. Driver Differential Output-Delay and Transition-Time Test Circuit and Voltage Waveforms

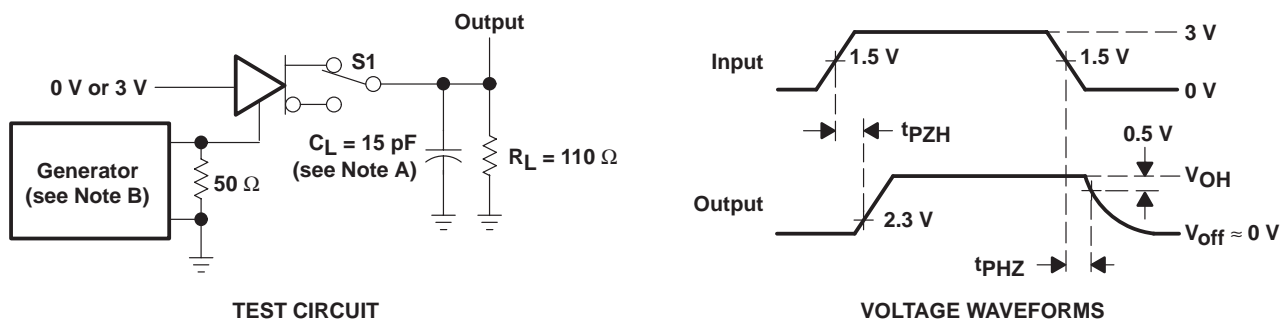
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $Z_O = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

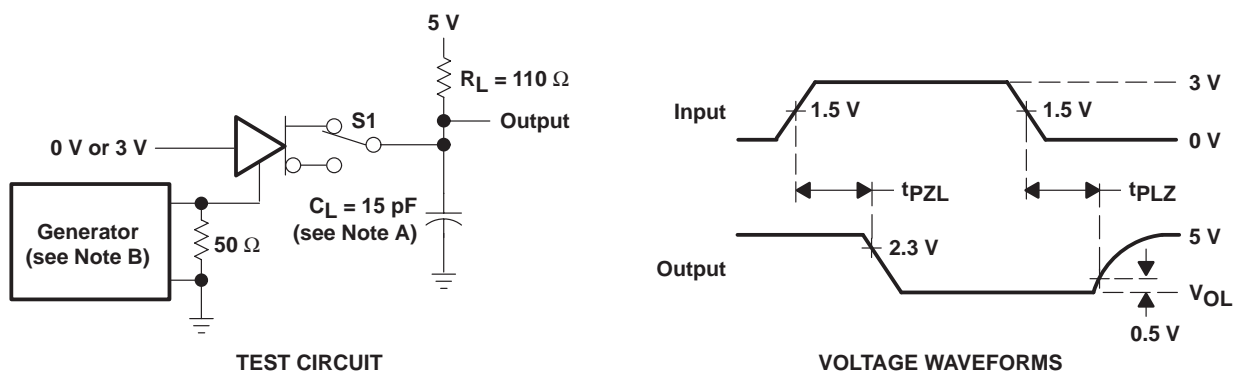
Figure 4. Driver Propagation-Time Test Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $Z_O = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

Figure 5. Driver Enable- and Disable-Time Test Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.

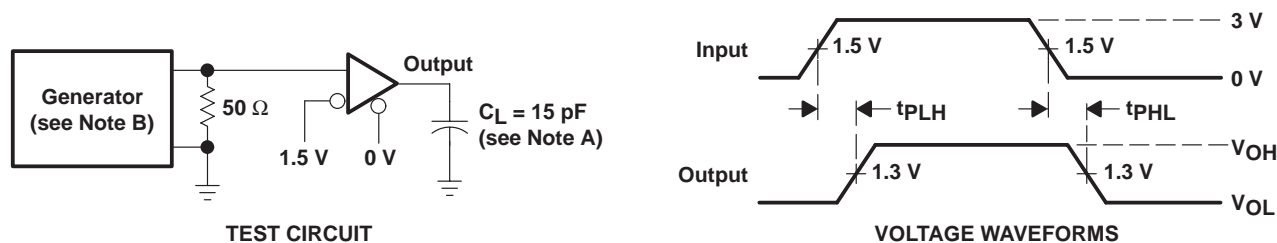
B. The pulse generator has the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $Z_O = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

Figure 6. Driver Enable- and Disable-Time Test Circuit and Voltage Waveforms

SN751177, SN751178 DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

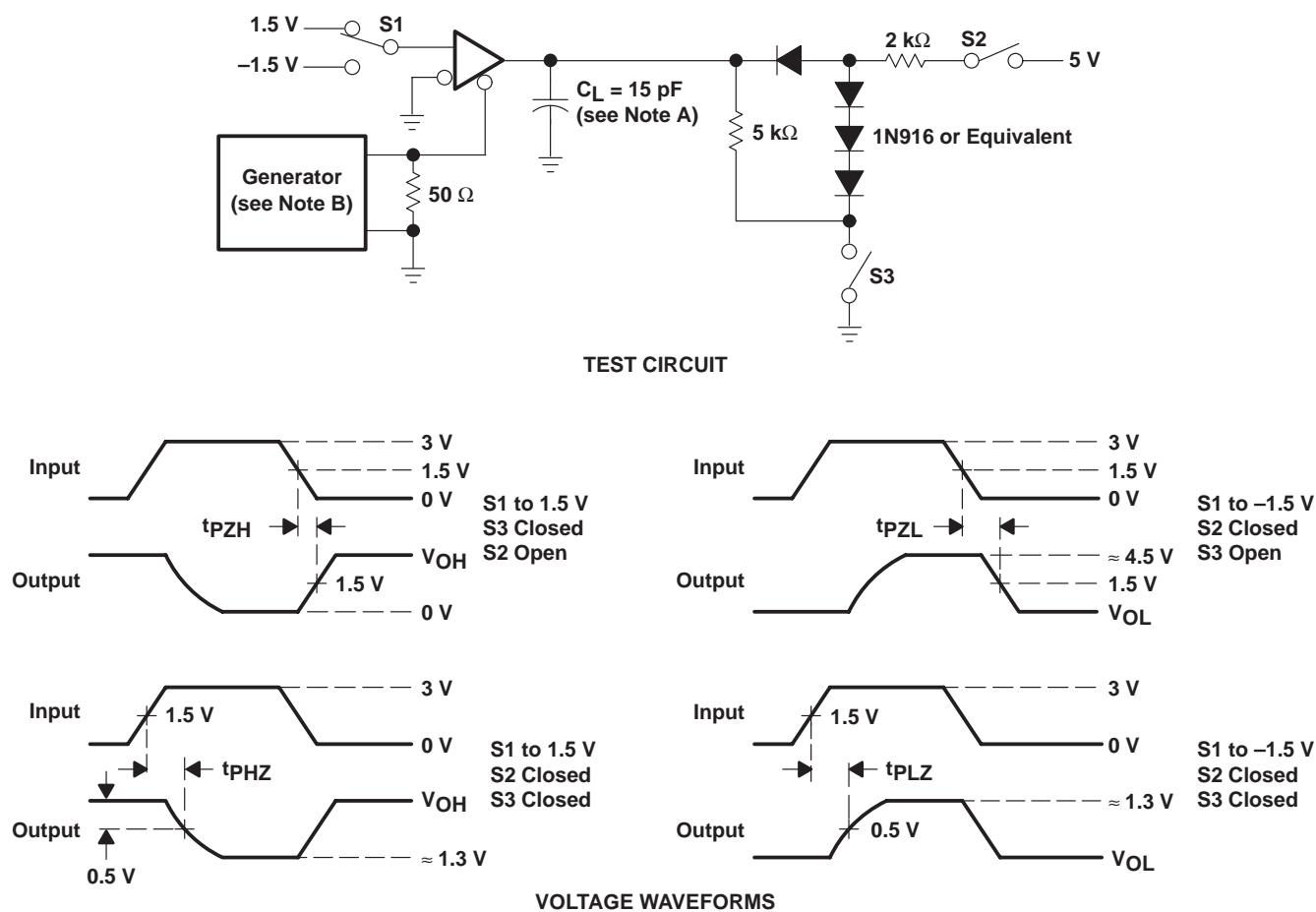
SLLS059D – FEBRUARY 1990 – REVISED MAY 1999

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $\text{PRR} \leq 1\ \text{MHz}$, 50% duty cycle, $Z_O = 50\ \Omega$, $t_r \leq 6\ \text{ns}$, $t_f \leq 6\ \text{ns}$.

Figure 7. Receiver Propagation-Time Test Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $\text{PRR} \leq 1\ \text{MHz}$, 50% duty cycle, $Z_O = 50\ \Omega$, $t_r \leq 6\ \text{ns}$, $t_f \leq 6\ \text{ns}$.

Figure 8. Receiver Output Enable- and Disable-Time Test Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.