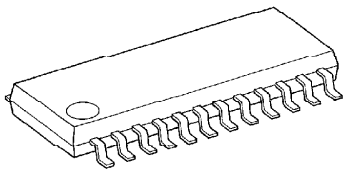
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT MULTICHIP

TB6512AF

PWM CHOPPER TYPE BIPOLAR STEPPING MOTOR DRIVER

The TB6512AF is PWM chopper type sinusoidal micro step bipolar stepping motor driver.
Sinusoidal micro step operation is accomplished only a clock signal inputting by means of built-in hard ware.



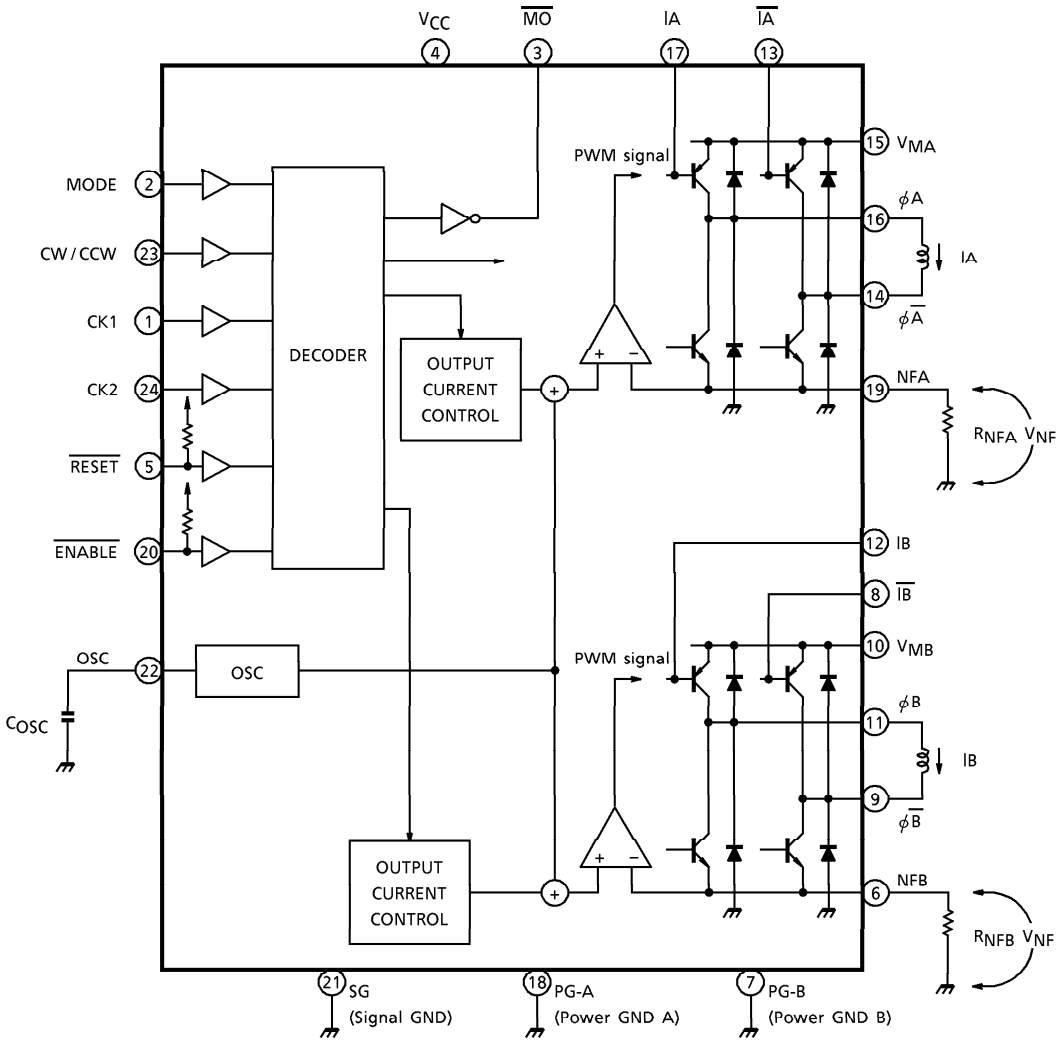
SSOP24-P-300-1.00B

Weight : 0.27g (Typ.)

FEATURES

- 1 chip bipolar sinusoidal micro step stepping motor driver.
- Output Current up to 150mA
- PWM chopper type.
- Structured by high voltage Bi-CMOS process technology.
- Forward and reverse rotation are available.
- 1-2, 2W1-2 phase 1 or 2 clock drives are selectable.
- Package : SSOP24-P-300B
- Input Pull-Up Resistor equipped with RESET and ENABLE Terminal : R = 500kΩ (Typ.)
- Output Monitor available with $\overline{MO}$. $I_{O\,(\overline{MO})}$ = ±2mA MAX.
- Reset and Enable are available with $\overline{RESET}$ and $\overline{ENABLE}$.

BLOCK DIAGRAM

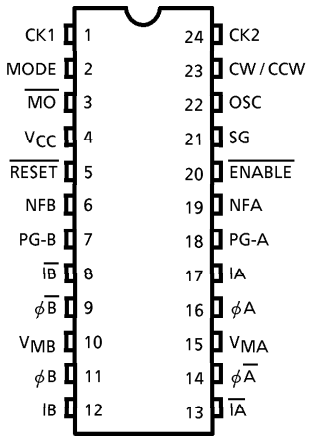


⑤, ⑳ : Pull-up Resistor 500kΩ (Typ.)

PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION	
1	CK1	CLOCK Signal Input terminal	Truth table A
2	MODE	Excitation Mode Setting terminal	Truth table B
3	$\overline{MO}$	Monitor Output terminal	
4	V_{CC}	Power voltage supply terminal for Logic	
5	$\overline{RESET}$	Reset Signal Input terminal	Truth table A
6	NFB	B Channel current detective terminal	
7	PG-B	Power GND B terminal	
8	$I\overline{B}$	Upper PNP Transistor Base terminal	
9	$\phi\overline{B}$	Output $\overline{B}$ terminal	
10	V_{MB}	Power voltage supply terminal for Motor B	
11	ϕB	Output B terminal	
12	IB	Upper PNP Transistor Base terminal	
13	$I\overline{A}$	Upper PNP Transistor Base terminal	
14	$\phi\overline{A}$	Output $\overline{A}$ terminal	
15	V_{MA}	Power voltage supply terminal for Motor A	
16	ϕA	Output A terminal	
17	IA	Upper side PNP Transistor Base terminal	
18	PG-A	Power GND $\overline{A}$ terminal	
19	NFA	A Channel current detective terminal	
20	$\overline{ENABLE}$	ENABLE Signal Input terminal	Truth table A
21	SG	Signal GND terminal	
22	OSC	Internal Oscillation frequency detective terminal	
23	CW / CCW	Forward rotation / Reverse rotation signal Input	Truth table A
24	CK2	Clock signal Input terminal	

PIN CONNECTION



TRUTH TABLE A

INPUT					MODE
CK1	CK2	CW / CCW	$\overline{RESET}$	$\overline{ENABLE}$	
⌐‾	H	L	H	L	CW
⌐‾¬	L	L	H	L	INHIBIT
H	⌐‾	L	H	L	CCW
L	⌐‾¬	L	H	L	INHIBIT
⌐‾	H	H	H	L	CCW
⌐‾¬	L	H	H	L	INHIBIT
H	⌐‾	H	H	L	CW
L	⌐‾¬	H	H	L	INHIBIT
X	X	X	L	L	INITIAL
X	X	X	X	H	Z

Z : High Impedance
X : Don't Care

(Note) Do not use INHIBIT MODE

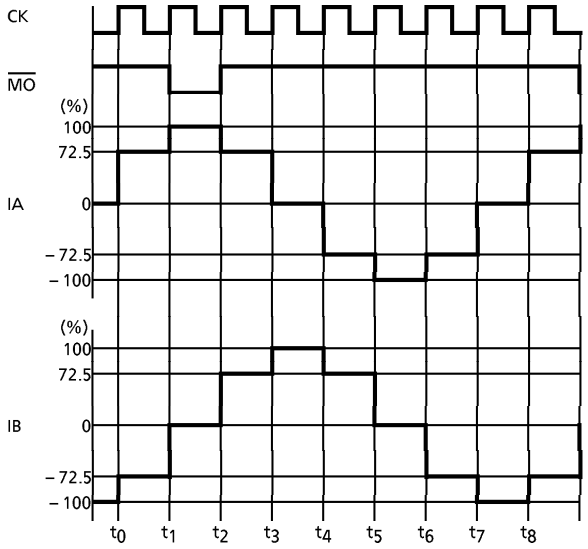
TRUTH TABLE B

INPUT / MODE	MODE (EXCITATION)
L	1-2 phase
H	2W1-2 phase

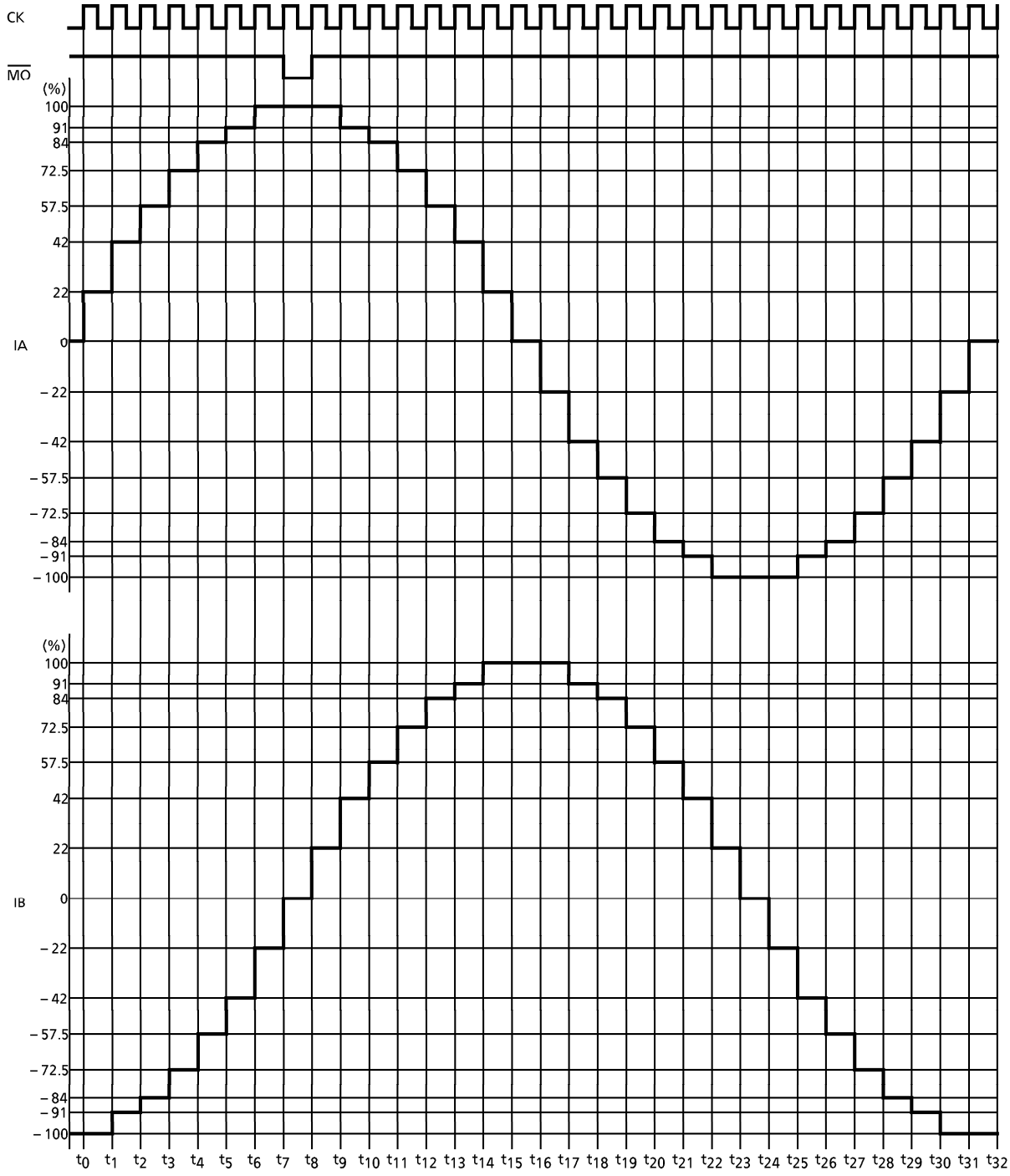
INITIAL MODE

EXCITATION MODE	I_{OUT} (A)	I_{OUT} (B)
1-2 phase	100%	0%
2W1-2 phase	100%	0%

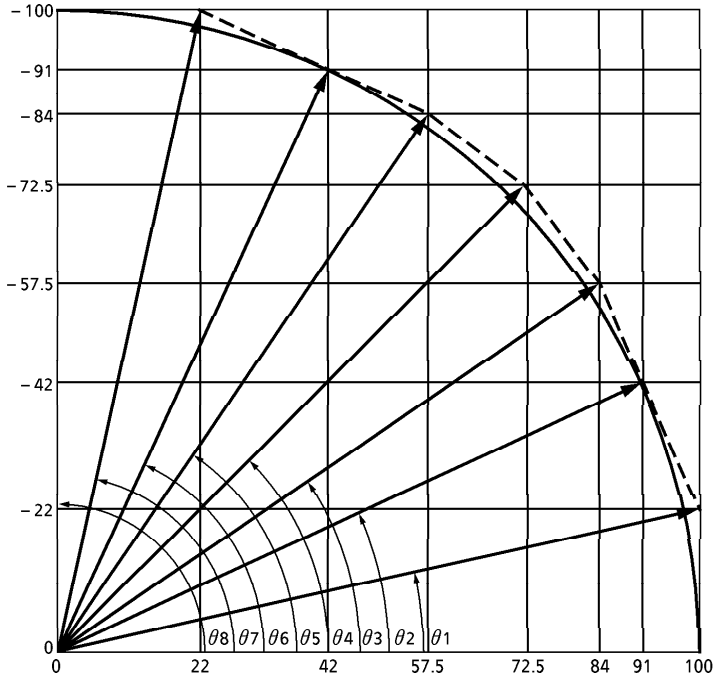
1-2 PHASE EXCITATION (MODE : L, CW mode)



2W1-2 PHASE EXCITATION (MODE : H, CW mode)

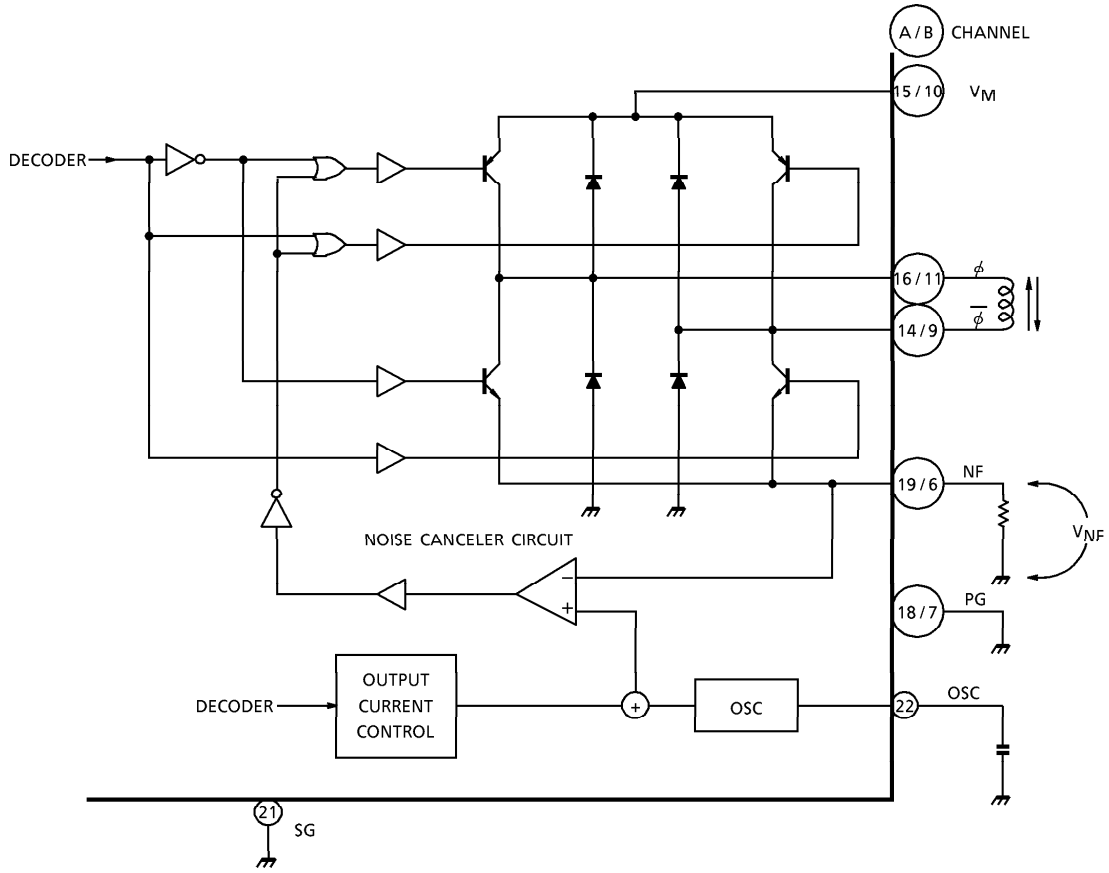


OUTPUT CURRENT VECTOR OR BIT (Normalize to 90 deg for each one step)



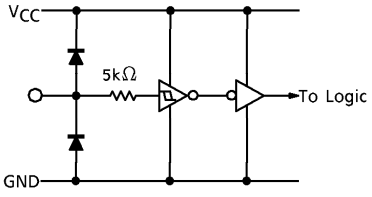
θ	ROTATION ANGLE		VECTOR LENGTH	
	IDEAL	TB6512AF	IDEAL	TB6512AF
θ0	0°	0°	100	100.00
θ1	11.25°	12.41°	100	102.39
θ2	22.5°	27.78°	100	100.22
θ3	33.75°	34.39°	100	101.80
θ4	45°	45°	100	102.53
θ5	56.25°	55.61°	100	101.81
θ6	67.5°	65.22°	100	100.22
θ7	78.75°	77.59°	100	102.39
θ8	90°	90°	100	100.00
			1-2 / 2W1-2 phase	

OUTPUT CIRCUIT

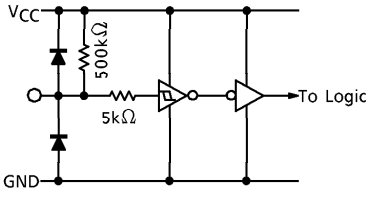


INPUT CIRCUIT

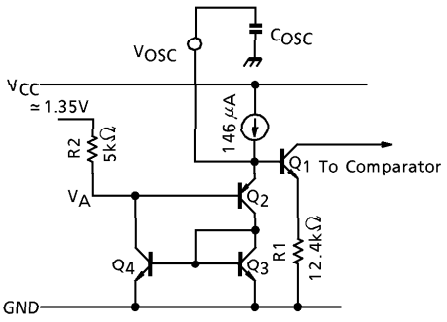
CK1, CK2, CW / CCW, MODE Terminals



$\overline{\text{RESET}}$, $\overline{\text{ENABLE}}$ Terminals



OSC Terminals



- OSC frequency calculation

Sawtooth OSC circuit consists of Q_1 through Q_4 and R_1 through R_4.
Q_2 is turned "off" when V_{OSC} is less than the voltage of $2.5V + V_{BE}$ Q_2 approximately equal to 2.05V.
V_{OSC} is increased by C_{OSC} charging through R_1.
Q_3 and Q_4 are turned "on" when V_{OSC} becomes 2.05V (Higher level.)
Lower level of $V_{㉒}$ pin is equal to V_{BE} $Q_2 + V_{SAT}$ Q_4 approximately equal to 1.4V.
V_{OSC} is calculated by following equation.
Assuming that $V_{OSC} = 1.4V$ $(t = t_1)$ and $= 2.05$ $(t = t_2)$
C_{OSC} is external capacitance connected to pin㉒ and R_1 is on-chip 10kΩ resistor.
Therefore, OSC frequency is calculated as follows.

$$t_1 = \frac{1.0\ C_{OSC}}{146 \times 10^{-6}}$$

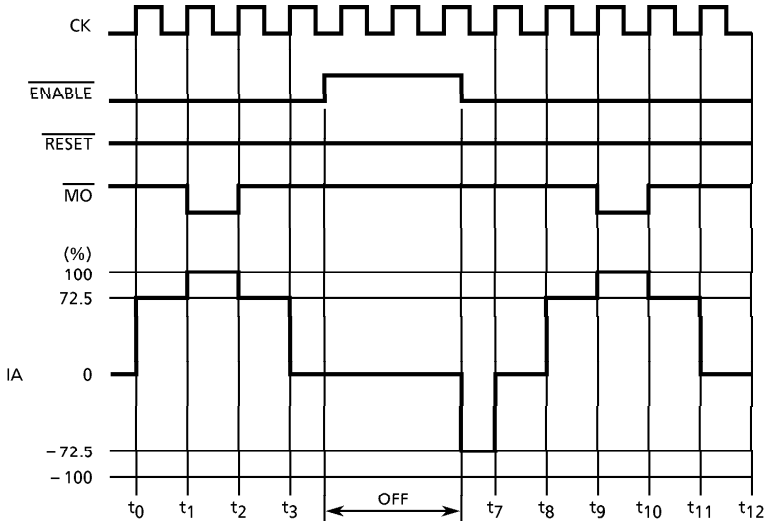
$$t_2 = \frac{2.05 \cdot C_{OSC}}{146 \times 10^{-6}}$$

$$f_{OSC} = \frac{1}{t_2 - t_1} = \frac{146 \times 10^{-6}}{C_{OSC}\ (2.05 - 1.0)}$$

$$= \frac{0.139}{C_{OSC}}\ (\text{kHz})\ (C_{OSC}\ \text{unit} = \mu\text{F})$$

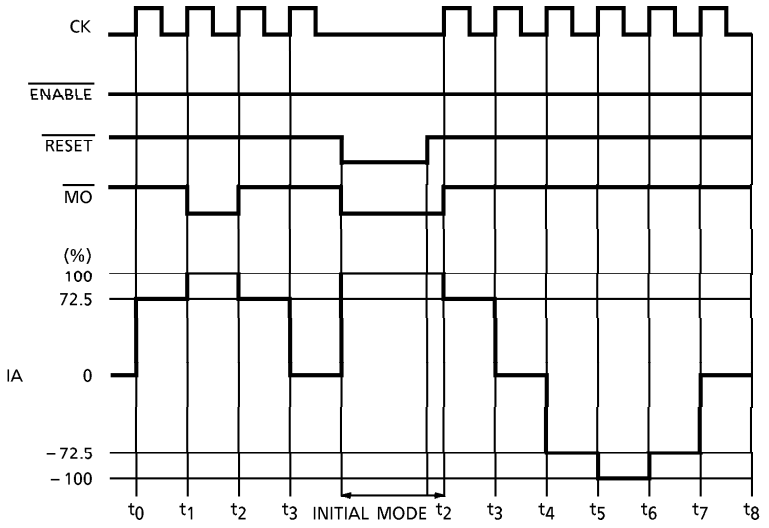
$\overline{\text{ENABLE}}$ AND $\overline{\text{RESET}}$ FUNCTION AND $\overline{\text{MO}}$ SIGNAL

Fig.1. 1-2 phase drive mode (MODE : L)



$\overline{\text{ENABLE}}$ signal disables only Output signal. Internal logic functions are proceeded by CK signal without regard to $\overline{\text{ENABLE}}$ signal.
Therefore, Output Current is initiated from the proceeded timing point of internal logic circuit, after release of disable mode.
Fig.1 shows the $\overline{\text{ENABLE}}$ functions, when the system is selected in 1-2 phase drive mode.

Fig.2. 1-2 phase drive mode (MODE : L)



As $\overline{\text{RESET}}$ is low, the decoder is initialized and $\overline{\text{MO}}$ is low.
After $\overline{\text{RESET}}$ is high, the motion is resumed from next clock as show in Fig.2.
$\overline{\text{MO}}$ (Monitor Output) signals is used as rotation and initial signal for stable. rotation checking.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	5.5	V
Output Voltage		$V_{M\ (opr.)}$	4.0~10.0	V
		$V_{M\ (MAX.)}$	12.0	
Output Current		$I_{O\ (MAX.)}$	120	mA
	AVE.	$I_{O\ (\overline{MO})}$	±2	
Input Voltage		V_{IN}	~V_{CC}	V
Power Dissipation		P_D	0.83 (Note 1)	W
			1.04 (Note 2)	
Operating Temperature		T_{opr}	−30~85	°C
Storage Temperature		T_{stg}	−55~150	°C
Feed Back Voltage		V_I	1.0	V

(Note 1) No heat sink
(Note 2) With heat sink (50 × 50 × 1.6mm Cu 10%)

RECOMMENDED OPERATING CONDITIONS (Ta = −30~85°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V_{CC\ (opr.)}$		2.7	3.0	5.5	V
Output Voltage	$V_{M\ (opr.)}$		4.0	—	10.0	V
Output Current	I_{OUT}		—	—	100	mA
Input Voltage	V_{IN}		—	—	V_{CC}	V
Clock Frequency	f_{CLOCK}		—	—	5	kHz
OSC Frequency	f_{OSC}		15	—	80	kHz

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, (Ta = 25°C, V_{CC} = 3V, V_M = 5V, L = 20mH / R = 0.5Ω)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	High	$V_{IN\ (H)}$	1	MODE, CW / CCW, $\overline{ENABLE}$ CK1, CK2, $\overline{RESET}$	V_{CC} × 0.7	—	V_{CC} + 0.4	V
	Low	$V_{IN\ (L)}$			GND − 0.4	—	GND × 0.3	
Input Hysteresis Voltage		V_H			—	600	—	mV
Input Current		$I_{IN\text{-}1\ (H)}$	1	M1, M2, REF IN, V_{IN} = 5.0V	—	—	100	nA
		$I_{IN\text{-}1\ (L)}$		$\overline{RESET}$, V_{IN} = 0V, $\overline{ENABLE}$ Internal pull-up resistor	3	6	12	μA
		$I_{IN\text{-}2\ (L)}$		V_{IN} = 0V	—	—	100	nA
Quiescent Current V_{CC}		I_{CC1}	2	Output open, $\overline{RESET}$: H, $\overline{ENABLE}$: L, (1-2 phase excitation)	—	5	9	mA
		I_{CC2}		Output open, $\overline{RESET}$: H, $\overline{ENABLE}$: L (2W1-2 phase excitation)	—	5	9	
		I_{CC3}		$\overline{RESET}$: L, $\overline{ENABLE}$: H	—	1.3	—	
		I_{CC4}		$\overline{RESET}$: H, $\overline{ENABLE}$: H	—	1.3	—	
Comparator Reference Voltage		V_{NF}	3	R_{NF} = 2.5Ω, C_{OSC} = 0.0033μF	0.22	0.25	0.28	V
Output Diffirencial		ΔV_O	—	B / A, C_{OSC} = 0.0033μF R_{NF} = 2.5Ω	− 10	—	10	%
Maximum OSC Frequency		$f_{OSC\ (MAX.)}$	—		100	—	—	kHz
Minimum OSC Frequency		$f_{OSC\ (MIN.)}$	—		—	—	10	kHz
OSC Frequency		f_{OSC}	—	C_{OSC} = 0.0033μF	31	44	70	kHz
Output Voltage		$V_{OH\ (MO)}$	—	I_{OH} = − 40μA	2.5	—	V_{CC}	V
		$V_{OL\ (MO)}$	—	I_{OL} = 40μA	GND	0.1	0.5	

Output block

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Saturation Voltage	Upper Side		$V_{SAT\ U1}$	4	I_{OUT} = 0.12A		—	0.08	0.23	V
	Lower Side		$V_{SAT\ L1}$				—	0.16	0.43	
	Upper Side		$V_{SAT\ U2}$		I_{OUT} = 0.06A		—	0.06	—	
	Lower Side		$V_{SAT\ L2}$				—	0.10	—	
Diode Forward Voltage	Upper Side		$V_{F\ U1}$	5	I_{OUT} = 0.12A		—	1.13	1.8	V
	Lower Side		$V_{F\ L1}$				—	0.95	1.6	
Output Dark Current (A + B Channels)			I_{M1}	2	$\overline{ENABLE}$: "H" level $\overline{RESET}$: "L" level Output open		—	—	50	μA
			I_{M2}		$\overline{ENABLE}$: "L" level $\overline{RESET}$: "H" level Output open		—	17	28	mA
NF Dark Current (1 Channels)			I_{NF}		$\overline{ENABLE}$: "L" level $\overline{RESET}$: "H" level Output open		1	2.5	7	
A-B Chopping Current (Note)	2W1-2φ	1-2φ	VECTOR	3	θ = 0	R_{NF} = 2.5Ω C_{OSC} = 0.0033μF	—	100	—	%
	2W1-2φ	—			θ = 1 / 8		—	100	—	
	2W1-2φ	—			θ = 2 / 8		86	91	96	
	2W1-2φ	—			θ = 3 / 8		79	84	89	
	2W1-2φ	1-2φ			θ = 4 / 8		67.5	72.5	77.5	
	2W1-2φ	—			θ = 5 / 8		52.5	57.5	62.5	
	2W1-2φ	—			θ = 6 / 8		37	42	47	
	2W1-2φ	—			θ = 7 / 8		17	22	27	

(Note) Maximum current (θ = 0) : 100%
2W1-2φ : 2W1, 2 phase excitation mode
W1-2φ : W1, 2 phase excitation mode
1-2φ : 1, 2 phase excitation mode

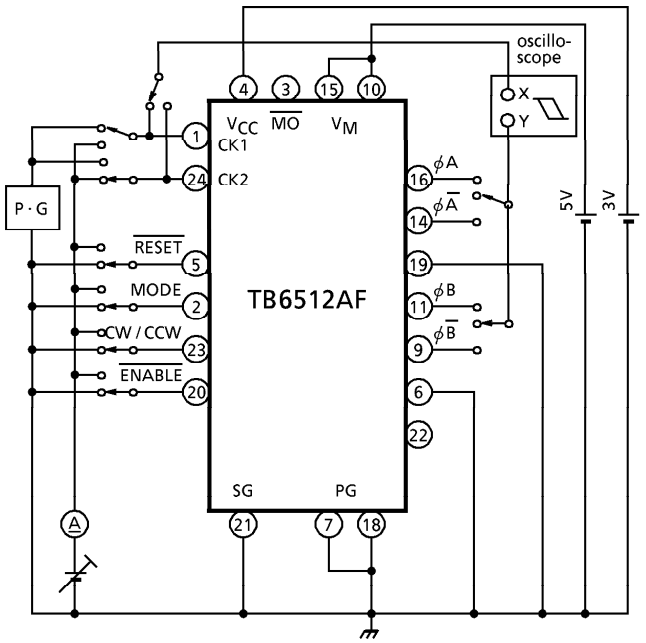
ELECTRICAL CHARACTERISTICS

Unless otherwise specified, (Ta = 25°C, V_{CC} = 3V, V_M = 5V, L = 20mH / R = 0.5Ω)

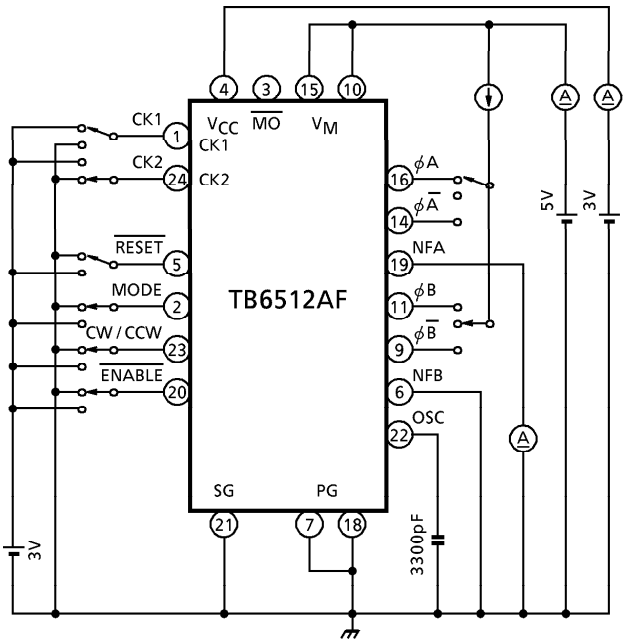
CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
A-B Chopping Current (Note)	2W1-2φ	1-2φ	VECTOR	3	θ = 0	R_{NF} = 3.3Ω, C_{OSC} = 0.0033μF, L = 5mH / R = 50Ω	—	100	—	%
	2W1-2φ	—			θ = 1 / 8		—	100	—	
	2W1-2φ	—			θ = 2 / 8		—	91.1	—	
	2W1-2φ	—			θ = 3 / 8		—	83.6	—	
	2W1-2φ	1-2φ			θ = 4 / 8		—	72.6	—	
	2W1-2φ	—			θ = 5 / 8		—	60.0	—	
	2W1-2φ	—			θ = 6 / 8		—	44.5	—	
	2W1-2φ	—			θ = 7 / 8		—	24.3	—	
Reference Voltage			ΔV_{NF}		Δθ = 0 / 8 – 1 / 8	R_{NF} = 2.5Ω, C_{OSC} = 0.0033μF	—	0	—	mV
					Δθ = 1 / 8 – 2 / 8		10	22.5	35	
					Δθ = 2 / 8 – 3 / 8		5	17.5	30	
					Δθ = 3 / 8 – 4 / 8		16.25	28.75	41.25	
					Δθ = 4 / 8 – 5 / 8		25	37.5	50	
					Δθ = 5 / 8 – 6 / 8		26.25	38.75	51.25	
					Δθ = 6 / 8 – 7 / 8		37.5	50	62.5	
Output Tr Switching Characteristics			t_r	7	R_L = 2Ω, V_{NF} = 0V, C_L = 15pF		—	0.3	—	μs
			t_f				—	2.2	—	
			t_{pLH}		CK~Output		—	1.5	—	
			t_{pHL}				—	2.7	—	
			t_{pLH}		OSC~Output		—	5.4	—	
			t_{pHL}				—	6.3	—	
			t_{pLH}		$\overline{RESET}$~Output		—	2.0	—	
			t_{pHL}				—	2.5	—	
			t_{pLH}		$\overline{ENABLE}$~Output		—	5.0	—	
			t_{pHL}				—	6.0	—	
Output Leakage Current	Upper Side		I_{OH}	6	V_M = 12V		—	—	50	μA
	Lower Side		I_{OL}				—	—	50	

(Note) Maximum current (θ = 0) : 100%
2W1-2φ : 2W1, 2 phase excitation mode
W1-2φ : W1, 2 phase excitation mode
1-2φ : 1,2 phase excitation mode

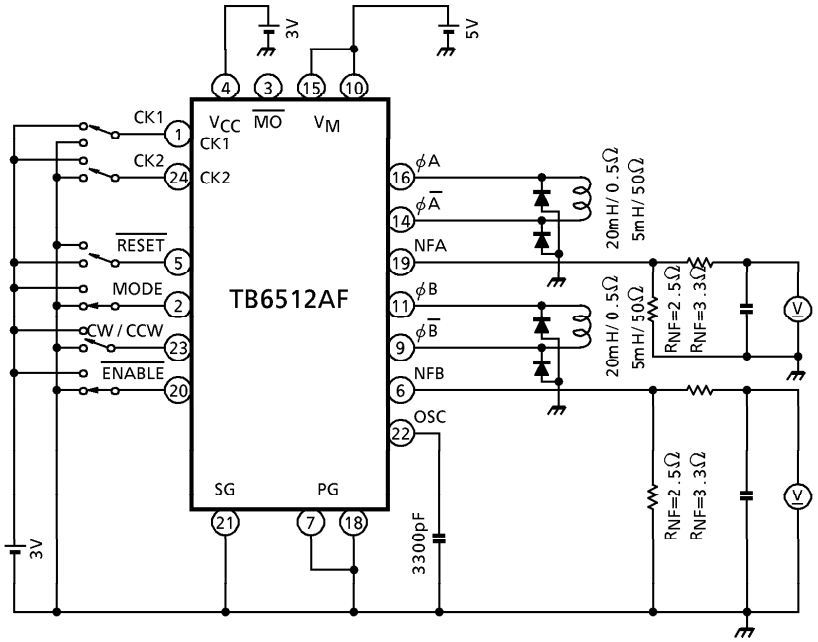
TEST CIRCUIT 1 : V_{IN} (H), (L), I_{IN} (H), (L)



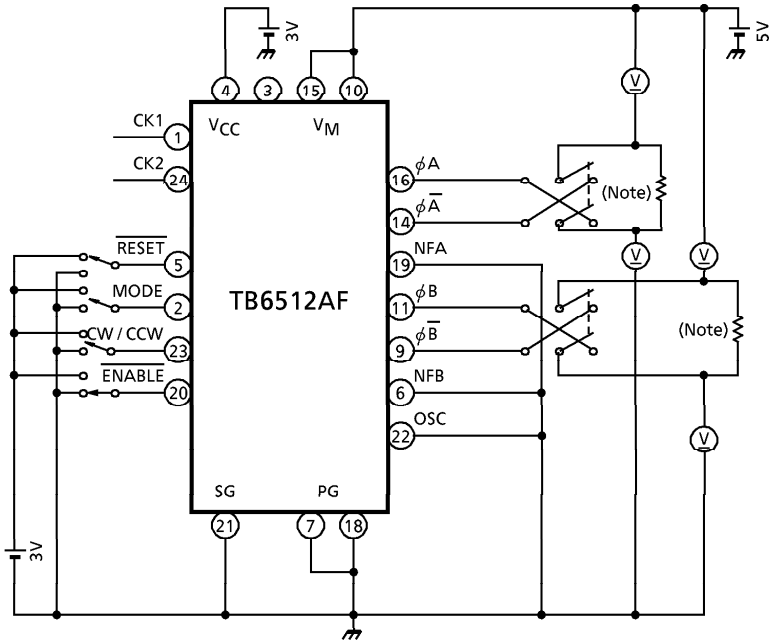
TEST CIRCUIT 2 : I_{CC}, I_M, I_{NF}



TEST CIRCUIT 3 : V_{NF}

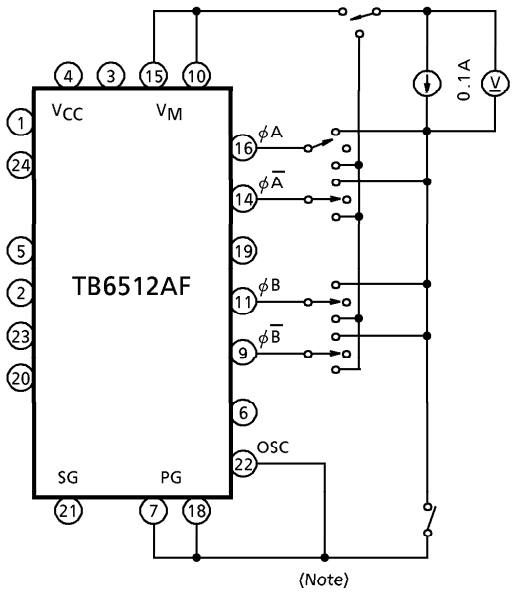


TEST CIRCUIT 4 : $V_{CE\,(SAT)}$ Upper, lower

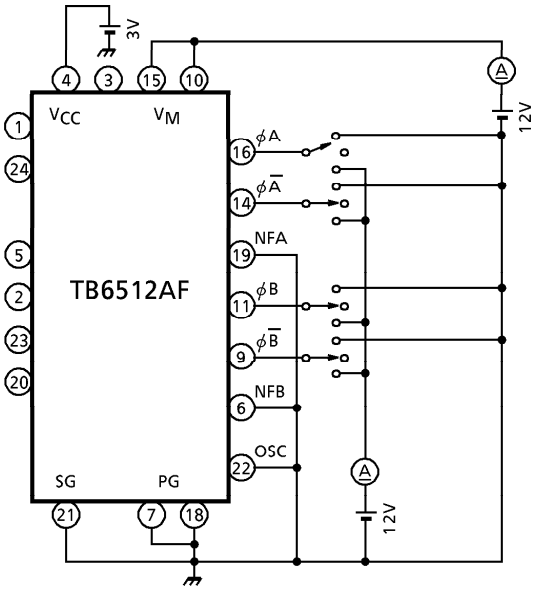


(Note) Calibrate Output Current becomes 0.06A (or 0.10A) with this resistor.

TEST CIRCUIT 5 : V_{F-U}, V_{F-L}



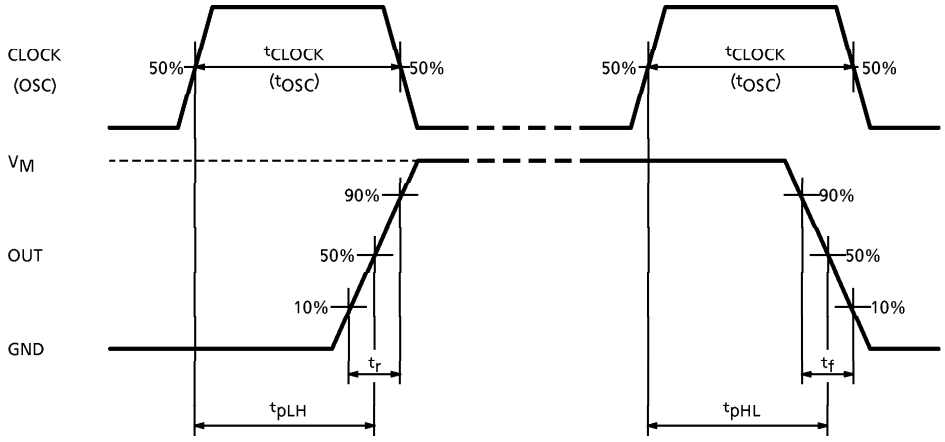
TEST CIRCUIT 6 : I_{OH}, I_{OL}

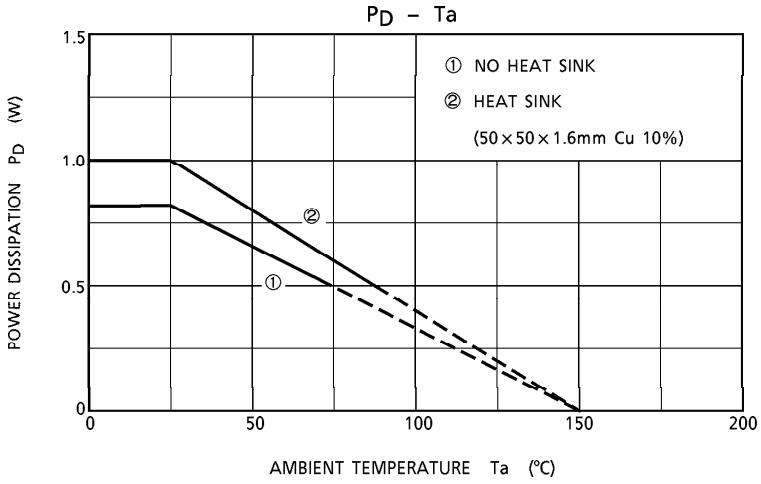


(Note) Not to take a GND with any non-connecting Pins.

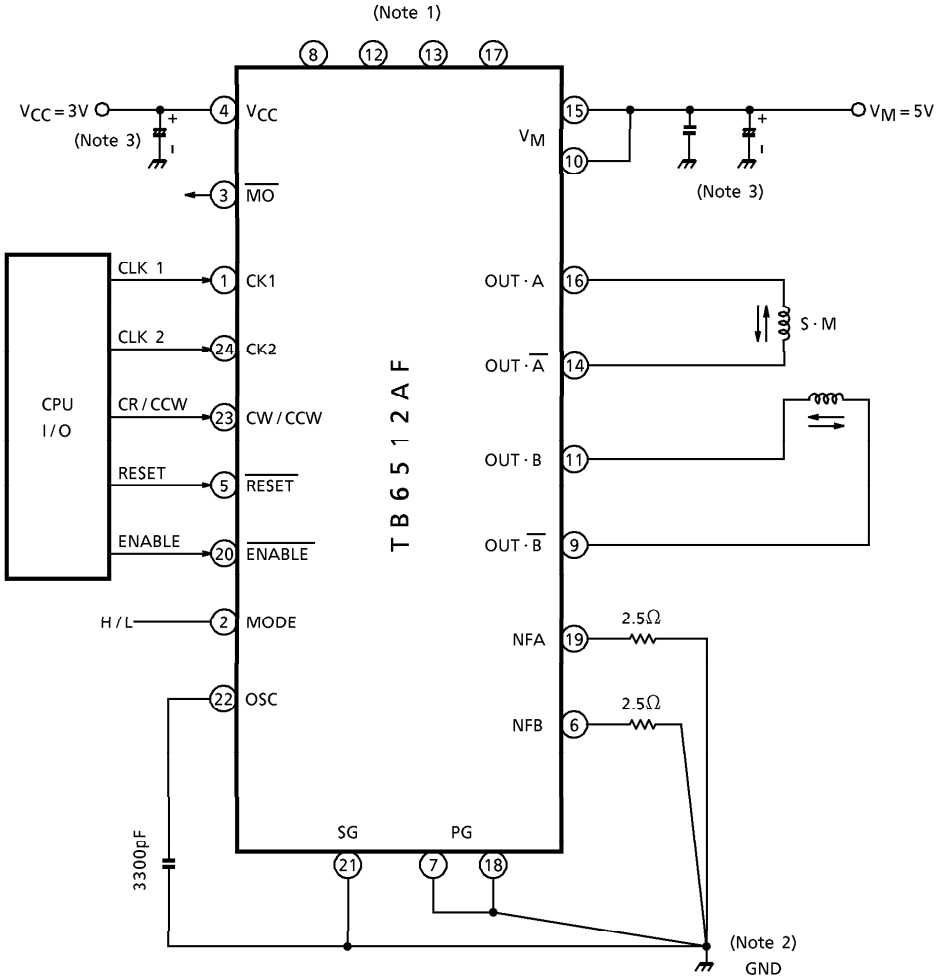
AC ELECTRICAL, CHARACTERICAL

CK (OSC) – OUT





APPLICATION CIRCUIT



(Note 1) ⑧, ⑫, ⑬, ⑰pin : open

(Note 2) GND pattern to be laid out at one point in order to prevent common impedance.

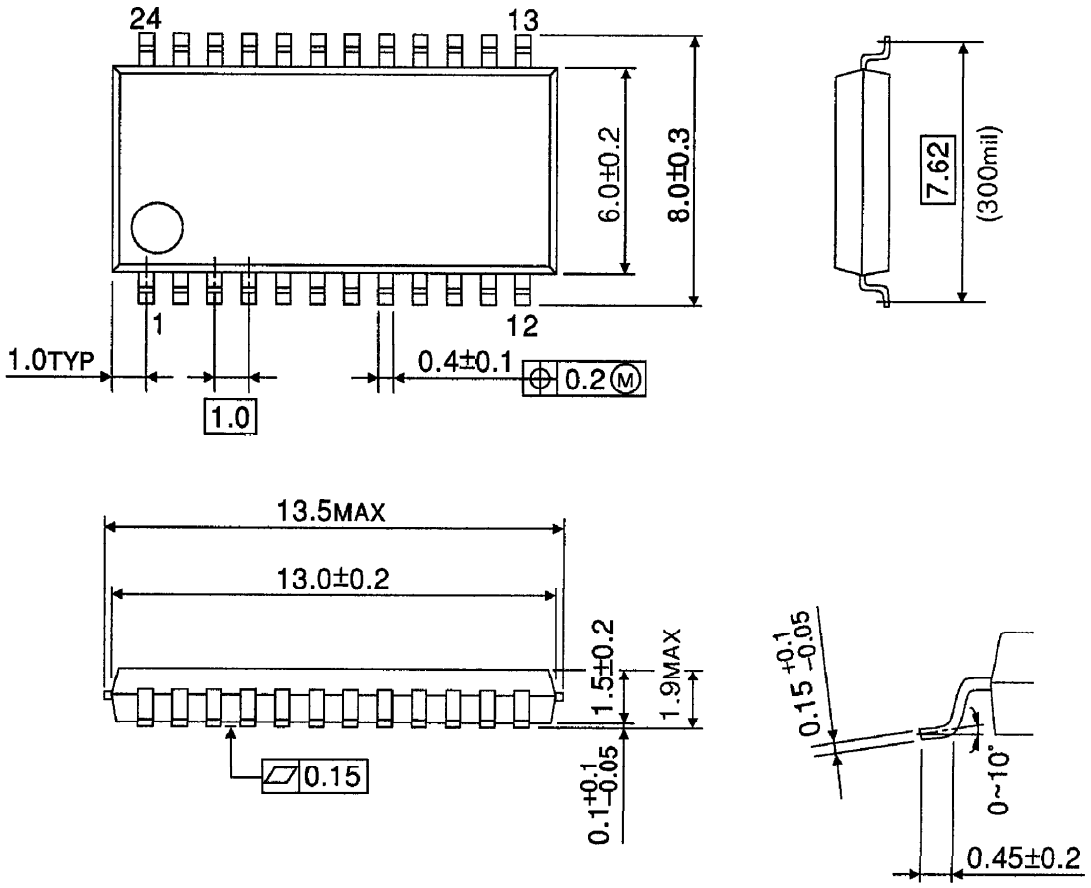
(Note 3) Capacitor for noise suppression to be connected between the Power Supply (V_{CC}, V_M) and GND to stabilize the operation.

(Note 4) Utmost care is necessary in the design of the output line, V_M and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING

SSOP24-P-300-1.00B

Unit : mm



Weight : 0.27g (Typ.)