August 1995
Edition 6.0b

FUJITSU

DATA SHEET

MB501L/504/504L

TWO MODULUS PRESCALERS

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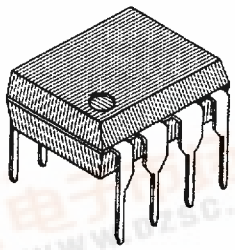
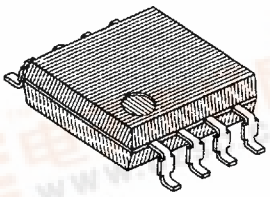
The Fujitsu MB501L/504/504L are two modulus prescalers, which are use with a frequency synthesizer to make a PLL (Phase Locked Loop). They will divide the input frequency by the modulus of 64/65 or 128/129 for the MB501L, and 32/33 or 64/65 for the MB504/MB504L. The MB501L and MB504L are low-power versions. The output of 1.6V peak to peak on ECL level applies to all.

- High Operating Frequency, Low Power Operation:
  1.1GHz at 50mW typ. (MB501L)
  520MHz at 50mW typ. (MB504)
  520MHz at 25mW typ. (MB504L)
- Pulse Swallow Function
- Wide Operation Temperature T_A = −40°C to +85°C
- Stable Output Amplitude: V_{OUT} = 1.6Vp-p
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package



PLASTIC PACKAGE
DIP-08P-M01



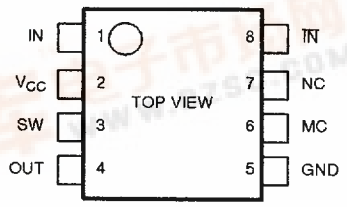
PLASTIC PACKAGE
FPT-08P-M01

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	V_O	10	mA
Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{STG}	− 55 to +125	°C

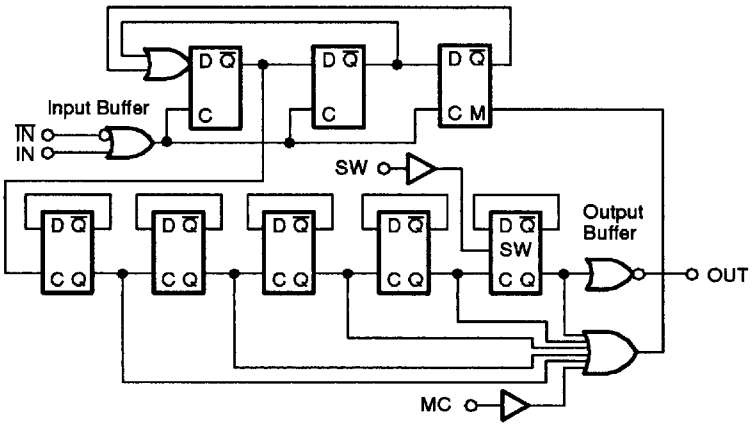
Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

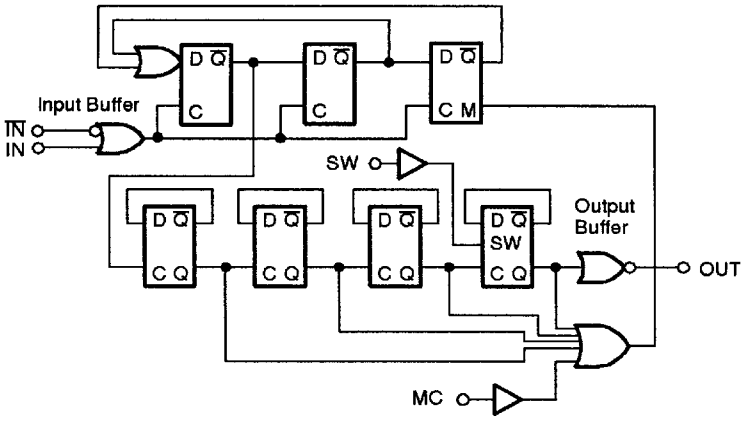
a) MB501L



	SW	MC	Divide Ratio
MB501/ MB501L	H	H	1/64
	H	L	1/65
	L	H	1/128
	L	L	1/129

Note: SW: H = V_{CC}, L = OPEN
MC: H = 2.0V to V_{CC},
L = GND to 0.8V

b) MB504/MB504L



	SW	MC	Divide Ratio
MB504/ MB504L	H	H	1/32
	H	L	1/33
	L	H	1/64
	L	L	1/65

Note: SW: H = V_{CC}, L = OPEN
MC: H = 2.0V to V_{CC},
L = GND to 0.8V

Figure 1. Block Diagrams

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	−40		+85	°C
Load Capacitance	C_L			12	pF

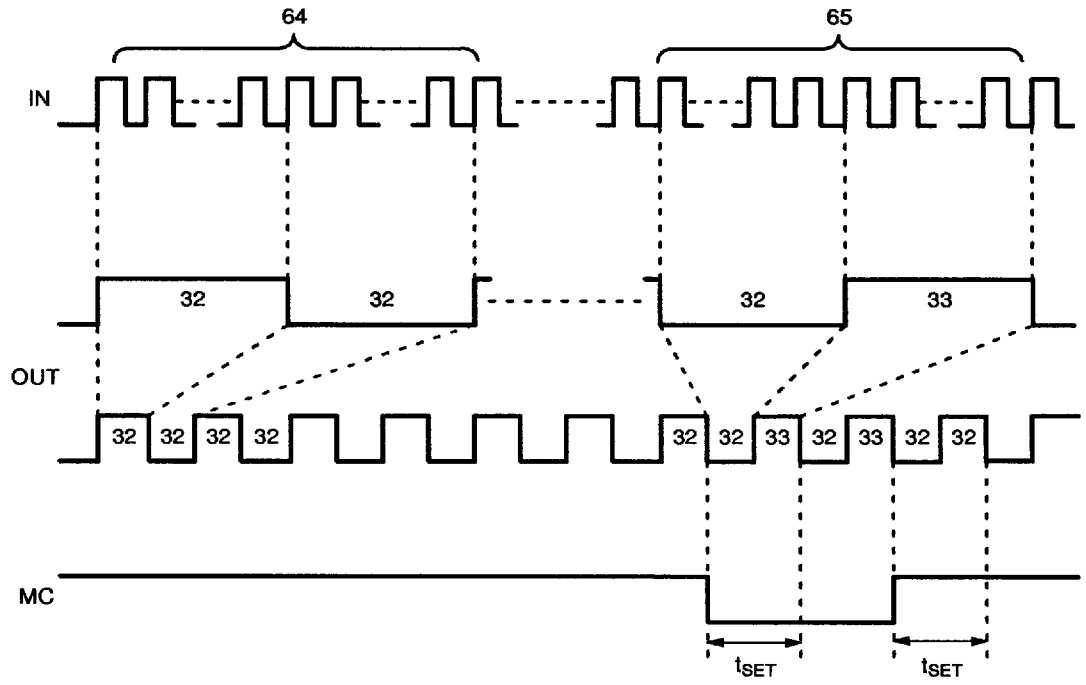
ELECTRICAL CHARACTERISTICS
(Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power Supply Current	MB501L	I_{CC}	I/O pins are open		10	14*	mA
	MB504				10	14*	mA
	MB504L				5	7*	mA
Output Amplitude		V_O		1.0	1.6		V_{P-P}
Input Frequency	MB501L	f_{IN}	With input coupling capacitor 1000pF	10		1100	MHz
	MB504			10		520	MHz
	MB504L			10		520	MHz
Input Signal Amplitude for IN	MB501L	P_{IN}		−4		5.5	dBm
	MB504			−12		10	dBm
	MB504L			−12		10	dBm
High Level Input Voltage for MC		V_{IHM}		2.0			V
Low Level Input Voltage for MC		V_{ILM}				0.8	V
High Level Input Voltage for SW		V_{IHS}**		V_{CC} −0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW		V_{ILS}		OPEN			V
High Level Input Current for MC		I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC		I_{ILM}	V_{IL} = 0.8V	−0.2			mA
Modulus Set-up Time MC to OUT	MB501L	t_{SET}			16	26	ns
	MB504				20	30	ns
	MB504L				18	28	ns

Note: * V_{CC} = 5V, T_A = 25°C
** Design Guarantee

MB501L TIMING CHART (2 MODULUS)

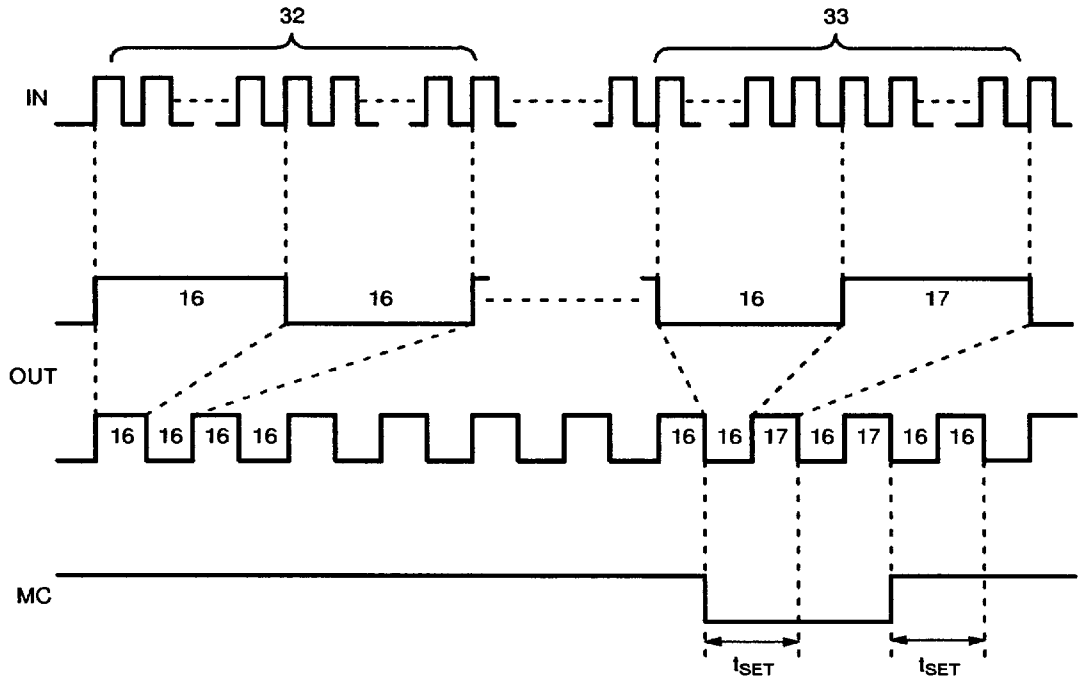
Example: Divide Ratio of 64/65



Note: When divide ratio of 65 is selected, positive pulse is applied by one to 33.
The typical set up time is 16ns (MB501L) from the MC signal input to the timing of change of prescaler divide ratio.

MB504/MB504L TIMING CHART (2 MODULUS)

Example: Divide Ratio of 32/33



Note: When divide ratio of 33 is selected, positive pulse is applied by one to 17.
The typical set up time is 20ns (MB504), 18ns (MB504L) from the MC signal input to the timing of change of prescaler divide ratio.

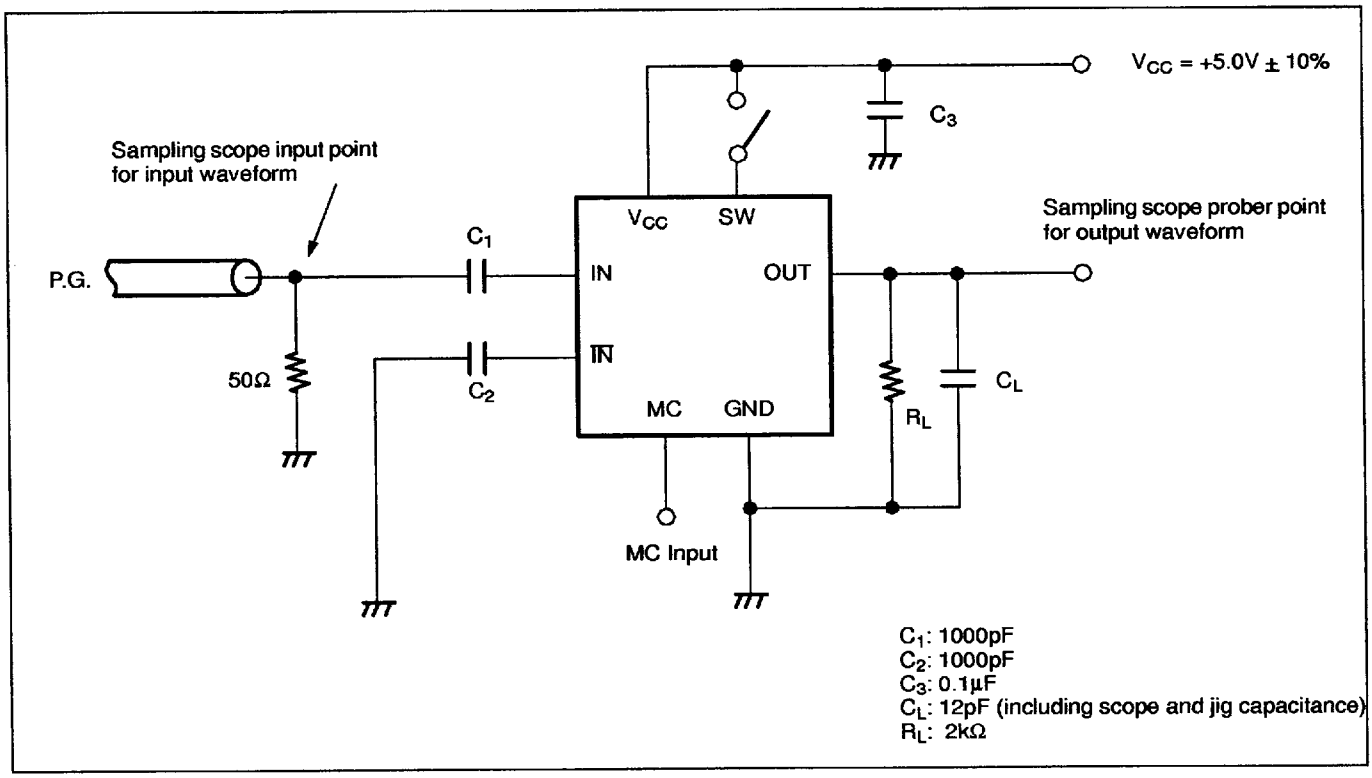


Figure 2. Test Circuit

TYPICAL CHARACTERISTICS CURVES

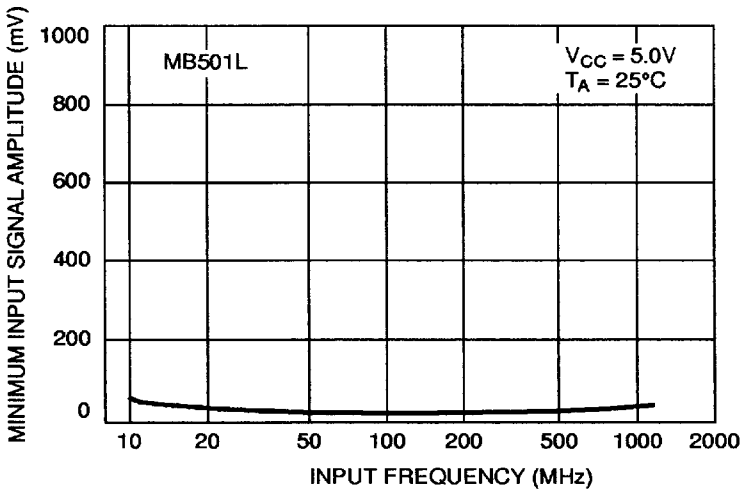


Figure 3. Input Signal Amplitude vs. Input Frequency

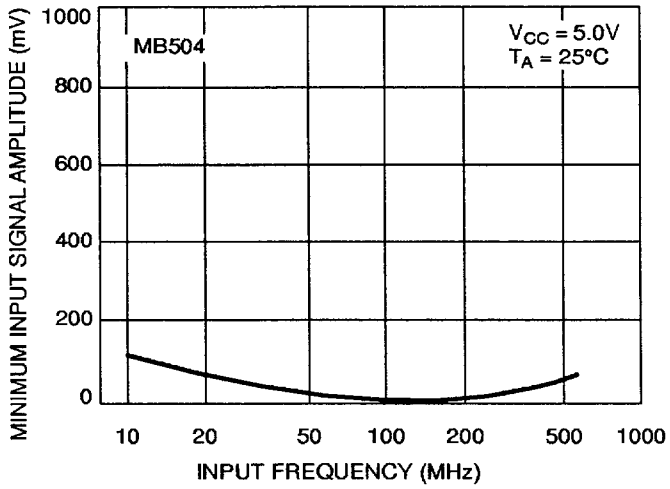


Figure 4. Input Signal Amplitude vs. Input Frequency

TYPICAL CHARACTERISTICS CURVES (Continued)

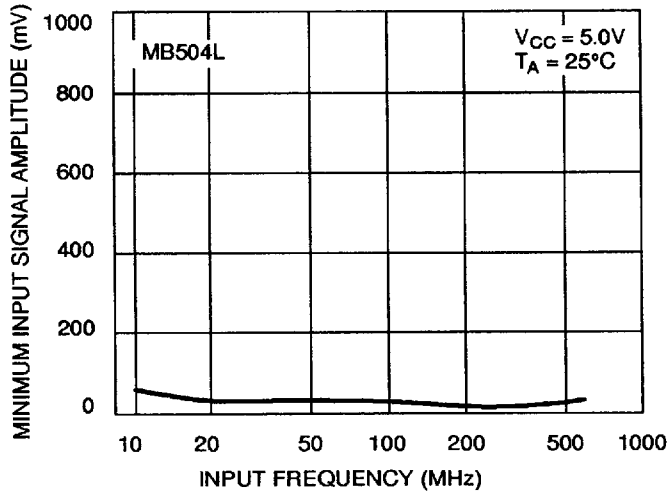
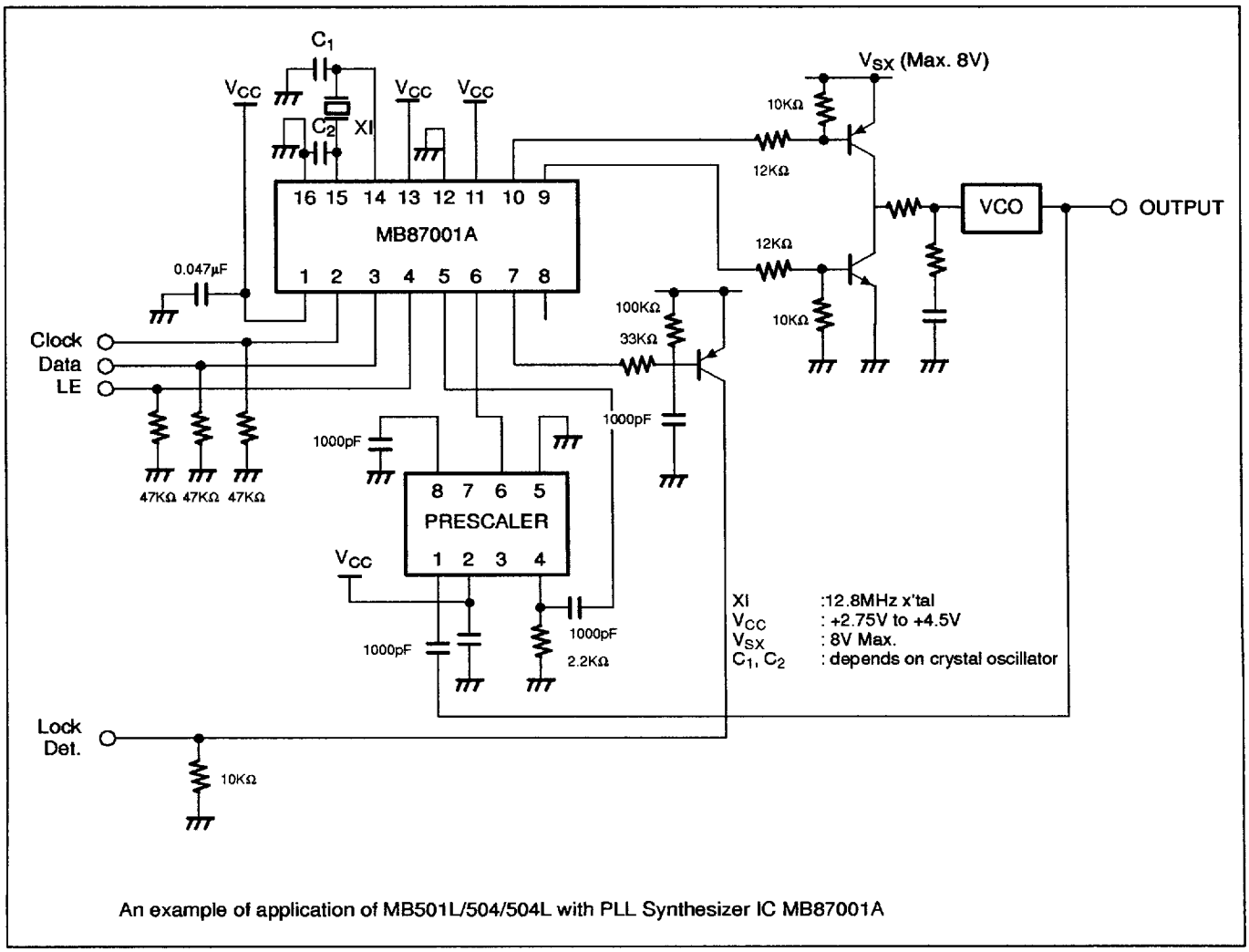


Figure 5. Input Signal Amplitude vs. Input Frequency

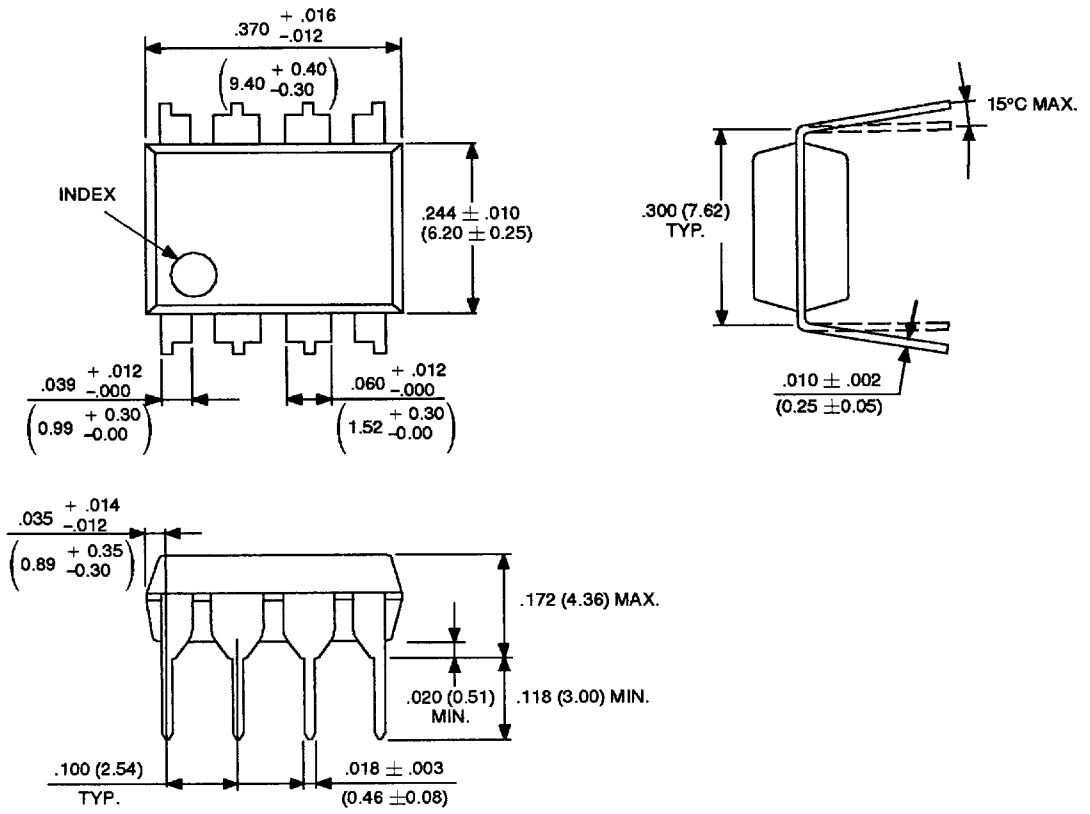


An example of application of MB501L/504/504L with PLL Synthesizer IC MB87001A

Figure 6. Typical Application Example

PACKAGE DIMENSIONS

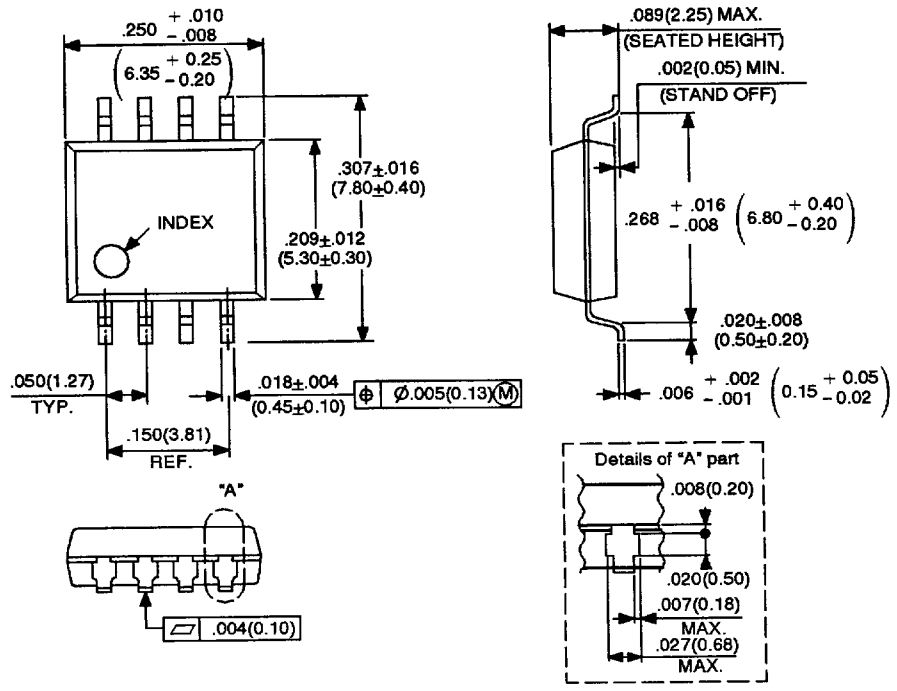
8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters).

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in inches (millimeters).