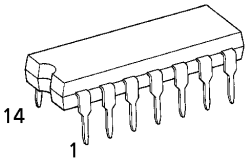
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC4001BP, TC4001BF, TC4001BFN, TC4001BFT

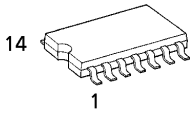
TC4001B QUAD 2 INPUT NOR GATE

The TC4001B is 2-input positive NOR gate, respectively.
Since the outputs of these gates are epuipped with the buffers, the input / output transmission characteristics have been improved and the variation of transmission time due to an increase in the load capacity is kept minimum.

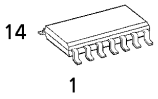
(Note) The JEDEC SOP (FN) is not available in Japan.



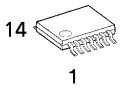
P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)



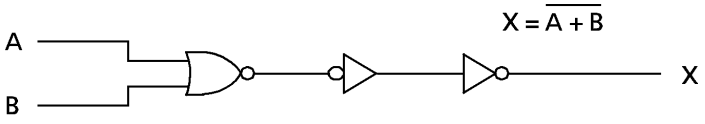
FT (TSSOP14-P-0044-0.65)
Weight : 0.06g (Typ.)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T_{opr}	– 40~85	°C
Storage Temperature Range	T_{stg}	– 65~150	°C

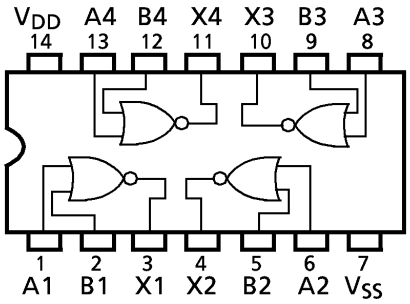
LOGIC DIAGRAM

1 / 4 TC4001B



PIN ASSIGNMENT (TOP VIEW)

TC4001B



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RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	−40°C MIN.	−40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.00 10.00 15.00	— — —	4.95 9.95 14.95	— — —	V
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	— — —	0.05 0.05 0.05	— — —	0.00 0.00 0.00	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
Output High Current	I_{OH}	V_{OH} = 4.6V V_{OH} = 2.5V V_{OH} = 9.5V V_{OH} = 13.5V $V_{IN} = V_{SS}$	5 5 10 15	−0.61 −2.50 −1.50 −4.00	— — — —	−0.51 −2.10 −1.30 −3.40	−1.0 −4.0 −2.2 −9.0	— — — —	−0.42 −1.70 −1.10 −2.80	— — — —	mA
Output Low Current	I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V $V_{IN} = V_{SS}, V_{DD}$	5 10 15	0.61 1.50 4.00	— — —	0.51 1.30 3.40	1.2 3.2 12.0	— — —	0.42 1.10 2.80	— — —	mA
Input High Voltage	V_{IH}	V_{OUT} = 0.5V V_{OUT} = 1.0V V_{OUT} = 1.5V $\|I_{OUT}\| < 1\mu A$	5 10 15	3.5 7.0 11.0	— — —	3.5 7.0 11.0	2.75 5.50 8.25	— — —	3.5 7.0 11.0	— — —	V
Input Low Voltage	V_{IL}	V_{OUT} = 4.5V V_{OUT} = 9.0V V_{OUT} = 13.5V $\|I_{OUT}\| < 1\mu A$	5 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
Input Current "H"Level	I_{IH}	V_{IH} = 18V	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL} = 0V	18	—	−0.1	—	-10^{-5}	−0.1	—	−1.0	μA
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ *	5 10 15	— — —	0.25 0.50 1.00	— — —	0.001 0.001 0.002	0.25 0.50 1.00	— — —	7.5 15.0 30.0	μA

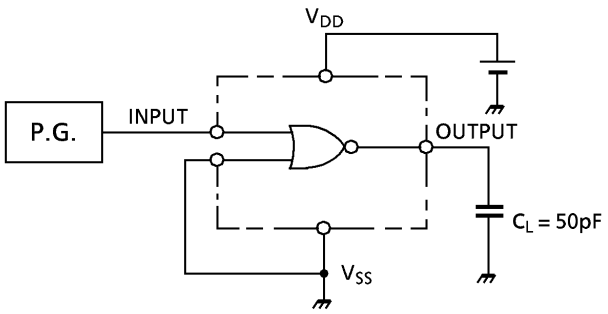
* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, C_L = 50pF)

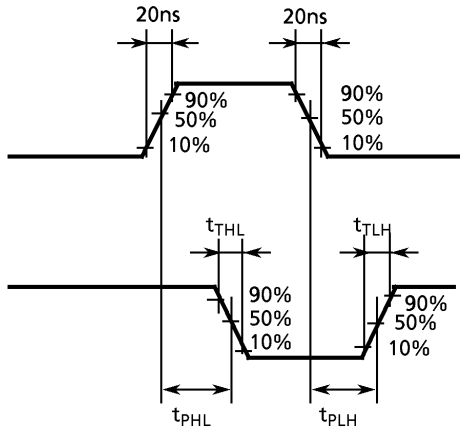
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH}		5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output Transition Time	t_{THL}		5	—	70	200	
			10	—	35	100	
			15	—	30	80	
Propagation Delay Time	t_{pLH}		5	—	65	200	
			10	—	30	100	
			15	—	25	80	
Propagation Delay Time	t_{pHL}		5	—	65	200	
			10	—	30	100	
			15	—	25	80	
Input Capacitance	C_{IN}			—	5	7.5	pF

CIRCUIT A D WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

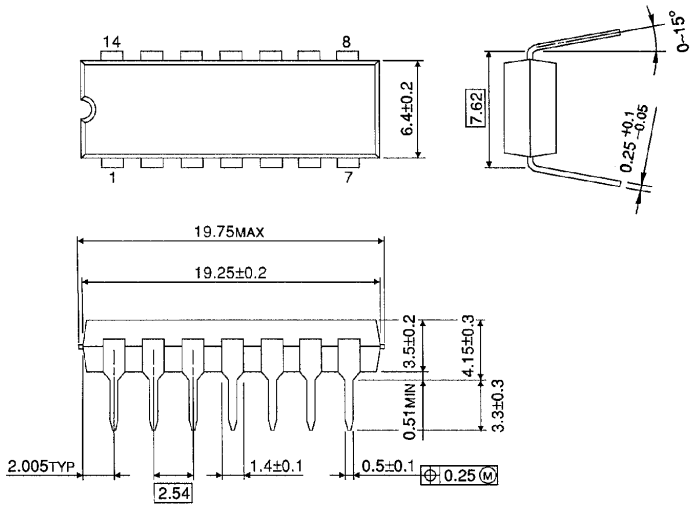
CIRCUIT



WAVEFORM

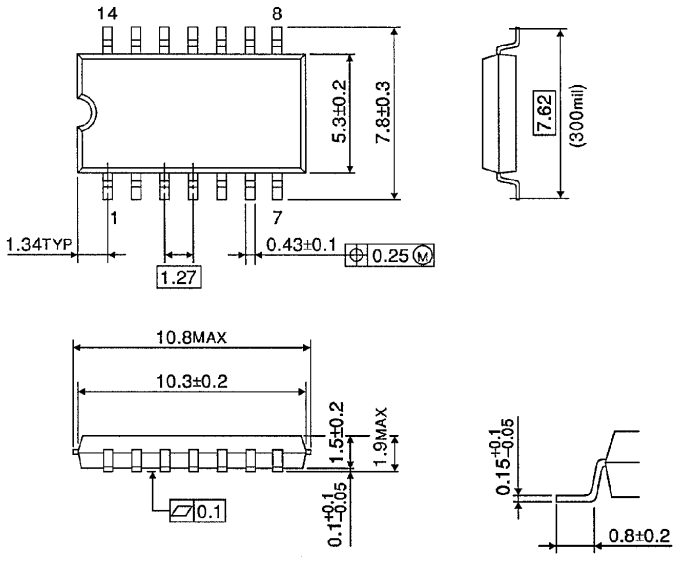


DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54) Unit in mm



Weight : 0.96g (Typ.)

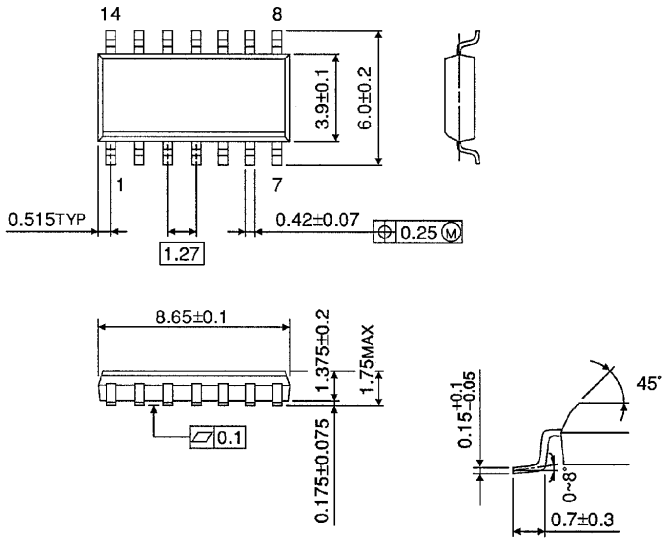
SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

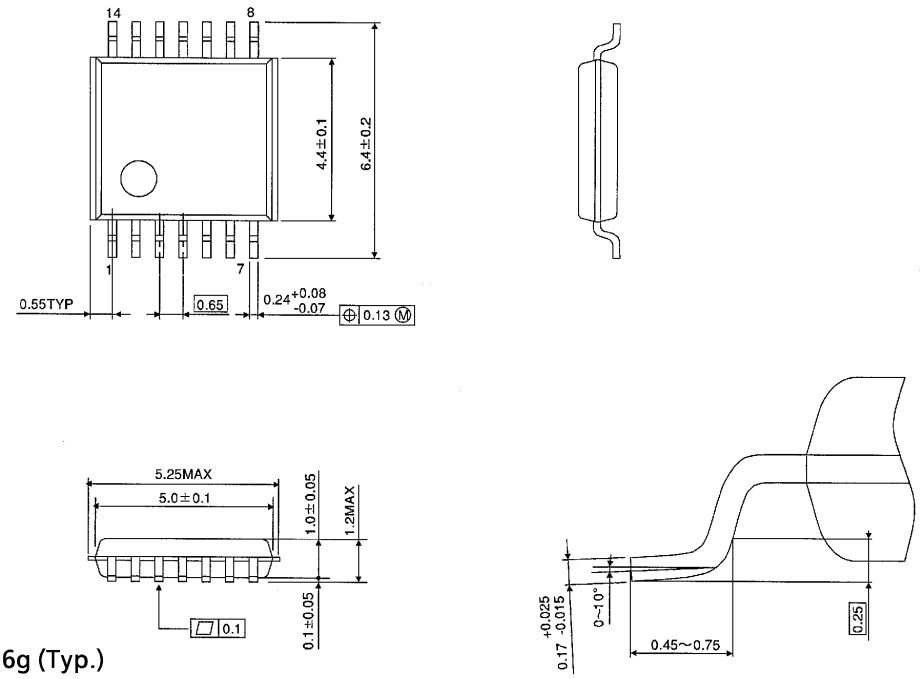
SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

TSSOP 14PIN (170mil BODY) OUTLINE DRAWING (TSSOP14-P-0044-0.65) Unit in mm



Weight : 0.06g (Typ.)